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MT9074

T1/E1/J1 Single Chip Transceiver

Data Sheet

August 2011

Features

- Combined E1 (PCM30) and T1 (D4/ESF) framer, Line Interface Unit (LIU) and link controller with optional digital framer only mode
- In T1 mode the LIU can recover signals attenuated by up to 30 dB (5000 ft. of 24 AWG cable)
- In E1 mode the LIU can recover signals attenuated by up to 30 dB (1900 m. of 0.65 mm cable)
- Two HDLCs: FDL and channel 24 in T1 mode, timeslot 0 (Sa bits) and timeslot 16 in E1 mode
- Two-frame elastic buffer in Rx & Tx (T1) directions
- Programmable transmit delay through transmit slip buffer
- Low jitter DPLL for clock generation
- Enhanced alarms, performance monitoring and error insertion functions
- Intel or Motorola non-multiplexed parallel microprocessor interface
- ST-BUS 2.048 Mbit/s backplane bus for both data and signaling
- Japan Telecom J1 Framing and Yellow Alarm

Ordering Information

MT9074AL1	100 Pin MQFP*	Trays
MT9074AP1	68 Pin PLCC*	Tubes
MT9074APR1	68 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

- Hardware data link access
- JTAG Boundary Scan

Applications

- E1/T1 add/drop multiplexers and channel banks
- CO and PBX equipment interfaces
- Primary Rate ISDN nodes
- Digital Cross-connect Systems (DCS)

* MT9074A was revised after its market introduction. Software can confirm that the installed chip is the most recent revision of MT9074A as follows:

1. In T1 mode, the LSB (Least Significant Bit) of the Synchronization Status Word - bit 0, Page 3 Address 10H is set high.
2. Batch codes 61755.0 or higher, and/or date code beginning with 00, 01, 02, etc.

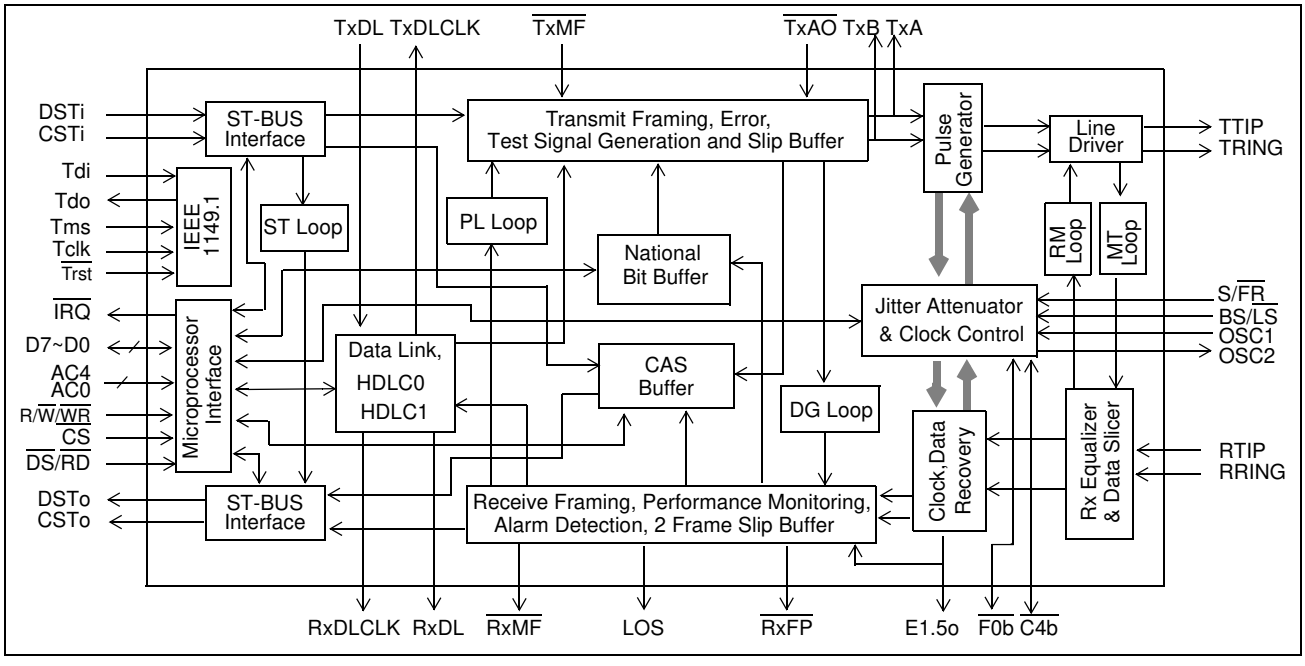


Figure 1 - Functional Block Diagram

Description

The MT9074 is a single chip device, operable in either T1 or E1 mode, integrating either an advanced T1 (T1 mode) or PCM30 (E1 mode) framer with a Line Interface Unit (LIU).

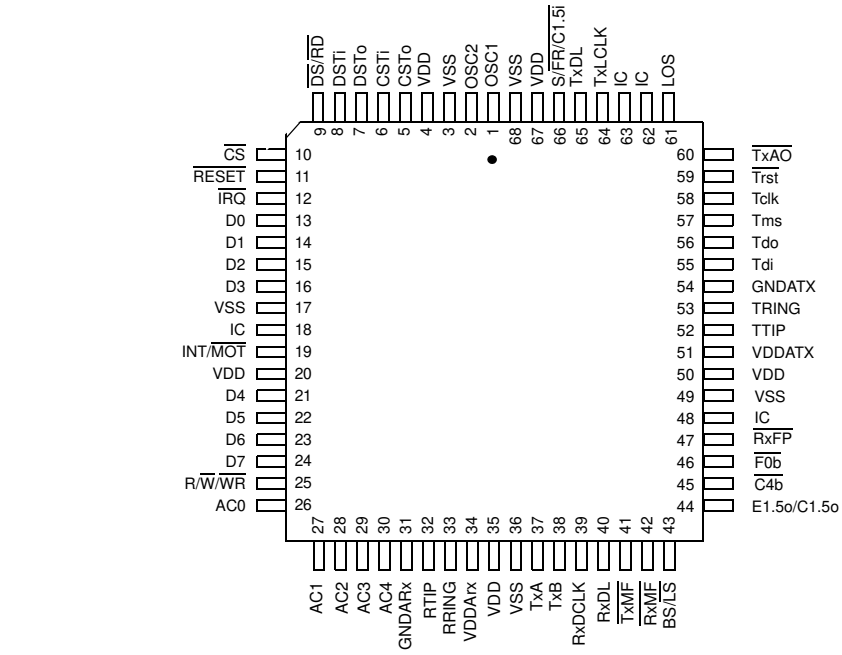
The framer interfaces to a 2.048 Mbit/s backplane providing selectable data link access with optional HDLC controllers for either the FDL bits and channel 24 (T1 mode) or S_a bits and channel 16 (E1 mode). The LIU interfaces the framer to T1 (T1 mode) or PCM30 (E1 mode) transformer-isolated four-wire line with minimal external components required.

In T1 mode, the MT9074 supports D4, ESF and SLC-96 formats, meeting the latest recommendations including ITU I.431, AT&T PUB43801, TR-62411, ANSI T1.102, T1.403 and T1.408. In E1 mode the MT9074 supports the latest ITU-T Recommendations including G.703, G.704, G.706, G.732, G.775, G.796, G.823 for PCM30, and I.431 for ISDN primary rate. It also supports ETSI ETS 300 011, ETS 300 166 and ETS 300 233.

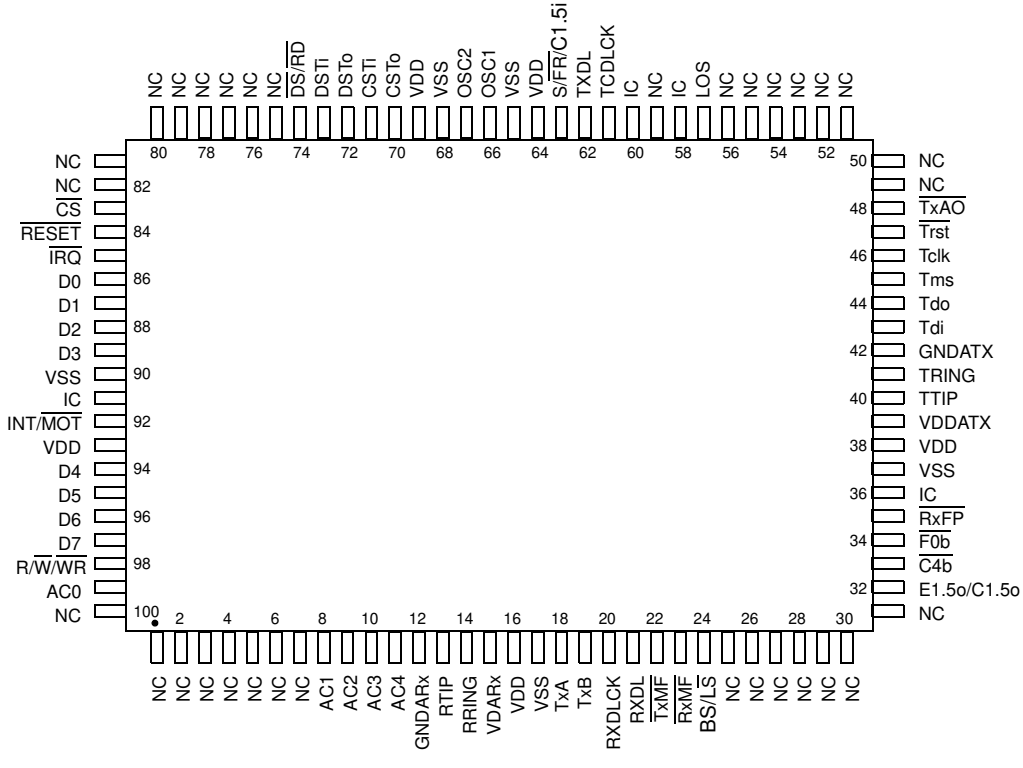
Change Summary

Changes from the August 2005 issue to the August 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.



68 PIN PLCC



100 PIN MQFP (JEDEC MO-112)

Figure 2 - Pin Connections

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Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
1	66	**OSC1**	**Oscillator Input.** This pin is either connected via a 20.000 MHz crystal to OSC2 where a crystal is used, or is directly driven when a 20.000 MHz. oscillator is employed**.**
2	67	**OSC2**	**Oscillator Output.** Connect a 20.0 MHz crystal between OSC1 and OSC2. Not suitable for driving other devices.
3	68	**V_{SS}**	**Negative Power Supply (Input).** Digital ground.
4	69	**V_{DD}**	**Positive Power Supply (Input).** Digital supply (+5 V ± 5%).
5	70	**CSTo**	**Control ST-BUS Output.** CSTo carries serial streams for CAS and CCS respectively a 2.048 Mbit/s ST-BUS status stream which contains the 30 receive signaling nibbles (ABCDZZZZ or ZZZZABCD). The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are tristated when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and tristated nibbles are reversed.
6	71	**CSTi**	**Control ST-BUS Input.** CSTi carries serial streams for CAS and CCS respectively a 2.048 Mbit/s ST-BUS control stream which contains the 30 transmit signaling nibbles (ABCDXXXX or XXXXABCD) when RPSIG=0. When RPSIG=1 this pin has no function. The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are ignored when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and ignored nibbles is reversed.
7	72	**DSTo**	**Data ST-BUS Output.** A 2.048 Mbit/s serial stream which contains the 24/30 PCM(T1/E1) or data channels received on the PCM24/30 (T1/E1) line.
8	73	**DSTi**	**Data ST-BUS Input.** A 2.048 Mbit/s serial stream which contains the 24/30 (T1/E1)PCM or data channels to be transmitted on the PCM24/30 (T1/E1)line.
9	74	**$\overline{DS}$/$\overline{RD}$**	**Data/Read Strobe (Input)**. In Motorola mode ($\overline{DS}$), this input is the active low data strobe of the microprocessor interface. In Intel mode ($\overline{RD}$), this input is the active low read strobe of the microprocessor interface.
10	83	**$\overline{CS}$**	**Chip Select (Input)**. This active low input enables the non-multiplexed parallel microprocessor interface of the MT9074. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
11	84	**$\overline{RESET}$**	**RESET (Input).** This active low input puts the MT9074 in a reset condition. $\overline{RESET}$ should be set to high for normal operation. The MT9074 should be reset after power-up. The $\overline{RESET}$ pin must be held low for a minimum of 1μsec. to reset the device properly.
12	85	**$\overline{IRQ}$**	**Interrupt Request (Output)**. A low on this output pin indicates that an interrupt request is presented. $\overline{IRQ}$ is an open drain output that should be connected to V_{DD} through a pull-up resistor. An active low $\overline{CS}$ signal is not required for this pin to function.

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
13 - 16	86-89	D0 - D3	**Data 0 to Data 3 (Three-state I/O).** These signals combined with D4-D7 form the bidirectional data bus of the microprocessor interface (D0 is the least significant bit).
17	90	Vss	**Negative Power Supply (Input).** Digital ground.
18	91	IC	**Internal Connection**. Tie to Vss (ground) for normal operation.
19	92	INT/$\overline{\text{MOT}}$	**Intel/Motorola Mode Selection (Input).**A high on this pin configures the processor interface for the Intel parallel non-multiplexed bus type. A low configures the processor interface for the Motorola parallel non-multiplexed type.
20	93	VDD	**Positive Power Supply (Input).** Digital supply (+5 V± 5%).
21 - 24	94-97	D4 - D7	**Data 4 to Data 7 (Three-state I/O).** These signals combined with D0-D3 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit)**.**
25	98	R/$\overline{\text{W}}$/$\overline{\text{WR}}$	Read/Write/Write Strobe (Input). In Motorola mode (R/$\overline{\text{W}}$), this input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{\text{W}}$ is high, the parallel processor is reading data from the MT9074. When low, the parallel processor is writing data to the MT9074. For Intel mode ($\overline{\text{WR}}$), this active low write strobe configures the data bus lines as input.
26 - 30	99, 8-11	AC0 - AC4	**Address/Control 0 to 4 (Inputs).** Address and control inputs for the non-multiplexed parallel processor interface. AC0 is the least significant input.
31	12	GND_{ARx}	**Receive Analog Ground (Input)**. Analog ground for the LIU receiver.
32 33	13 14	RTIP RRING	**Receive TIP and RING (Input)**. Differential inputs for the receive line signal - must be transformer coupled (See Figure 5). In digital framer mode these are TTL level inputs that connect to the digital outputs of a receiver. If the receiver serial data output is NRZ connect that output to RTIP. If the receiver data output is split phase unipolar signal connect one signal to RTIP and the complementary signal to RRING.
34	15	VDD_{ARx}	**Receive Analog Power Supply (Input).** Analog supply for the LIU receiver (+5 V ± 5%).
35	16	VDD	**Positive Power Supply (Input).** Digital supply (+5 V ± 5%).
36	17	VSS	**Negative Power Supply (Input).** Digital ground.
37	18	TxA	**Transmit A (Output).** When the internal LIU is disabled (digital framer only mode), if control bit NRZ=1, and NRZ output data is clocked out on pin TxA with the rising edge of C1.50 (TxB has no function when NRZ format is selected). If NRZ=0, pins TxA and TxB are a complementary pair of signals that output digital dual-rail clocked out with the rising edge of C1.50.
38	19	TxB	**Transmit B (Output).** When the internal LIU is disabled and control bit NRZ=0, pins TxA and TxB are a complementary pair of signals that output digital dual-rail data clocked out with the rising edge of C1.50.
39	20	RxDLCLK	**Data Link Clock (Output)**. A gapped clock signal derived from the extracted clock from the line clock, available for an external device to clock in RxDL data (at 4, 8, 12, 16 or 20 kHz) on the rising edge.

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
40	21	RxDL	**Receive Data Link (Output).** A serial bit stream containing received line data after zero code suppression. This data is clocked out with the rising edge of E1.5o.
41	22	$\overline{\text{TxMF}}$	**Transmit Multiframe Boundary (Input)**. An active low input used to set the transmit multiframe boundary (CAS or CRC multiframe). The MT9074 will generate its own multiframe if this pin is held high. This input is usually pulled high for most applications.
42	23	$\overline{\text{RxMF}}$	**Receive Multiframe Boundary (Output).** An output pulse delimiting the received multiframe boundary. The next frame output on the data stream (DSTo) is basic frame zero on the T1 or PCM30 link. In E1 mode this receive multiframe signal can be related to either the receive CRC multiframe (page 01H, address 17H, bit 6, MFSEL=1) or the receive signaling multiframe (MFSEL=0).
43	24	BS/$\overline{\text{LS}}$	**Bus/Line Synchronization Mode Selection (Input)**. If high, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be inputs; if low, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be outputs.
44	32	E1.5o/C1.5o	**2.048 MHz in E1 mode or 1.544 MHz in T1 mode, Extracted Clock (Output).** If the internal L/U is enabled, this output is the clock extracted from the received signal and used internally to clock in data received on RTIP and RRING. If the internal LIU is disabled (digital framer mode), this output is a 1.544 MHz clock (T1) C1.5o or a 2.048 MHz clock C2o which clocks out the transmit digital data TXA, TXB.
45	33	$\overline{\text{C4b}}$	**4.096 MHz System Clock (Input/Output).** $\overline{\text{C4b}}$ is the clock for the $\overline{\text{ST}}$-BUS sections and transmit serial PCM data of the MT9074. In the free-run (S/$\overline{\text{FR}}$=0) or line synchronous mode (S/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in bus synchronous mode (S/$\overline{\text{FR}}$=1) this signal is an input clock which is phase-locked to the extracted clock (E1.5o).
46	34	$\overline{\text{F0b}}$	**Frame Pulse (Input/Output).** This is the ST-BUS frame synchronization signal, which delimits the 32 channel frame of CSTi, CSTo, DSTi, DSTo and the PCM30 link. In the free-run (S/$\overline{\text{FR}}$=0) or line synchronous mode (S/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in the bus synchronous mode (S/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=1) this signal is an input.
47	35	$\overline{\text{RxFP}}$	**Receive Frame Pulse (Output).** An 8 kHz pulse signal, which is low for one extracted clock period. This signal is synchronized to the receive DS1 or PCM30 basic frame boundary.
48	36	IC	**Internal Connection.** Must be left open for normal operation.
49	37	V_{SS}	**Negative Power Supply (Input).** Digital ground.
50	38	V_{DD}	**Positive Power Supply (Input).** Digital supply (+5 V ± 5%).
51	39	VDD_{ATx}	**Transmit Analog Power Supply (Input).** Analog supply for the LIU transmitter (+5 V ± 5% 10%)).
52 53	40 41	TTIP TRING	**Transmit TIP and RING (Outputs).** Differential outputs for the transmit DS1 line signal - must be transformer coupled (See Figure 5).
54	42	GND_{ATx}	**Transmit Analog Ground (Input).** Analog ground for the LIU transmitter.
55	43	Tdi	**IEEE 1149.1 Test Data Input.** If not used, this pin should be pulled high.

Pin Description

Pin #		Name	Description
68 Pin PLCC	100 Pin MQFP		
56	44	Tdo	**IEEE 1149.1 Test Data Output.** If not used, this pin should be left unconnected.
57	45	Tms	**IEEE 1149.1 Test Mode Selection (Input).** If not used, this pin should be pulled high.
58	46	Tclk	**IEEE 1149.1 Test Clock Signal (Input).** If not used, this pin should be pulled high.
59	47	$\overline{\text{Trst}}$	**IEEE 1149.1 Reset Signal (Input).** If not used, this pin should be held low.
60	48	$\overline{\text{TxAO}}$	**Transmit All Ones (Input).**High - TTIP, TRING will transmit data normally. Low - TTIP, TRING will transmit an all ones signal.
61	57	LOS	**Loss of signal or synchronization (Output).**When high, and LOS/LOF (page 1 address 19 bit 0) is zero, this signal indicates that the receive portion of the MT9074 is either not detecting an incoming signal (bit LLOS on page 03H address 16H is one) or is detecting a loss of basic frame alignment condition (bit SYNC on page 03H address 10H is one). If LOS/LOF=1, a high on this pin indicates a loss of signal condition.
62	58	IC	**Internal Connection.** Tie to Vss (Ground) for normal operation.
	59	NC	**No Connection.** Leave open for normal operation.
63	60	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
64	61	TxDLCLK	**Transmit Data Link Clock (Output).** A gapped clock signal derived from a gated 2.048 Mbit/s clock for transmit data link at 4, 8, 12, 16 or 20 kHz. The transmit data link data (TxDL) is clocked in on the rising edge of TxDLCLK. TxDLCLK can also be used to clock DL data out of an external serial controller.
65	62	TxDL	**Transmit Data Link (Input).** An input serial stream of transmit data link data at 4, 8, 12, 16 or 20 kbit/s.
66	63	S/$\overline{\text{FR}}$/C1.5i	**Sychronous/Freerun Extracted Clock (Input):** If low, and the internal LIU is enabled, the MT9074 is in free run mode. Pins 45 C4b and 46 F0b are outputs generating system clocks. Slips will occur in the receive slip buffer as a result of any deviation between the MT9074's internal PLL (which is free - running) and the frequency of the incoming line data. If high, and the internal LIU is enabled, the MT9074 is in Bus or Line Synchronization mode depending on the BS/$\overline{\text{LS}}$ pin. If the internal LIU is disabled, in digital framer mode, this pin (C1.5i) takes an input clock 1.544 Mhz (T1) / 2.048 Mhz (E1) that clocks in the received digital data on pins RTIP and RRING with its rising edge.
67	64	VDD	**Positive Power Supply (Input).** Digital supply (+5 V ± 5%).
68	65	VSS	**Negative Power Supply (Input).** Digital ground.

Device Overview

The MT9074 in T1 mode operates as an advanced T1 framer with an on-chip Line Interface Unit (LIU) that meets or supports the recommendations including ITU I.431, AT&T PUB43801, TR-62411, ANSI T1.102, T.403 and T.408.

The MT9074 in E1 mode operates as an advanced PCM30 framer with an on-chip Line Interface Unit (LIU) that meets or supports the latest ITU-T Recommendations for PCM30 and ISDN primary rate including G.703, G.704, G.706, G.775, G.796, G.732, G.823 and I.431. It also meets or supports the layer 1 requirements of ETSI ETS 300 011, ETS 300 166, ETS 300 233 and BS6450.

The Line Interface Unit (LIU) of the MT9074 interfaces the digital framer functions to either the DS1 (T1 mode) or PCM30 (E1 mode) transformer-isolated four wire line. The transmit portion of the MT9074 LIU consists of a digital buffer, a digital-to-analog converter, and a differential line driver. The receiver portion of the MT9074 LIU consists of an input signal peak detector, an optional equalizer, a smoothing filter, data and clock slicers and a clock extractor.

System timing may be slaved to the line, operated in free-run mode or controlled by an external timing source. In T1 mode the MT9074 contains a PLL which always generates the transmit timing for the LIU. In E1 mode the LIU also contains a Jitter Attenuator (JA), which can be included in either the transmit or receive path. The MT9074 will attenuate jitter from 2.5 Hz and roll-off at a rate of 20 dB/decade. The intrinsic jitter is less than 0.02 UI. The PLL output (@1.544 MHz for T1 mode and @2.048 MHz for E1 mode) clocks out the transmit line data.

To accommodate some special applications, the MT9074 also supports a digital framer only mode by providing direct access to the transmit and receive data in digital format, i.e., by-passing the analog LIU front-end.

The digital portion of the MT9074 connects selected channels of an incoming stream of time multiplexed 2.048 Mbit/s PCM channels to the transmit payload of either the T1 or E1 trunk, while the receive payload is connected to the ST-BUS 2.048 Mbit/s backplane bus for both data and signaling with channel times and the frame boundary synchronous to the transmit side. Control, reporting and conditioning of the line is implemented via a parallel microprocessor interface.

The MT9074 has a comprehensive suite of status, alarm, performance monitoring and reporting features. These include counters for BPVs, CRC errors, F-bit errors (T1 only), E-bit errors (E1 only), errored frame alignment signals (E1 only), BERT, OOF (T1 only), and RAI and continuous CRC errors (E1 only). Also, included are transmission error insertion for BPVs, CRC-6 errors (T1 only), CRC-4 errors (E1 only), framing bit errors (T1 only), frame and non-frame alignment signal errors (E1 only), payload errors and loss of signal errors. A built-in PRBS generator (2^{15} -1) can be connected to any combination of outgoing channels; an equivalent PRBS error detector can be independently connected to any combination of receive channels.

A complete set of loopbacks has been implemented, which include digital, remote, ST-BUS, payload, local, metallic and remote time slot.

The MT9074 also provides a comprehensive set of maskable interrupts. Interrupt sources consist of synchronization status, alarm status, counter indication and overflow, timer status, slip indication, maintenance functions and receive channel associated signaling bit changes.

In T1 mode the framer operates in any one of the framing modes: D4, SLC-96 and Extended Superframe (ESF). The ESF FDL bits of the MT9074 can be accessed either through the data link pins TxDL, RxDL, RxDLCLK and TxDLCLK, or through internal registers for Bit Oriented Messages, or through a built-in HDLC. A second HDLC may be connected to DS1 channel 24 for the ISDN Primary Rate signaling applications.

In E1 mode the MT9074 operates in either termination or transparent modes selectable via software control. In the termination mode the CRC-4 calculation is performed as part of the framing algorithm. In the transmit transparent mode, no framing or signaling is imposed on the data transmit from DSTi on the line. In addition, the MT9074 optionally allows the data link maintenance channel to be modified and updates the CRC-4 remainder bits to reflect the modification. All channel, framing and signaling data passes through the device unaltered. This is useful for intermediate point applications of a PCM30 link where the data link data is modified, but the error information transported by the CRC-4 bits must be passed to the terminating end. In the receive transparent mode, the

received line data is channelled to DSTo with framing operations disabled, consequently, the data passes through the slip buffer and drives DSTo with an arbitrary alignment.

In E1 mode the S_a bits can be accessed by the MT9074 in the following three ways:

- Programming a register;
- Data link pins TxDL, RxDL, RxDLCLK and TxDLCLK;
- HDLC Controller with a 128 byte FIFO.

A second HDLC Controller with a 128 byte FIFO is available for connection to timeslot 16 in E1 mode.

Functional Description

MT9074 Line Interface Unit (LIU)

Receiver

The receiver portion of the MT9074 LIU consists of an input signal peak detector, an optional equalizer with two separate high pass sections, a smoothing filter, data and clock slicers and a clock extractor. Receive equalization gain can be set manually (i.e., software) or it can be determined automatically by peak detectors.

The output of the receive equalizer is conditioned by a smoothing filter and is passed on to the clock and data slicer. The clock slicer output signal drives a phase locked loop, which generates an extracted clock (C1.50). This extracted clock is used to sample the output of the data comparator.

In T1 mode, the receiver portion of the LIU can reliably recover clock and data from signals attenuated by up to 30 dB @ 772 kHz (translates to 5000 ft. of PIC 24 AWG cable) and tolerate jitter to the maximum specified by AT&T TR 62411 (see Figure 3).

In E1 mode the receiver portion of the LIU can reliably recover clock and data from signals attenuated by up to 30 dB @ 1024 kHz (translates to 1900 m. of PIC 0.65 mm or 22 AWG cable) and tolerate jitter to the maximum specified by ETS 300 011 (Figure 4).

The LOS output pin function is user selectable to indicate any combination of loss of signal and/or loss of basic frame synchronization condition.

The LLOS (Loss of Signal) status bit indicates when the receive signal level is lower than the analog threshold for at least 1 millisecond, or when more than 192 consecutive zeros have been received. In E1 mode the analog threshold is either of -20 dB or -40 dB. For T1 mode the analog threshold is -40 dB.

In T1 mode, the receive LIU circuit requires a terminating resistor of 100 Ω across the device side of the receive 1:1 transformer.

In E1 mode the receive LIU circuit requires a terminating resistor of either 120 Ω or 75 Ω across the device side of the receive1:1 transformer.

The jitter tolerance of the clock extractor circuit exceeds the requirements of TR 62411 in T1 mode (see Figure 3) and G.823 in E1 mode (see Figure 4).

Transmitter

The transmit portion of the MT9074 LIU consists of a high speed digital-to-analog converter and complementary line drivers.

When a pulse is to be transmitted, a sequence of digital values (dependent on transmit equalization) are read out of a ROM by a high speed clock. These values drive the digital-to-analog converter to produce an analog signal, which is passed to the complementary line drivers.

The complementary line drivers are designed to drive a 1:2 step-up transformer (see Figure 5 for T1 mode and Figure 6 for E1 mode). A 0.47 uF capacitor is required between the TTIP and the transmit transformer. Resistors RT (as shown in Figure 5) are for termination for transmit return loss. The values of RT may be optimized for T1 mode, E1 120 Ω lines, E1 75 Ω lines or set at a compromise value to serve multiple applications. Program the LIU Control Word (address 1FH page 1) to adjust the pulse amplitude accordingly.

Alternatively, the pulse level and shape may be discretely programmed by writing to the Custom Pulse Level registers (addresses 1CH to 1FH, page 2) and setting the Custom Transmit Pulse bit high (bit 3 of the Transmit Pulse Control Word). In this case the output of each of the registers directly drives the D/A converter going to the line driver. Tables 1 and 2 show recommended transmit pulse amplitude settings.

In T1 mode, the template for the transmitted pulse (the DSX-1 template) is shown in Figure 7. The nominal peak voltage of a mark is 3 volts. The ratio of the amplitude of the transmit pulses generated by TTIP and TRING lie between 0.95 and 1.05.

In E1 mode, the template for the transmitted pulse, as specified in G.703, is shown in Figure 8. The nominal peak voltage of a mark is 3 volts for 120 Ω twisted pair applications and 2.37 volts for 75 Ω coax applications. The ratio of the amplitude of the transmit pulses generated by TTIP and TRING lie between 0.95 and 1.05.

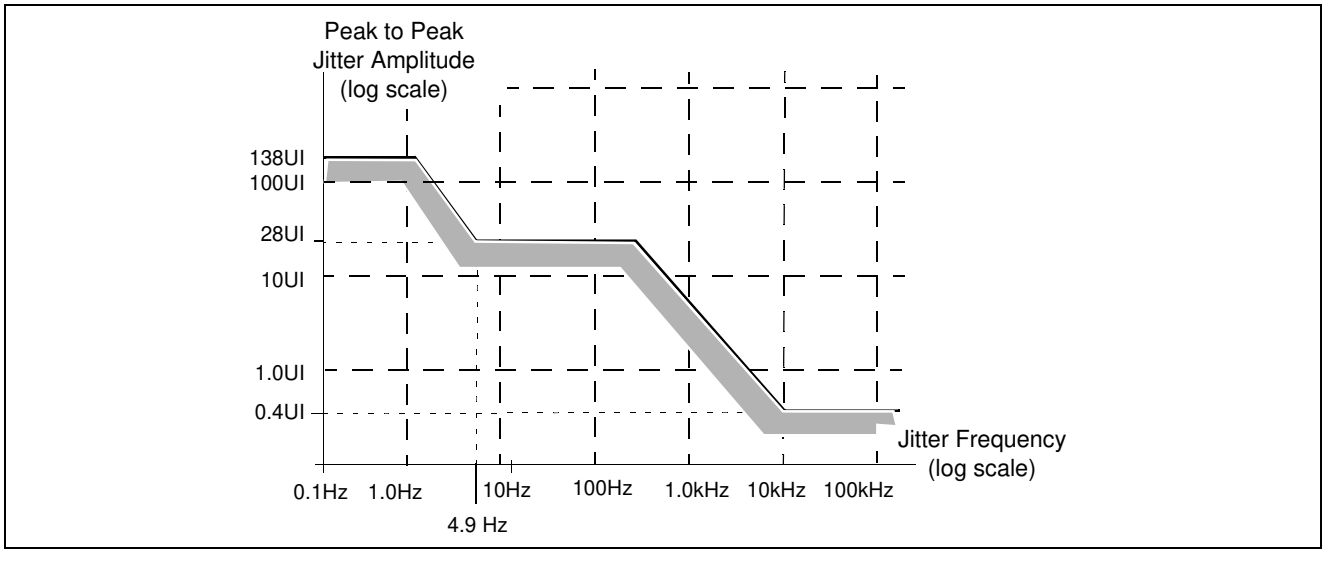

Figure 3 - Input Jitter Tolerance as Recommended by TR-62411 (T1)

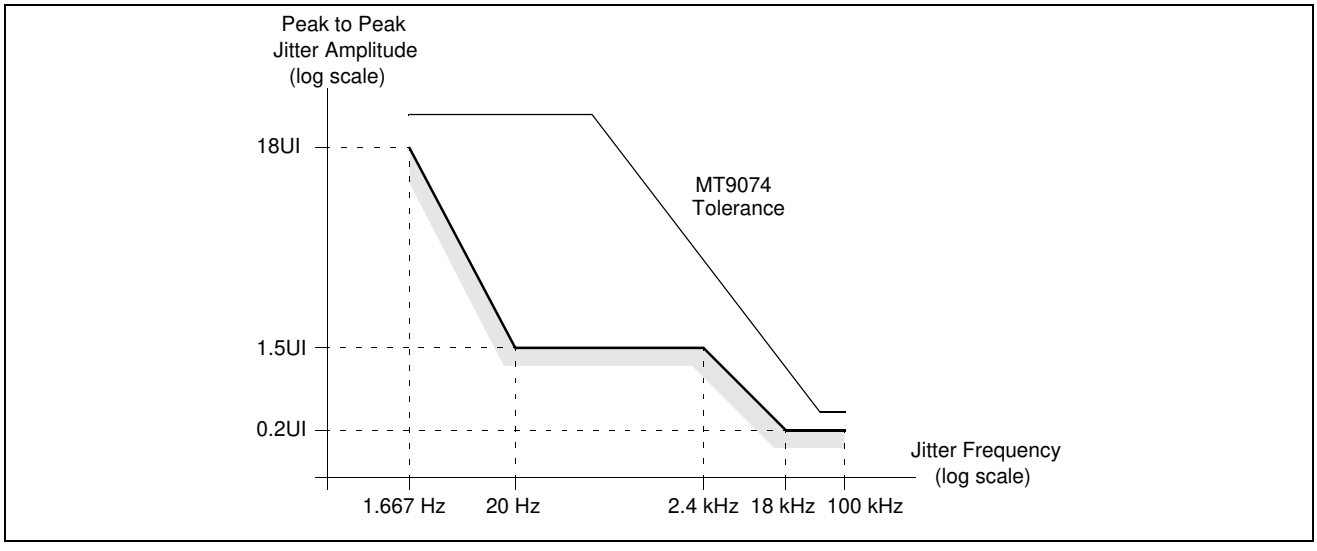

Figure 4 - Input Jitter Tolerance as recommended by ETSI 300 011 (E1)

Name	Functional Description
TXL2-0	**Transmit Line Build Out 2 - 0**. Setting these bits shapes the transmit pulse as detailed in the table below:

TXL2	TXL1	TXL0	Line Build Out
0	0	0	0 to 133 feet/ 0 dB
0	0	1	133 to 266 feet
0	1	0	266 to 399 feet
0	1	1	399 to 533 feet
1	0	0	533 to 655 feet
1	0	1	-7.5 dB
1	1	0	-15 dB
1	1	1	-22.5 dB

After reset these bits are zero.

Table 1 - Transmit Line Build Out (T1)

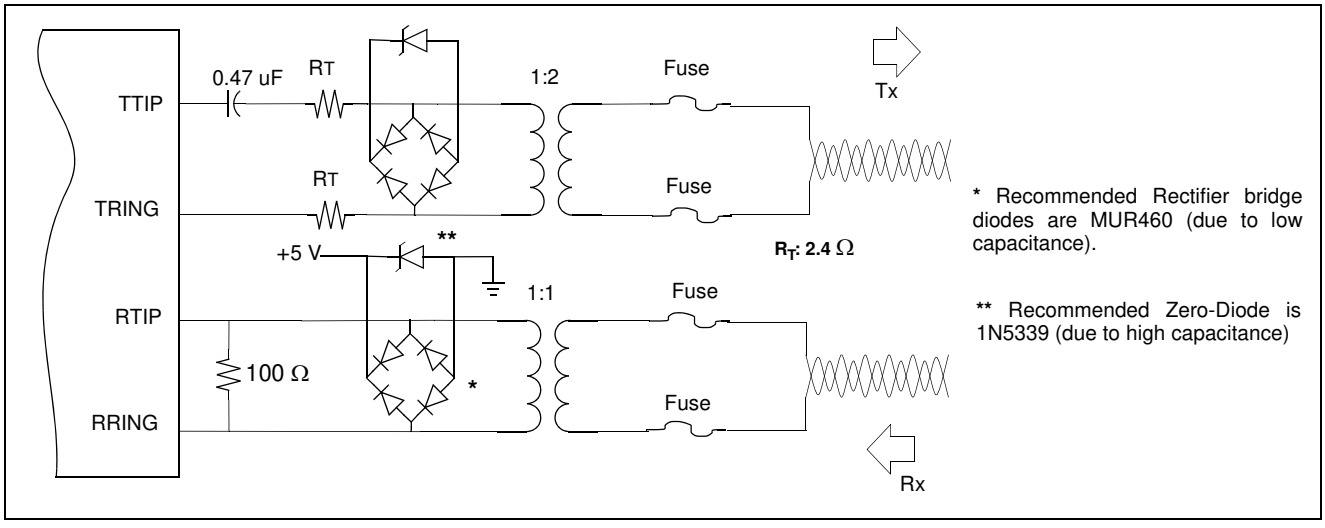

Figure 5 - Analog Line Interface (T1)

Name	Functional Description
TX2-0	**Transmit pulse amplitude.** Select the TX2 –TX0 bits according to the line type, value of termination resistors (RT), and transformer turns ratio used TX2 TX1 TX0 Line Impedance(Ω) RT(Ω) Transformer Ratio 0 0 0 120 0 1:2 0 0 1 120 0 1:1 0 1 0 120 15 1:2 0 1 1 120 / 75 12.1 1:2 1 0 0 75 0 1:2 1 0 1 75 0 1:1 1 1 0 75 9.1 1:2 1 1 1 75 / 120 12.1 1:2 After reset these bits are zero.

Table 2 - Transmit Pulse Amplitude (E1)

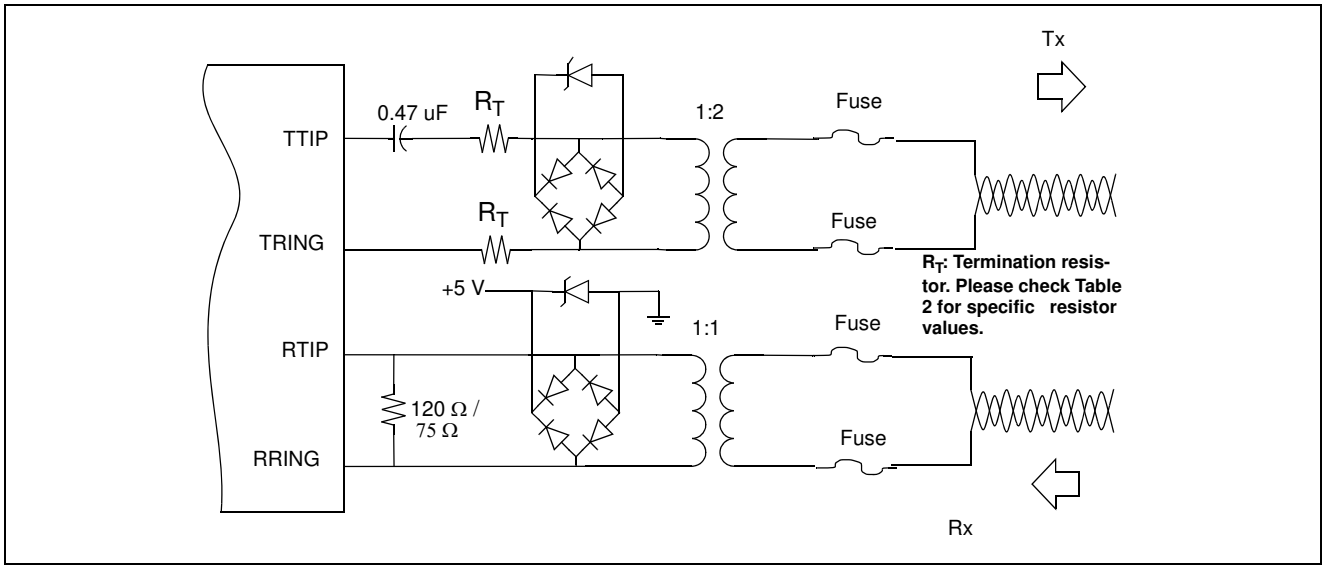

Figure 6 - Analog Line Interface (E1)

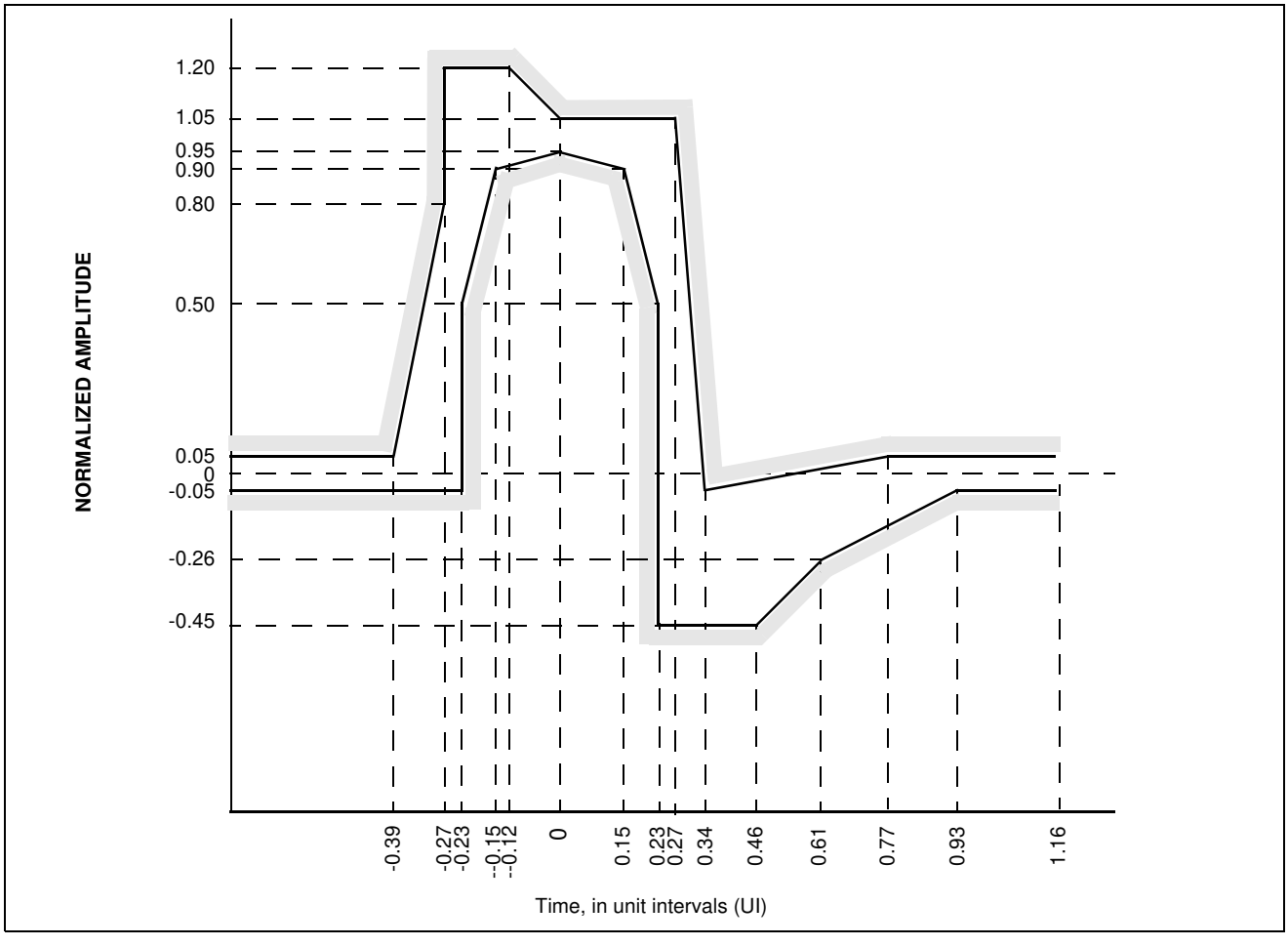

Figure 7 - Pulse Template (T1.403) (T1)

Time (Nanoseconds)	-499	-253	-175	-175	-78	0	175	220	499	752	---	---
Time U.I.	-.77	-.39	-.27	-.27	-.12	0	.27	.34	.77	1.16	---	---
Normalized Amplitude	.05	.05	.8	1.2	1.2	1.05	1.05	-.05	.05	.05	---	---

Table 3 - Maximum Curve for Figure 7

Time (Nanoseconds)	-499	-149	-149	-97	0	97	149	149	298	395	603	752
Time U.I.	-.77	-.23	-.23	-.15	0	.15	.23	.23	.46	.61	.93	1.16
Normalized Amplitude	-.05	-.05	.5	.9	.95	.9	.5	-.45	-.45	-.26	-.05	-.05

Table 4 - Minimum Curve for Figure 7

Note: One Unit Interval = 648 nanoseconds

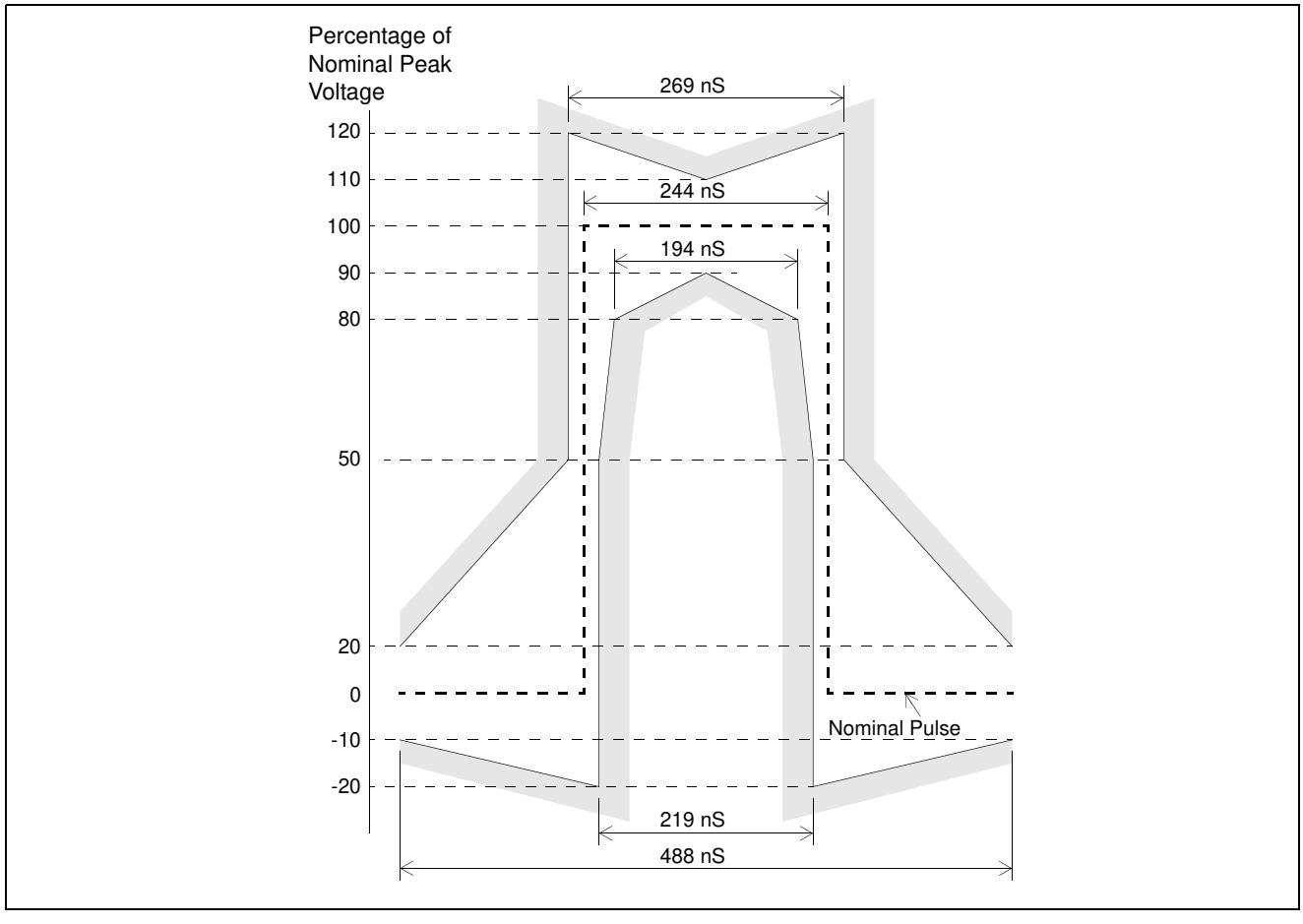

Figure 8 - Pulse Template (G.703)(E1)

20 Mhz Clock

The MT9074 requires a 20 MHz clock. This may provided by a 50 ppm oscillator as per Figure 9.

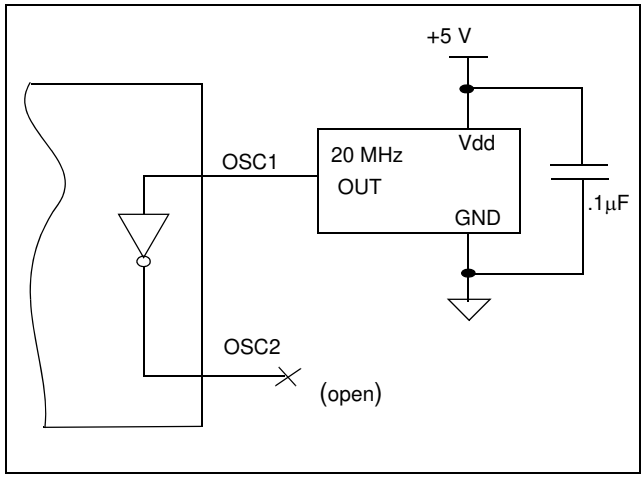

Figure 9 - Clock Oscillator Circuit

Alternatively, a crystal oscillator may be used. A complete oscillator circuit made up of a crystal, resistors and capacitors is shown in Figure 10. The crystal specification is as follows.

Frequency:	*20 MHz*
Tolerance:	*50 ppm*
Oscillation Mode:	*Fundamental*
Resonance Mode:	*Parallel*
Load Capacitance:	*32 pF*
Maximum Series Resistance:	*35 Ω*
Approximate Drive Level:	*1 mW*

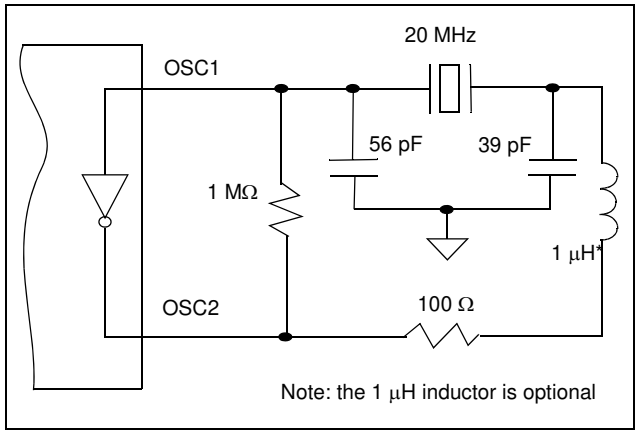

Figure 10 - Crystal Oscillator Circuit

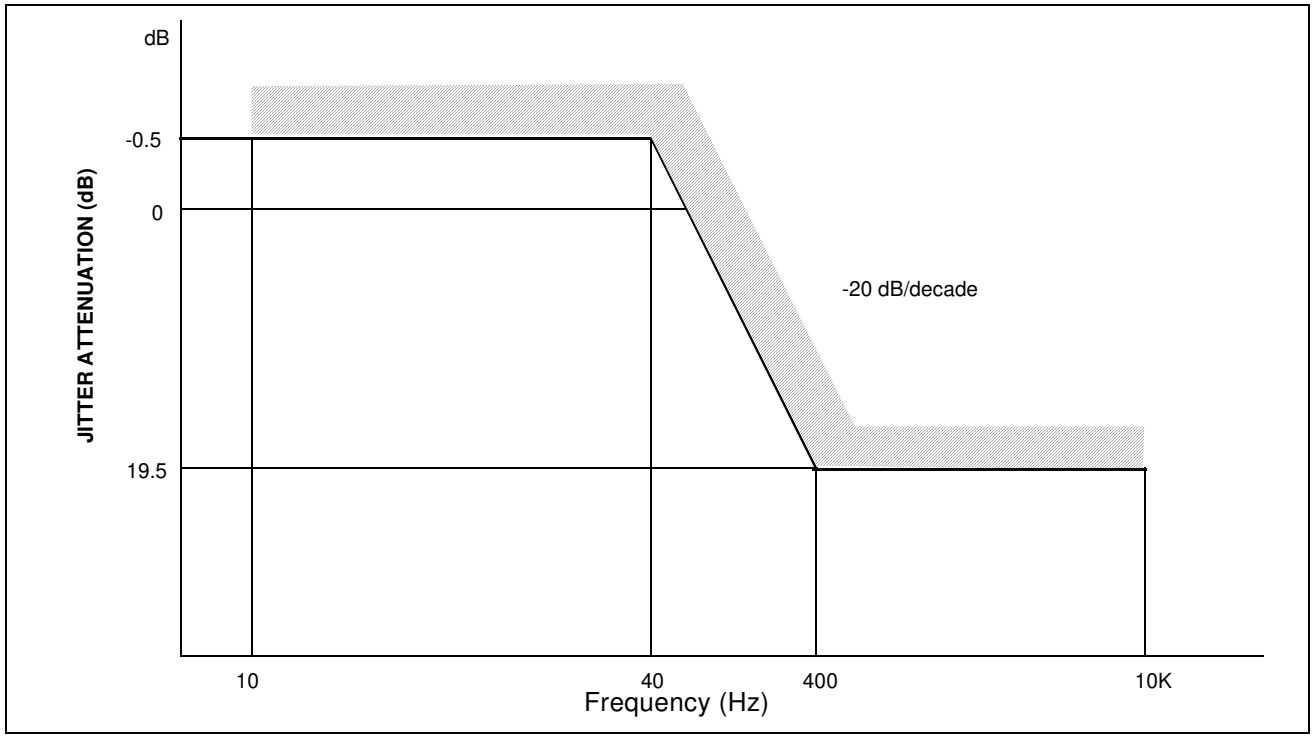

Figure 11 - TR 62411 Jitter Attenuation Curve

Phase Lock Loop (PLL)

The MT9074 contains a PLL, which can be locked to either an input 4.096 Mhz clock or the extracted line clock.The PLL will attenuate jitter from less than 2.5 Hz and roll-off at a rate of 20 dB/decade. Its intrinsic jitter is less than 0.02 UI. The PLL will meet the jitter transfer characteristics as specified by ATT document TR 62411 and the relevant recommendations as shown in Figure 11.

Clock Jitter Attenuation Modes

MT9074 has three basic jitter attenuation modes of operation, selected by the BS/$\overline{LS}$ and S/$\overline{FR}$ control pins. Referring to the mode names given in Table 5 the basic operation of the jitter attenuation modes are:

- System Bus Synchronous Mode
- Line Synchronous Mode
- Free-Run Mode

Mode Name	BS/$\overline{LS}$	S/$\overline{FR}$	Note
System Bus Synchronous	1	1	PLL locked to $\overline{C4b}$
Line Synchronous	0	1	PLL locked to E1.5o
Free-Run	x	0	PLL free - running.

Table 5 - Selection of Clock Jitter Attenuation Modes using the M/$\overline{S}$ and MS/FR Pins

In System Bus Synchronous mode pins $\overline{C4b}$ and $\overline{F0b}$ are always configured as inputs, while in the Line Synchronous and Free-Run modes $\overline{C4b}$ and $\overline{F0b}$ are configured as outputs.

In *System Bus Synchronous* mode an external clock is applied to $\overline{C4b}$. The applied clock is dejittered by the internal PLL before being used to synchronize the transmitted data. The clock extracted (with no jitter attenuation performed) from the receive data can be monitored on pin E1.5o.

In *Line Synchronous* mode, the clock extracted from the receive data is dejittered using the internal PLL and then output on pin $\overline{C4b}$. Pin E1.5o provides the extracted receive clock before it has been dejittered. The transmit data is synchronous to the clean receive clock.

In *Free-Run* mode the transmit data is synchronized to the internally generated clock. The internal clock is output on pin $\overline{C4b}$. The clock signal extracted from the receive data is not dejittered and is output directly on E1.5o.

Depending on the mode selection above, the PLL can either attenuate transmit clock jitter or the receive clock jitter. Table 5 shows the appropriate configuration of each control pin to achieve the appropriate mode and Jitter attenuation capability of the MT9074

The Digital Interface

T1 Digital Interface

In T1 mode DS1 frames are 193 bits long and are transmitted at a frame repetition rate of 8000 Hz, which results in an aggregate bit rate of 193 bits x 8000/sec= 1.544 Mbits/sec. The actual bit rate is 1.544 Mbits/sec +/-50 ppm optionally encoded in B8ZS format. The Zero Suppression control register (page 1, address 15H,) selects either B8ZS encoding, forced one stuffing or alternate mark inversion (AMI) encoding. Basic frames are divided into 24 time slots numbered 1 to 24. Each time slot is 8 bits in length and is transmitted most significant bit first (numbered bit 1). This results in a single time slot data rate of 8 bits x 8000/sec. = 64 kbits/sec.

It should be noted that the Zarlink ST-BUS has 32 channels numbered 0 to 31. When mapping to the DS1 payload only the first 24 time slots and the last (time slot 31, for the overhead bit) of an ST-BUS are used (see Table 6). All unused channels are tristate.

When signaling information is written to the MT9074 in T1 mode using ST-BUS control links (as opposed to direct writes by the microport to the on - board signaling registers), the CSTi channels corresponding to the selected DSTi channels streams are used to transmit the signaling bits.

Since the maximum number of signaling bits associated with any channel is 4 (in the case of ABCD), only half a CSTi channel is required for sourcing the signaling bits. The choice of which half of the channel to use is selected by the control bit MSN (page 01H address 14H). The same control bit selects which half of the CSTo channel will contain receive signaling information (the other nibble in the channel being tristate). Unused channels are tristate.

The most significant bit of an eight bit ST-BUS channel is numbered bit 7 (see Zarlink Application Note MSAN-126). Therefore, ST-BUS bit 7 is synonymous with DS1 bit 1; bit 6 with bit 2: and so on.

Frame and Superframe Structure in T1 mode