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Features

August 2011

- Combined PCM 30 framer, Line Interface Unit (LIU) and link controllers in a 68 pin PLCC or 100 pin MQFP package

- Selectable bit rate data link access with optional S_a bits HDLC controller (HDLC0) and channel 16 HDLC controller (HDLC1)

- LIU dynamic range of 20 dB

- Enhanced performance monitoring and programmable error insertion functions

- Low jitter DPLL for clock generation

- Operating under synchronized or free run mode

- Two-frame receive elastic buffer with controlled slip direction indication

- Selectable transmit or receive jitter attenuator

- Intel or Motorola non-multiplexed parallel microprocessor interface

- CRC-4 updating algorithm for intermediate path points of a message-based data link application

- ST-BUS/GCI 2.048 Mbit/s backplane bus for both data and signalling

Ordering Information

MT9075BPR1   68 Pin PLCC*   Tape & Reel
MT9075BP1   68 Pin PLCC*   Tubes
MT9075BL1   100 Pin MQFP*   Trays
*Pb Free Matte Tin

-40°C to +85°C

Applications

- E1 add/drop multiplexers and channel banks

- CO and PBX equipment interfaces

- Primary Rate ISDN nodes

- Digital Cross-connect Systems (DCS)
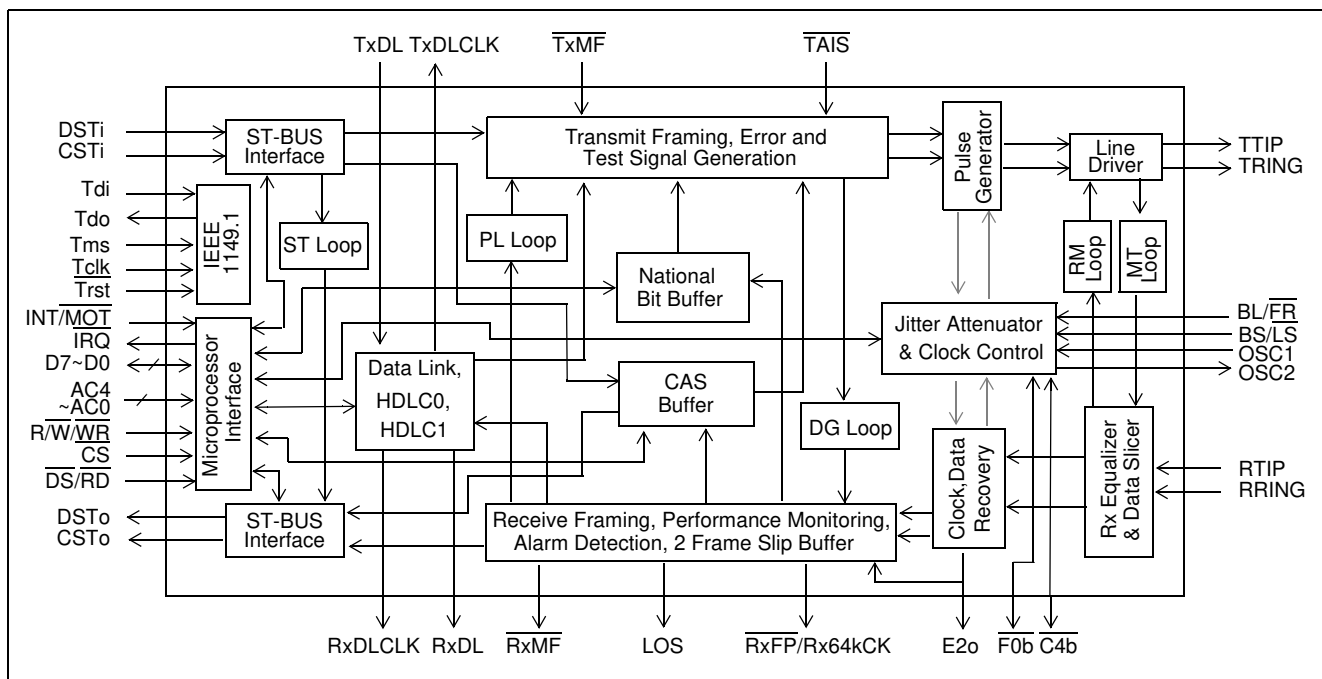
Figure 1 - Functional Block Diagram

Description

The MT9075B is a single chip device which integrates an advanced PCM 30 framer with a Line Interface Unit (LIU).

The framer interfaces to a 2.048 Mbit/s backplane and provides selectable rate data link access with optional HDLC controllers for S_a bits and channel 16. The LIU interfaces the framer functions to the PCM 30 transformer-isolated four wire line.

The MT9075B meets or supports the latest ITU-T Recommendations including G.703, G.704, G.706, G.732, G.775, G.796, G.823 for PCM 30, and I.431 for ISDN primary rate. It also meets or supports ETSI ETS 300 011, ETS 300 166 and ETS 300 233 as well as BS 6450.

Change Summary

Changes from the August 2005 issue to the August 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

68 PIN PLCC

Top row (pins 9–61):
DS/RD, DSTi, DSTo, CSTi, CSTo, VDD, VSS, OSC2, OSC1, VSS, VDD, BL/FR, TxDL, TxDLCK, IC, IC, LOS

Left column:
- CS — 10
- RESET — 11
- IRQ — 12
- D0 — 13
- D1 — 14
- D2 — 15
- D3 — 16
- VSS — 17
- IC — 18
- INT/MOT — 19
- VDD — 20
- D4 — 21
- D5 — 22
- D6 — 23
- D7 — 24
- R/W/WR — 25
- AC0 — 26

Right column:
- 60 — TAIS
- 59 — Trst
- 58 — Tclk
- 57 — Tms
- 56 — Tdo
- 55 — Tdi
- 54 — GNDATx
- 53 — TRING
- 52 — TTIP
- 51 — VDDATx
- 50 — VDD
- 49 — VSS
- 48 — IC
- 47 — RxFP/Rx64KCK
- 46 — F0b
- 45 — C4b
- 44 — E2o

Bottom row (pins 27–43):
AC1, AC2, AC3, AC4, GNDARx, RTIP, RRING, VDDARx, VDD, VSS, NC, NC, RxDCLK, RxDL, TxMF, RxMF, BS/LS

100 PIN MQFP (JEDEC MO-112)

Top row: NC, NC, NC, NC, NC, NC, DS/RD, DSTi, DSTo, CSTi, CSTo, VDD, VSS, OSC2, OSC1, VSS, VDD, BL/FR, TXDL, TCDLCK, IC, NC, IC, LOS, NC, NC, NC, NC, NC, NC (pins 80 ... 52 50)

Left column:
- NC — 80
- NC — 82
- CS
- RESET — 84
- IRQ
- D0 — 86
- D1
- D2 — 88
- D3
- VSS — 90
- IC
- INT/MOT — 92
- VDD
- D4 — 94
- D5
- D6 — 96
- D7
- R/W/WR — 98
- AC0
- NC — 100

Right column:
- NC — 50
- NC
- TAIS — 48
- Trst
- Tclk — 46
- Tms
- Tdo — 44
- Tdi
- GNDATx — 42
- TRING
- TTIP — 40
- VDDATx
- VDD — 38
- VSS
- IC — 36
- RxFP/Rx64KCK
- F0b — 34
- C4b
- E2o — 32
- NC

Bottom row (pins 2 ... 30): NC, NC, NC, NC, NC, NC, AC1, AC2, AC3, AC4, GNDARx, RTIP, RRING, VDARx, VDD, VSS, IC, IC, RXDLCK, RXDL, TxMF, RxMF, BS/LS, NC, NC, NC, NC, NC, NC

Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
PLCC	MQFP		
1	66	OSC1	**Oscillator Input.** This pin is either connected via a 20.000 MHz crystal to OSC2 where a crystal is used, or is directly driven when a 20.000 MHz oscillator is employed (see Figures 6 and 7). CMOS input switching level.
2	67	OSC2	**Oscillator Output.** Not suitable for driving other devices.
3	68	V_{SS}	**Negative Power Supply (Input).** Digital ground.
4	69	V_{DD}	**Positive Power Supply (Input).** Digital supply (+5V $\pm$ 5%).
5	70	CSTo	**Control ST-BUS Output.** CSTo carries one of the following two serial streams for CAS and CCS respectively: (i) A 2.048 Mbit/s ST-BUS status stream which contains the 30 receive signalling nibbles (ABCDZZZZ or ZZZZABCD). The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are tristated when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and tristated nibbles is reversed. (ii) A 64 kb/s output when the 64 KHz common channel signalling option is selected (page 01H, address 1AH, bit 0, 64KCCS =1) for channel 16.
6	71	CSTi	**Control ST-BUS Input.** CSTi carries one of the following two serial streams for CAS and CCS respectively: (i) A 2.048 Mbit/s ST-BUS control stream which contains the 30 transmit signalling nibbles (ABCDXXXX or XXXXABCD) when page 01H, address 1AH, bit 3, RPSIG=0. When RPSIG=1 this pin has no function. The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are ignored when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and ignored nibbles is reversed. (ii) A 64 kb/s input when the 64 KHz common channel signalling option is selected (page 01H, address 1AH, bit 0, 64KCCS =1) for channel 16.
7	72	DSTo	**Data ST-BUS Output.** A 2.048 Mbit/s serial stream which contains the 30 PCM or data channels received on the PCM 30 line.
8	73	DSTi	**Data ST-BUS Input.** A 2.048 Mbit/s serial stream which contains the 30 PCM or data channels to be transmitted on the PCM 30 line.
9	74	$\overline{DS}/\overline{RD}$	**Data/Read Strobe (Input).** In Motorola mode ($\overline{DS}$), this input is the active low data strobe of the microprocessor interface. In Intel mode ($\overline{RD}$), this input is the active low read strobe of the microprocessor interface.
10	83	$\overline{CS}$	**Chip Select (Input).** This active low input enables the non-multiplexed parallel microprocessor interface of the MT9075B. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
11	84	$\overline{RESET}$	**RESET (Input).** This active low input puts the MT9075B in a reset condition. $\overline{RESET}$ should be set to high for normal operation. The MT9075B should be reset after power-up. The $\overline{RESET}$ pin must be held low for a minimum of 1μsec. to reset the device properly.

Pin Description (continued)

Pin #		Name	Description
PLCC	**MQFP**		
12	85	$\overline{\text{IRQ}}$	**Interrupt Request (Output).** A low on this output pin indicates that an interrupt request is presented. $\overline{\text{IRQ}}$ is an open drain output that should be connected to V_{DD} through a pull-up resistor. An active low $\overline{\text{CS}}$ signal is not required for this pin to function.
13 - 16	86-89	D0 - D3	**Data 0 to Data 3 (Three-state I/O).** These signals combined with D4-D7 form the bidirectional data bus of the microprocessor interface (D0 is the least significant bit).
17	90	VSS	**Negative Power Supply (Input).** Digital ground.
18	91	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
19	92	INT/$\overline{\text{MOT}}$	**Intel/Motorola Mode Selection (Input).** A high on this pin configures the processor interface for the Intel parallel non-multiplexed bus type. A low configures the processor interface for the Motorola parallel non-multiplexed type.
20	93	VDD	**Positive Power Supply (Input).** Digital supply (+5V $\pm$ 5%).
21 - 24	94-97	D4 - D7	**Data 4 to Data 7 (Three-state I/O).** These signals combined with D0-D3 form the bidirectional data bus of the microprocessor interface (D7 is the most significant bit).
25	98	R/$\overline{\text{W}}$/$\overline{\text{WR}}$	**Read/Write/Write Strobe (Input).** In Motorola mode (R/$\overline{\text{W}}$), this input controls the direction of the data bus D[0:7] during a microprocessor access. When R/$\overline{\text{W}}$ is high, the parallel processor is reading data from the MT9075B. When low, the microprocessor is writing data to the MT9075B. For Intel mode ($\overline{\text{WR}}$), this active low write strobe configures the data bus lines as output.
26 - 30	99, 8-11	AC0 - AC4	**Address/Control 0 to 4 (Inputs).** Address and control inputs for the microprocessor interface. AC0 is the least significant input.
31	12	GNDARx	**Receive Analog Ground (Input).** Analog ground for the LIU receiver.
32 33	13 14	RTIP RRING	**Receive TIP and RING (Inputs).** Differential inputs for the receive line signal - must be transformer coupled (See Figure 4).
34	15	VDDARx	**Receive Analog Power Supply (Input).** Analog supply for the LIU receiver (+5V $\pm$ 5%).
35	16	VDD	**Positive Power Supply (Input).** Digital supply (+5V $\pm$ 5%).
36	17	VSS	**Negative Power Supply (Input).** Digital ground.
37	18	IC	**Internal Connection.** Must be left open for normal operation.
38	19	IC	**Internal Connection.** Must be left open for normal operation.
39	20	RxDLCLK	**Receive Data Link Clock (Output).** A gapped clock signal derived from a 2.048 Mbit/s clock, available for an external device to clock in RxDL data (at 4, 8, 12, 16 or 20 kHz) on the rising edge.
40	21	RxDL	**Receive Data Link (Output).** A 2.048 Mbit/s data stream containing received line data after HDB3 decoding. This data is clocked out with the rising edge of E2o.
41	22	$\overline{\text{TxMF}}$	**Transmit Multiframe Boundary (Input).** An active low input used to set the transmit multiframe boundary (CAS or CRC multiframe). The MT9075B will generate its own multiframe if this pin is held high. This input is usually pulled high for most applications.

Pin Description (continued)

Pin #		Name	Description
PLCC	MQFP		
42	23	$\overline{\text{RxMF}}$	**Receive Multiframe Boundary (Output).** An output pulse delimiting the received multiframe boundary. The next frame output on the data stream (DSTo) is basic frame zero on the PCM 30 link. This receive multiframe signal can be related to either the receive CRC multiframe (page 01H, address 10H, bit 6, MFSEL=1) or the receive signalling multiframe (MFSEL=0).
43	24	BS/$\overline{\text{LS}}$	**System Bus Synchronous/Line Synchronous Selection (Input).** If high, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be inputs; if low, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be outputs.
44	32	E2o	**2.048 MHz Extracted Clock (Output).** The clock extracted from the received signal and used internally to clock in data received on RTIP and RRING.
45	33	$\overline{\text{C4b}}$	**4.096 MHz System Clock (Input/Output).** $\overline{\text{C4b}}$ is the clock for the ST-BUS sections and transmit serial PCM data of the MT9075B. In the free-run (BL/$\overline{\text{FR}}$=0) or line synchronous mode (BL/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in the system bus synchronous mode (BS/$\overline{\text{LS}}$=1) this signal is an input clock.
46	34	$\overline{\text{F0b}}$	**Frame Pulse (Input/Output).** This is the ST-BUS or GCI frame synchronization signal, which delimits the 32 channel frame of CSTi, CSTo, DSTi, DSTo and the PCM30 link. In the free-run (BL/$\overline{\text{FR}}$=0) or loop synchronous mode (BL/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in the Bus Synchronous mode (BL/$\overline{\text{FR}}$=1 and BS/$\overline{\text{LS}}$=0) this signal is an input. The GCI/ST-BUS selection is made under software control. Page 02H, address 13H, bit 0, GCI/$\overline{\text{ST}}$=1 selects GCI frame pulse; GCI/$\overline{\text{ST}}$=0 selects ST-BUS.
47	35	$\overline{\text{RxFP}}$/Rx64KCK	**Receive Frame Pulse/Receive CCS Clock (Output).** An 8 kHz pulse signal, which is low for one extracted clock period. This signal is synchronized to the receive PCM 30 basic frame boundary. When 64KCCS (page 01H, address 1AH, bit 0) is set to 1, this pin outputs a 64 kHz clock derived by dividing down the extracted 2.048 MHz clock. This clock is used to clock CCS data out of pin CSTo in the CCS mode.
48	36	IC	**Internal Connection.** Must be left open for normal operation.
49	37	V_{SS}	**Negative Power Supply (Input).** Digital ground.
50	38	V_{DD}	**Positive Power Supply (Input).** Digital supply (+5V $\pm$ 5%).
51	39	VDD_{ATx}	**Transmit Analog Power Supply (Input).** Analog supply for the LIU transmitter (+5V $\pm$ 5%).
52 53	40 41	TTIP TRING	**Transmit TIP and RING (Outputs).** Differential outputs for the transmit line signal - must be transformer coupled (See Figure 4).
54	42	GND_{ATx}	**Transmit Analog Ground (Input).** Analog ground for the LIU transmitter.
55	43	Tdi	**IEEE 1149.1 Test Data Input.** If not used, this pin should be pulled high.
56	44	Tdo	**IEEE 1149.1 Test Data Output.** If not used, this pin should be left unconnected.
57	45	Tms	**IEEE 1149.1 Test Mode Selection (Input).** If not used, this pin should be pulled high.
58	46	Tclk	**IEEE 1149.1 Test Clock Signal (Input).** If not used, this pin should be pulled high.
59	47	$\overline{\text{Trst}}$	**IEEE 1149.1 Reset Signal (Input).** If not used, this pin should be held low.

Pin Description (continued)

Pin #		Name	Description
PLCC	**MQFP**		
60	48	$\overline{\text{TAIS}}$	**Transmit Alarm Indication Signal (Input).** An active low on this input causes the MT9075B to transmit an AIS (all ones signal) on TTIP and TRING pins. $\overline{\text{TAIS}}$ should be set to high for normal data transmission.
61	57	LOS	**Loss of Signal or Synchronization (Output).** When high, and LOS/LOF (page 02H address 13H bit 2) is zero, this signal indicates that the receive portion of the MT9075B is either not detecting an incoming signal (bit LLOS on page 03H address 18H is one) or is detecting a loss of basic frame alignment condition (bit $\overline{\text{SYNC}}$ on page 03H address 10H is one). If LOS/LOF=1, a high on this pin indicates a loss of signal condition.
62	58	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
	59	NC	**No Connection.** Leave open for normal operation.
63	60	IC	**Internal Connection.** Tie to V_{SS} (Ground) for normal operation.
64	61	TxDLCLK	**Transmit Data Link Clock (Output).** A gapped clock signal derived from a gated 2.048 Mbit/s clock for transmit data link at 4, 8, 12, 16 or 20 kHz. The transmit data link data (TxDL) is clocked in on the rising edge of TxDLCLK. TxDLCLK can also be used to clock DL data out of an external serial controller.
65	62	TxDL	**Transmit Data Link (Input).** An input serial stream of transmit data link data at 4, 8, 12, 16 or 20 kbit/s composed of 488ns-wide bit cells which are multiplexed into selected national bits of the PCM 30 transmit signal.
66	63	BL/$\overline{\text{FR}}$	**Bus or Line/Freerun (Input).** If this pin is set to high, the MT9075B is in the System Bus or Line Synchronous mode depending on the BS/$\overline{\text{LS}}$ pin. If low, the MT9075B is in the free run mode.
67	64	VDD	**Positive Power Supply (Input).** Digital supply (+5V ± 5%).
68	65	VSS	**Negative Power Supply (Input).** Digital ground.
	1-7, 25-31, 49-56, 75-82, 100	NC	**No Connection.** Leave open for normal operation.

Device Overview

The MT9075B is an advanced PCM 30 framer with an on-chip Line Interface Unit (LIU) that meets or supports the latest ITU-T Recommendations for PCM 30 and ISDN primary rate including G.703, G.704, G.706, G.775, G.796, G.732, G.823 and I.431. It also meets or supports the layer 1 requirements of ETSI ETS 300 011, ETS 300 166, ETS 300 233 and BS6450.

The Line Interface Unit (LIU) of the MT9075B interfaces the digital framer functions to the PCM 30 transformer-isolated four wire line. The transmit portion of the MT9075B LIU consists of a digital buffer, a digital-to-analog converter and a differential line driver. The receiver portion of the LIU consists of an input signal peak detector, an optional two-stage equalizer, a smoothing filter, data and clock slicers and a clock extractor. The optional equalizer allows for error free reception of data with a line attenuation of up to 20 dB.

The LIU also contains a Jitter Attenuator (JA), which can be configured to either the transmit or receive path. The JA will attenuate jitter from 2.5 Hz and roll-off at a rate of 20 dB/decade. Its intrinsic jitter is less than 0.02 UI.

The digital portion of the MT9075B connects an incoming stream of time multiplexed PCM channels (at 2.048 Mbit/s) to the transmit payload of the E1 trunk, while the receive payload is connected to the ST-BUS or GCI 2.048 Mbit/s backplane bus for both data and signalling. Control, reporting and conditioning of the line is implemented via a parallel microprocessor interface. The MT9075B framing algorithm allows automatic interworking between CRC-4 and non-CRC-4 interfaces.

The S_a bits can be accessed by the MT9075B in the following four ways:

• Single byte registers;

• Five byte transmit and receive national bit buffers;

• Data link pins TxDL, RxDL, RxDLCLK and TxDLCLK;

• HDLC Controller with a 128 byte FIFO.

The MT9075B operates in either termination or transparent modes selectable via software control. In the termination mode the CRC-4 calculation is performed as part of the framing algorithm. In the transmit transparent mode, no framing or signalling is imposed on the data transmit from DSTi on the line. In addition, the MT9075B optionally allows the data link maintenance channel to be modified and updates the CRC-4 remainder bits to reflect the modification. All channel, framing and signalling data passes through the device unaltered. This is useful for intermediate point applications of a PCM 30 link where the data link data is modified, but the error information transported by the CRC-4 bits must be passed to the terminating end. In the receive transparent mode, the received line data is channelled to DSTo with framing operations disabled, consequently, the data passes through the slip buffer and drives DSTo with an arbitrary alignment.

The MT9075B has a comprehensive suite of status, alarm, performance monitoring and reporting features. These include counters for BPVs, CRC errors, E-bit errors, errored frame alignment signals, BERT, and RAI and continuous CRC errors. Also, included are transmission error insertion for BPVs, CRC-4 errors, frame and non-frame alignment signal errors, payload errors and loss of signal errors.

A complete set of loopback functions is provided, which includes digital, remote, ST-BUS, payload, metallic, local and remote time slot.

The MT9075B also contains a comprehensive set of maskable interrupts and an interrupt vector function. Interrupt sources consist of synchronization status, alarm status, counter indication and overflow, timer status, slip indication, maintenance functions and receive channel associated signalling bit changes. A special set of maskable interrupts have been included for sensing changes in the state of the national use bits and nibbles, in compliance to emerging ETS requirements.

The MT9075B system timing may be slaved to the line, operated in freerun mode, or controlled by an external timing source.

Functional Description

MT9075B Line Interface Unit (LIU)

Receiver

The receiver portion of the MT9075B LIU consists of an input signal peak detector, an optional two-stage equalizer, a smoothing filter, adaptive threshold comparators, data and clock slicers, and a clock extractor. Receive equalization gain can be set via software control or it can be determined automatically by the peak detectors.

The output of the receive equalizer is conditioned by a smoothing filter and is passed on to the clock and data slicer. The clock slicer output signal drives a phase locked loop, which generates the extracted clock (E2o). This extracted clock is used to sample the output of the data comparator.

The LOS output pin (pin 61 in PLCC, pin 57 in MQFP) is user selectable, by setting control bit LOS/LOF (page 02H, register 13H, bit 2), to indicate a loss of signal or loss of basic frame synchronization condition. In addition, a status

bit, LLOS (bit 4 in page 3, register 18H) is provided to indicate the presence of a loss signal condition. The occurrence of a loss signal condition is defined as per I.431, i.e., when the incoming signal amplitude is more than 20 dB below the nominal amplitude for a time duration of at least 1 ms.

The receive LIU circuit requires a terminating resistor of either 120 Ω or 75 Ω across the device side of the receive1:1 transformer as shown in Figure 4. The return loss of the receiver, complying with G.703, is greater than:

• 12 dB from 51 kHz to 102 kHz;

• 18 dB from 102 kHz to 2048 kHz;

• 14 dB from 2048 kHz to 3072 kHz.

The jitter tolerance of the MT9075B clock extractor circuit exceeds the requirements of G.823 (Figure 3).

Transmitter

The MT9075B differential line driver is designed to drive a 1:2 step-up transformer (see Figure 4). A 0.68 uF capacitor is required between the TTIP and the transmit transformer. Resistors R_T (as shown in Figure 4) are for termination for transmit return loss. The values of R_T may be optimized for 120 Ω lines, 75 Ω lines or set at an intermediary value to serve both applications. Program the Transmit Pulse Control Word (address 1FH page 1) to adjust the pulse amplitude accordingly. Alternatively, the pulse level and shape may be discretely programmed by writing to the Customer Pulse Level registers (addresses 1CH to 1FH, page 2) and setting the Custom Transmit Pulse bit high (bit 3 of the Transmit Pulse Control Word).
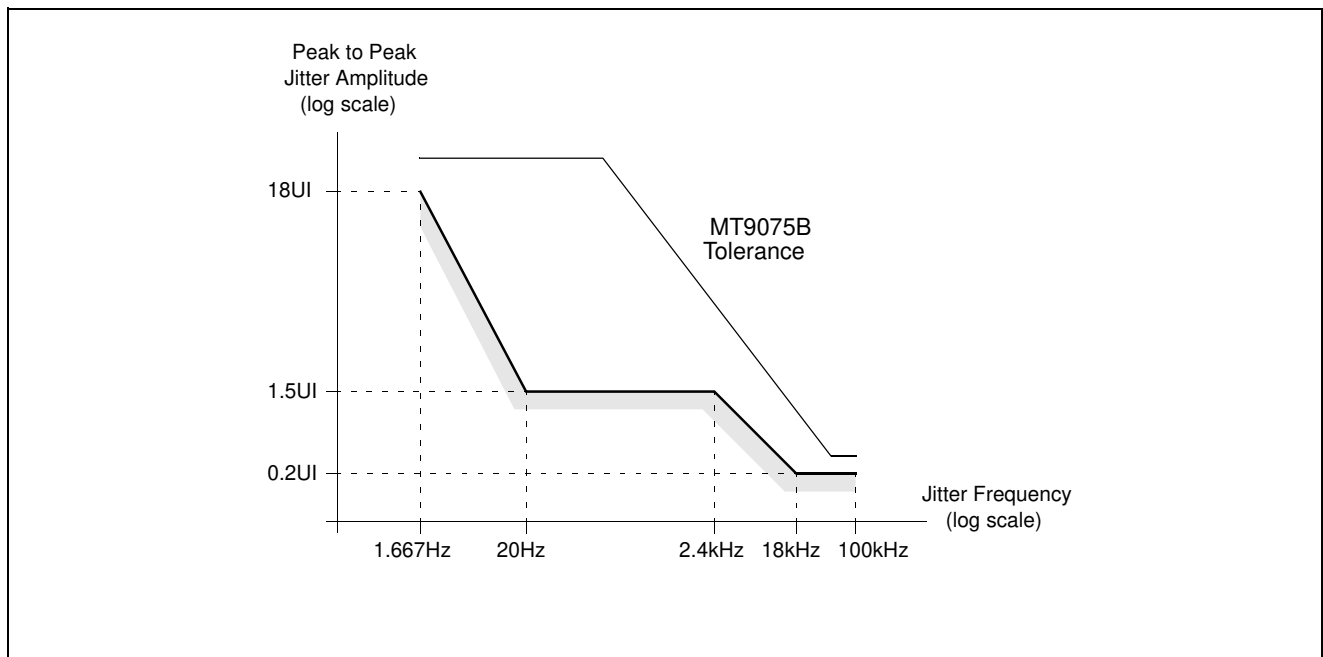

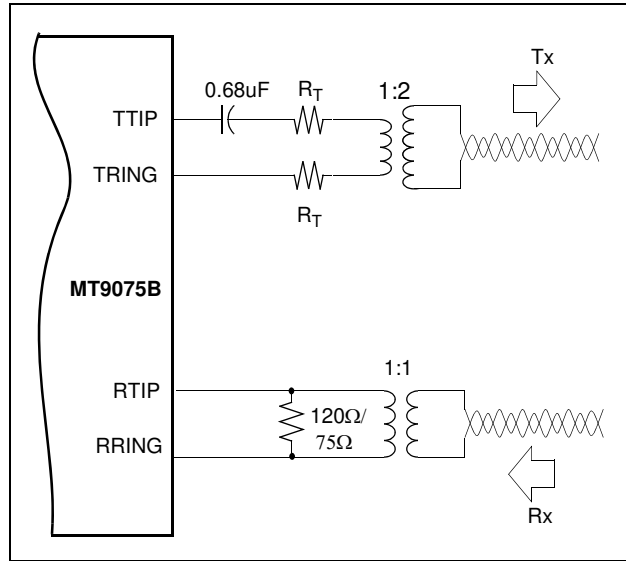
Figure 3 - Typical Jitter Tolerance

Figure 4 - Analog Line Interface

The template for the transmitted pulse, as specified in G703, is shown in Figure 5. The nominal peak voltage of a mark is 3 volts for 120 Ω twisted pair applications and 2.37 volts for 75 Ω coax applications. The ratio of the amplitude of the transmit pulses generated by TTP and TRING is between 0.95 and 1.05.
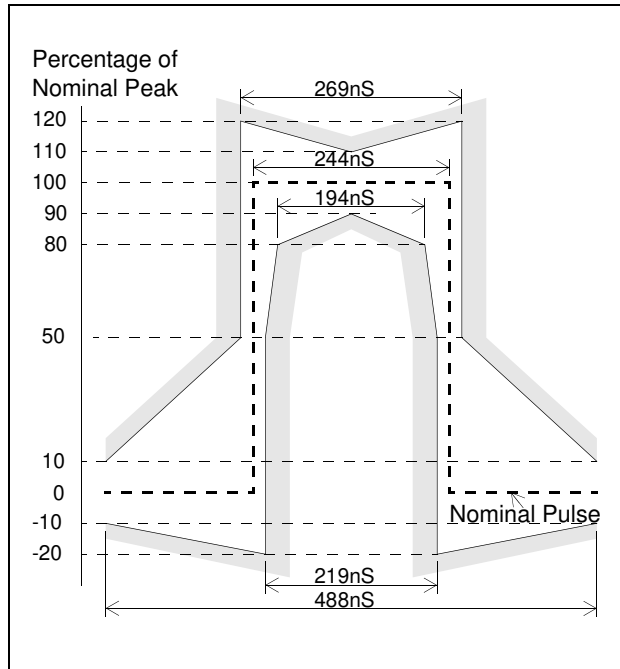

Figure 5 - Pulse Template (G.703)

Zarlink Semiconductor Inc.

Transformer Recommendation

Table 1 shows a list of recommended transformers for the MT9075B line interface.

Manufacturer	For Tx	For Rx
Filtran	5721-1	5721-2
Pulse Engineering	PE-65351	PE-64934
Midcom	50027	50026
OSEC	02934/A	02935/A

Table 1 - Transformer Manufacturers and Part Numbers

Timing Source

The MT9075B can use either a clock or crystal, connecting to pins OSC1 and OSC2, as the reference timing source.

Figure 6 shows a 20 MHz clock oscillator, with 50 ppm tolerance, directly connected to the OSC1 pin of the MT9075B.
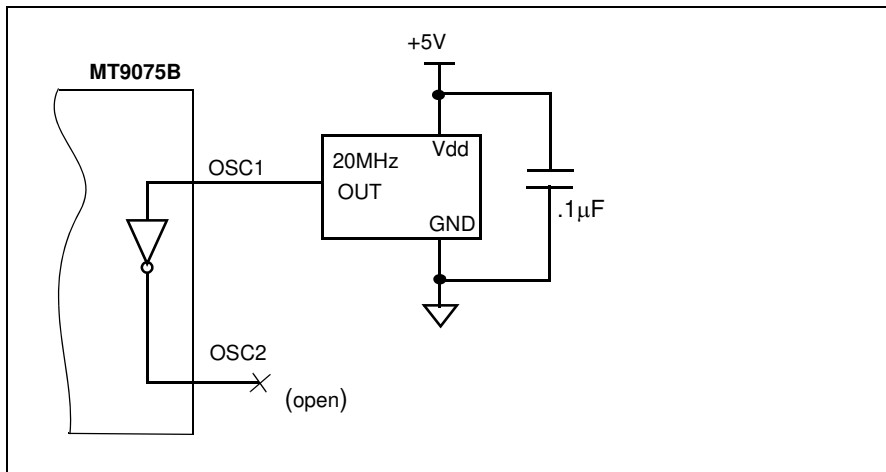
Figure 6 - Clock Oscillator Circuit

Alternatively, a crystal oscillator may be used. A complete oscillator circuit made up of a crystal, resistors and capacitors is shown in Figure 7. The crystal specification is as follows.

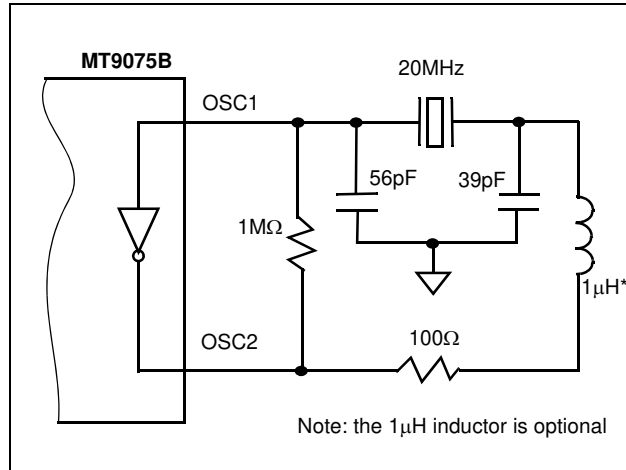|	
Frequency:	*20 MHz*
Tolerance:	*50 ppm*
Oscillation Mode:	*Fundamental*
Resonance Mode:	*Parallel*
Load Capacitance:	*32 pF*
Maximum Series Resistance:	*35 Ω*
Approximate Drive Level:	*1 mW*

Figure 7 - Crystal Oscillator Circuit

Jitter Attenuator (JA)

The MT9075B Jitter Attenuator (JA), which consists of a Phase Locked Loop (PLL) and data FIFO, can be used on either the transmit or receive side of the interface.

On the transmit side the $\overline{C4b}$ signal clocks the data into the FIFO, the PLL de-jitters the $\overline{C4b}$ clock and the resulting clean $\overline{C4b}$ signal clocks the data out of the FIFO.

When the JA is selected on the receive side, the extracted clock signal clocks the data into the FIFO. The same clock feeds the PLL and the resulting de-jittered clock is used to clock the data out of the FIFO.

The JA meets the jitter transfer characteristics as proposed by G.823 and the relevant recommendations as shown in Figure 8. The JA FIFO depth can be selected to be from 16 to 128 words deep, in multiples of 16 (2-bit) words. Its read pointer can be centered by changing the JFC bit (address 18H of page 02H) to provide maximum jitter tolerance. If the read pointer should come within 4 bits of either end of the FIFO, the read clock frequency will be increased or decreased by 0.0625 UI to correct the situation. The maximum time needed to centre is $T_{max}= 3904*Depth$ ns, where Depth is the selected JA FIFO depth. During this time the JA will not attenuate jitter.

To ensure normal operation, the JA FIFO depth should be set in software to be larger than the anticipated maximum UI of input jitter.

Clock Jitter Attenuation Modes

MT9075B has three basic jitter attenuation modes of operation, selected by the BS/$\overline{LS}$ and BL/$\overline{FR}$ control pins.

- System Bus Synchronous Mode
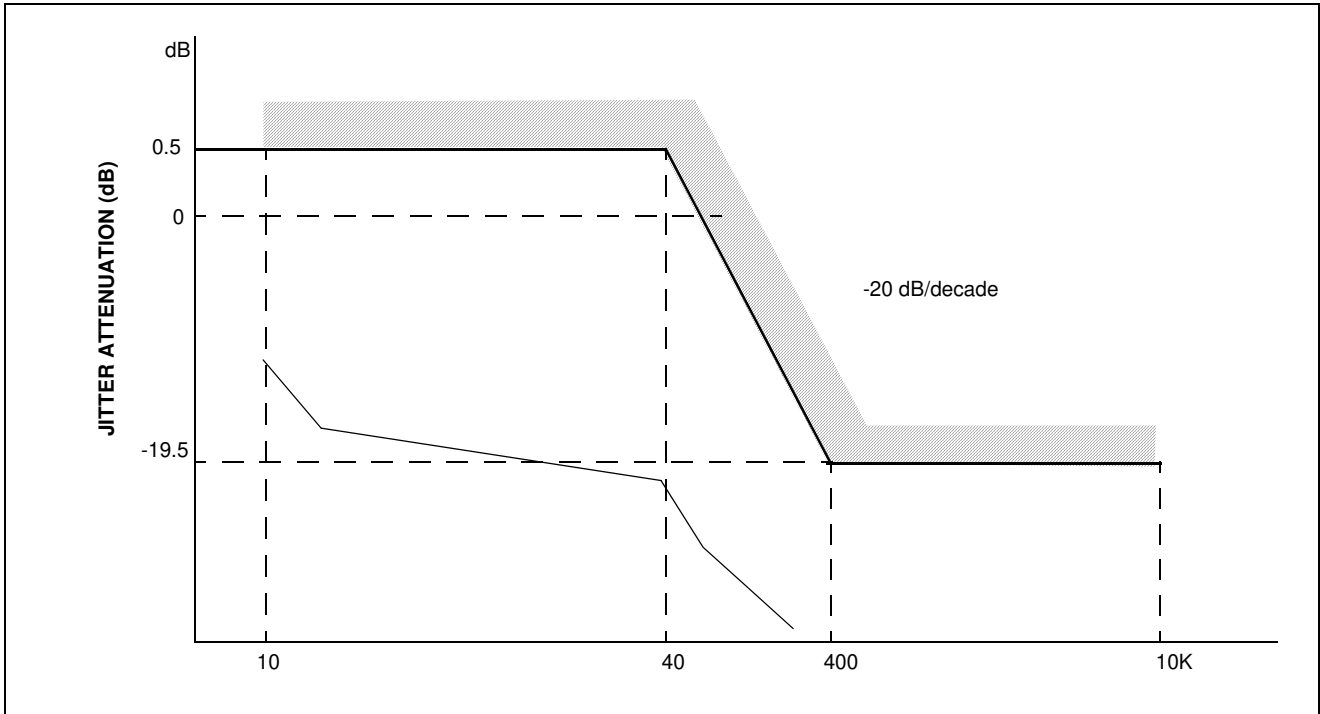- Line Synchronous Mode
- Free-run mode

Figure 8 - Typical Jitter Attenuation Curve

Mode Name	BS/$\overline{\text{LS}}$	BL/$\overline{\text{FR}}$	JAS	JAT/$\overline{\text{JAR}}$	Note
SysBusSync1	1	1	1	1	JA on Tx side; No JA on Rx side
SysBusSync2	1	1	1	0	JA on Rx side; No JA on Tx side
SysBusSync3	1	1	0	x	No JA on Tx or Rx side
Line Synchronous	0	1	x	x	By default, JA is on the receive side. Controls bits need not be selected.
Free-Run	x	0	x	x	In free-run mode JA will be automatically disconnected

Table 2 - Selection of Clock Jitter Attenuation Modes

Depending on the mode selected, the Jitter Attenuator (JA) can attenuate either transmit clock jitter or receive clock jitter, or be disconnected. Control bits JAS, JAT/$\overline{\text{JAR}}$ (address 18H of page 02H) determine the JA selection under certain modes. Table 2 shows the configuration of related control pins and control bits required to place the MT9075B in the appropriate jitter attenuation mode.

Referring to the mode names given in Table 2, the basic operation of the jitter attenuation modes is summarized as follows:

- In *SysBusSync* (1-3) modes, pins $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ are always configured as inputs, while in the Line Synchronous and Free-Run modes C4b and F0b are configured as outputs.

- In *SysBusSync1* mode, an external clock is applied to $\overline{\text{C4b}}$. The applied clock is dejittered by the internal PLL before being used to transmit data. The clock extracted (with no jitter attenuation performed) from the receive data can be monitored on pin E2o.

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- In *SysBusSync2* mode, the clock applied to pin $\overline{C4b}$ is assumed to be jitter-free and is directly used to transmit data. The internal PLL is used to dejitter the extracted receive clock. The dejittered receive clock is output on pin E2o.

- In *SysBusSync3* mode, no jitter attenuation is applied to either the transmit or receive clocks. The transmit data is synchronized to clock applied to pin C4b. The extracted receive clock is not dejittered and is supplied directly to the E2o output.

- In *Line Synchronous* mode, the clock extracted from the receive data is dejittered using the internal PLL and then output on pin C4b. Pin E2o provides the extracted receive clock before it has been dejittered. The transmit data is synchronous to the clean receive clock.

- In *Free-Run* mode the transmit data is synchronized to the internally generated clock. The internal clock is output on pin C4b. The clock signal extracted from the receive data is not dejittered and is output directly on pin E2o.

The PCM 30 Interface

PCM 30 (E1) basic frames are 256 bits long and are transmitted at a frame repetition rate of 8000 Hz, which results in an aggregate bit rate of 256 bits x 8000/sec = 2.048 Mbits/sec. The actual bit rate is 2.048 Mbits/sec +/-50 ppm encoded in HDB3 format. The HDB3 control bit (page 01H, address 15H, bit 5) selects either HDB3 encoding or alternate mark inversion (AMI) encoding. Basic frames are divided into 32 time slots numbered 0 to 31, see Figure 30. Each time slot is 8 bits in length and is transmitted most significant bit first (numbered bit 1). This results in a single time slot data rate of 8 bits x 8000/sec. = 64 kbits/sec.

It should be noted that the Zarlink ST-BUS also has 32 channels numbered 0 to 31, but the most significant bit of an eight bit channel is numbered bit 7 (see Zarlink Application Note MSAN-126). Therefore, ST-BUS bit 7 is synonymous with PCM 30 bit 1; bit 6 with bit 2: and so on (Figure 31).

PCM 30 time slot 0 is reserved for basic frame alignment, CRC-4 multiframe alignment and the communication of maintenance information. In most configurations time slot 16 is reserved for either Channel Associated Signalling (CAS or ABCD bit signalling) or Common Channel Signalling (CCS). The remaining 30 time slots are called channels and carry either PCM encoded voice signals or digital data. Channel alignment and bit numbering is consistent with time slot alignment and bit numbering. However, channels are numbered 1 to 30 and relate to time slots as per Table 3.

PCM 30 Timeslot	0	1 2 3...15	16	17 18 19...31
Voice/Data Channels	x	1 2 3...15	x	16 17 18...30

Table 3 - Time Slot to Channel Relationship

Basic Frame Alignment

Time slot 0 of every basic frame is reserved for basic frame alignment and contains either a Frame Alignment Signal (FAS) or a Non-Frame Alignment Signal (NFAS). FAS and NFAS occur in time slot zero of consecutive basic frames as shown in Table 7. Bit two is used to distinguish between FAS (bit two = 0) and NFAS (bit two = 1).

Basic frame alignment is initiated by a search for the bit sequence 0011011 which appears in the last seven bit positions of the FAS, see the Frame Algorithm section. Bit position one of the FAS can be either a CRC-4 remainder bit or an international usage bit.

Bits four to eight of the NFAS (i.e., S_{a4} - S_{a8}) are additional spare bits which may be used as follows:

- S_{a4} to S_{a8} may be used in specific point-to-point applications (e.g. transcoder equipments conforming to G.761).

- S_{a4} may be used as a message-based data link for operations, maintenance and performance monitoring.

- S_{a5} to S_{a8} are for national usage.

A maintenance channel or data link at 4,8,12,16,or 20 kHz for selected S_a bits is provided by the MT9075B to implement these functions. Note that for simplicity all S_a bits including S_{a4} are collectively called national bits throughout this document.

Bit three (designated as "A"), the Remote Alarm Indication (RAI), is used to indicate the near end basic frame synchronization status to the far end of a link. Under normal operation, the A (RAI) bit should be set to 0, while in alarm condition, it is set to 1.

Bit position one of the NFAS can be either a CRC-4 multiframe alignment signal, an E-bit or an international usage bit. Refer to an approvals laboratory and national standards bodies for specific requirements.

CRC-4 Multiframing

The primary purpose for CRC-4 multiframing is to provide a verification of the current basic frame alignment, although it can also be used for other functions such as bit error rate estimation. The CRC-4 multiframe consists of 16 basic frames numbered 0 to 15, and has a repetition rate of 16 frames X 125 microseconds/frame = 2 msec.

CRC-4 multiframe alignment is based on the 001011 bit sequence, which appears in bit position one of the first six NFASs of a CRC-4 multiframe.

The CRC-4 multiframe is divided into two submultiframes, numbered 1 and 2, which are each eight basic frames or 2048 bits in length.

The CRC-4 frame alignment verification functions as follows. Initially, the CRC-4 operation must be activated and CRC-4 multiframe alignment must be achieved at both ends of the link. At the local end of a link, all the bits of every transmit submultiframe are passed through a CRC-4 polynomial (multiplied by X^4 then divided by $X^4 + X + 1$), which generates a four bit remainder. This remainder is inserted in bit position one of the four FASs of the following submultiframe before it is transmitted (see Table 7).

The submultiframe is then transmitted and, at the far end, the same process occurs. That is, a CRC-4 remainder is generated for each received submultiframe. These bits are compared with the bits received in position one of the four FASs of the next received submultiframe. This process takes place in both directions of transmission.

When more than 914 CRC-4 errors (out of a possible 1000) are counted in a one second interval, the framing algorithm will force a search for a new basic frame alignment. See Frame Algorithm section for more details.

The result of the comparison of the received CRC-4 remainder with the locally generated remainder will be transported to the far end by the E-bits. Therefore, if $E_1 = 0$, a CRC-4 error was discovered in a submultiframe 1 received at the far end; and if $E_2 = 0$, a CRC-4 error was discovered in a submultiframe 2 received at the far end. No submultiframe sequence numbers or re-transmission capabilities are supported with layer 1 PCM 30 protocol. See ITU-T G.704 and G.706 for more details on the operation of CRC-4 and E-bits.

There are two CRC multiframe alignment algorithm options selected by the $\overline{\text{AUTC}}$ control bit (address 11H, page 01H). When $\overline{\text{AUTC}}$ is zero and $\overline{\text{CSYN}}$ is zero, automatic CRC-to-non-CRC interworking is selected, if CRC-4 multiframe alignment is not found in 400 msec, the status bit CRCIWK (page 03H, address 10H) is set low and no further attempt to achieve CRC-4 synchronization is made as long as the device remains in terminal frame synchronization. When $\overline{\text{AUTC}}$ is one and $\overline{\text{CSYN}}$ is zero, a reframe will be initiated every 8 msec if the MT9075B achieves terminal frame synchronization, but fails to achieve CRC-4 synchronization. In this case, if $\overline{\text{ARAI}}$ is low, RAI will flicker high with every reframe. If CRC MFAI is unsuccessful after 400ms, RAI will stay high continuously.

The control bit for transmit E bits (TE, bit 4 at address 16H of page 01H) will have the same function in both states of $\overline{\text{AUTC}}$. That is, when CRC-4 synchronization is not achieved the state of the transmit E-bits will be the same as the state of the TE control bit. When CRC-4 synchronization is achieved the transmit E-bits will function as per ITU-T G.704. Table 4 outlines the operation of the $\overline{\text{AUTC}}$, $\overline{\text{ARAI}}$ and TALM control bits of the MT9075B.

AUTC	ARAI	TALM	Description
0	0	x	Automatic CRC-interworking is activated. If no valid CRC MFAS is being received, transmit RAI will flicker high with every reframe (8 msec.), this cycle will continue for 400 msec., then transmit RAI will be low continuously. The device will stop searching for CRC MFAS, continue to transmit CRC-4 remainders, stop CRC-4 processing indicate CRC-to-non-CRC operation and transmit E-bits to be the same state as the TE control bit (page 01H, address 16H).
0	1	0	Automatic CRC-interworking is activated. Transmit RAI is low continuously upon loss of synchronization.
0	1	1	Automatic CRC-interworking is activated. Transmit RAI is high continuously upon loss of synchronization.
1	0	x	Automatic CRC-interworking is de-activated. If no valid CRC MFAS is being received, transmit RAI flickers high with every reframe (8 msec.), this cycle continues for 400 msec., then transmit RAI becomes high continuously. The device continues to search for CRC MFAS and transmit E-bits are the same state as the TE control bit. When $\overline{CRCSYN}$ = 0, the CRC MFAS search is terminated and the transmit RAI goes low.
1	1	0	Automatic CRC-interworking is de-activated. Transmit RAI is low continuously upon loss of synchronization.
1	1	1	Automatic CRC-interworking is de-activated. Transmit RAI is high continuously upon loss of synchronization.

Table 4 - Operation of $\overline{\text{AUTC}}$, $\overline{\text{ARAI}}$ and TALM Control Bits

CAS Signalling Multiframing

The purpose of the signalling multiframing algorithm is to provide a scheme that will allow the association of a specific ABCD signalling nibble with the appropriate PCM 30 channel. Time slot 16 is reserved for the communication of Channel Associated Signalling (CAS) information (i.e., ABCD signalling bits for up to 30 channels). Refer to ITU-T G.704 and G.732 for more details on CAS multiframing requirements.

A CAS signalling multiframe consists of 16 basic frames (numbered 0 to 15), which results in a multiframe repetition rate of 2 msec. It should be noted that the boundaries of the signalling multiframe may be completely distinct from those of the CRC-4 multiframe. CAS multiframe alignment is based on a multiframe alignment signal (a 0000 bit sequence), which occurs in the most significant nibble of time slot 16 of basic frame 0 of the CAS multiframe. Bit 6 of this time slot is the multiframe alarm bit (usually designated Y). When CAS multiframing is acquired on the receive side, the transmit Y-bit is zero; when CAS multiframing is not acquired, the transmit Y-bit is one. Bits 5, 7 and 8 (usually designated X) are spare bits and are normally set to one if not used.

Time slot 16 of the remaining 15 basic frames of the CAS multiframe (i.e., basic frames 1 to 15) are reserved for the ABCD signalling bits for the 30 payload channels. The most significant nibbles are reserved for channels 1 to 15 and the least significant nibbles are reserved for channels 16 to 30. That is, time slot 16 of basic frame 1 has ABCD for channel 1 and 16, time slot 16 of basic frame 2 has ABCD for channel 2 and 17, through to time slot 16 of basic frame 15 has ABCD for channel 15 and 30.

MT9075B Access and Control

Register Access

The control and status of the MT9075B is achieved through a non-multiplexed parallel microprocessor port. The parallel port may be configured for Motorola style control signals (by setting pin INT/$\overline{\text{MOT}}$ low) or Intel style control signals (by setting pin INT/$\overline{\text{MOT}}$ high).

The controlling microprocessor gains access to specific registers of the MT9075B through a two step process. First, writing to the internal Command/Address Register (CAR) selects one of the 18 pages of control and status registers (CAR address: AC4 = 0, AC3-AC0 = don't care, CAR data D7 - D0 = page number). Second, each page has a maximum of 16 registers that are addressed on a read or write to a non-CAR address (non-CAR: address AC4 = 1, AC3-AC0 = register address, D7-D0 = data). Once a page of memory is selected, it is only necessary to write to the CAR when a different page is to be accessed. See Figures 11 and 12 for timing requirements.

Please note that for microprocessors with read/write cycles less than 200 ns, a wait state or a dummy operation (for C programming) between two successive read/write operations to the HDLC FIFO is required.

Table 5 associates the MT9075B control and status pages with access and page descriptions.

Page Address D$_7$ - D$_0$	Register Description	Processor Access	ST-BUS Access
00000001 (01H)	Master	R/W	
00000010 (02H)	Control	R/W	--
00000011 (03H)	Master	R	
00000100 (04H)	Status	R/W	---
00000101 (05H)	Per Channel Transmit Signalling	R/W	CSTi
00000110 (06H)	Per Channel Receive Signalling	R	CSTo
00000111 (07H)	Per Time Slot	R/W	
00001000 (08H)	Control	R/W	---
00001001 (09H)	1 Second Status	R	---
00001010 (0AH)	unused		---
00001011 (0BH)	HDLC0 Control and Status (TS 0)	R/W	---
00001100 (0CH)	HDLC1 Control and Status (TS 16)	R/W	---
00001101 (0DH)	Transmit National Bit Buffer	R/W	---
00001110 (0EH)	Receive National Bit Buffer	R	---
00001111 (0FH)	Tx message mode Buffer 0	R/W	---
00010000 (10H)	Tx message mode Buffer 1	R/W	---
00010001 (11H)	Rx message mode Buffer 0	R/W	---
00010010 (12H)	Rx message mode Buffer 1	R/W	---

Table 5 - Register Summary

ST-BUS Streams

The ST-BUS stream can also be used to access channel associated signalling nibbles. CSTo contains the received channel associated signalling bits (e.g., ITU-T R1 and R2 signalling), and when control bit RPSIG (page 01H, address 1AH) is set to 0, CSTi is used to control the transmit channel associated signalling. The DSTi and DSTo streams contain the transmit and receive voice and digital data.

Identification Code

The MT9075B shall be identified by the code 10101010, read from the identification code status register (page 03H, address 1FH).

Reset Operation (Initialization)

The MT9075B can be reset using the hardware $\overline{\text{RESET}}$ pin (pin 11 in PLCC, pin 84 in MQFP, see pin description for external reset circuit requirements) or the software reset bit RST (page 01H, address 11H). When the device emerges from its reset state it will begin to function with the default settings described in Table 6. A reset operation takes 1 full frame (125 us) to complete.

Function	Status
Mode	Termination
Loopbacks	Deactivated
Transmit FAS	C_n0011011
Transmit non-FAS	1/S_n1111111
Transmit MFAS (CAS)	00001111
Data Link	Deactivated
CRC Interworking	Activated
Signalling	CAS Registers
ABCD Bit Debounce	Deactivated
Interrupts	Interrupt Mask Word Zero unmasked, all others masked; interrupts not suspended
RxMF Output	Signalling Multiframe
Error Insertion	Deactivated
HDLCs	Deactivated
Counters	Cleared
Tx Message Buffer	All locations set to 54H
Per Time Slot Control Buffer	All locations cleared

Table 6 - Reset Status

Transmit AIS Operation

The pin $\overline{\text{TAIS}}$ (Transmit AIS, pin 60 in PLCC, pin 48 in MQFP) allows an all ones signal to be transmitted from the point of power-up without the need to write any control registers. During this time the $\overline{\text{IRQ}}$ pin is tristated. After the interface has been initialized normal operation can take place by making $\overline{\text{TAIS}}$ high.

National Bit Buffers

Table 7 shows the contents of the transmit and receive Frame Alignment Signals (FAS) and Non-frame Alignment Signals (NFAS) of time slot zero of a PCM 30 signal. Even numbered frames (CRC Frame # 0, 2, 4,...) are FASs and odd numbered frames (CRC Frame # 1, 3, 5,...) are NFASs. The bits of each channel are numbered 1 to 8, with bit 1 being the most significant and bit 8 the least significant.

CRC	CRC Frame/Type	PCM 30 Channel Zero							
		1	2	3	4	5	6	7	8
Sub Multi Frame 1	0/FAS	C_1	0	0	1	1	0	1	1
	1/NFAS	0	1	A	S a4	S a5	S a6	S a7	S a8
	2/FAS	C_2	0	0	1	1	0	1	1
	3/NFAS	0	1	A	S a4	S a5	S a6	S a7	S a8
	4/FAS	C_3	0	0	1	1	0	1	1
	5/NFAS	1	1	A	S a4	S a5	S a6	S a7	S a8
	6/FAS	C_4	0	0	1	1	0	1	1
	7/NFAS	0	1	A	S a4	S a5	S a6	S a7	S a8
Sub Multi Frame 2	8/FAS	C_1	0	0	1	1	0	1	1
	9/NFAS	1	1	A	S a4	S a5	S a6	S a7	S a8
	10/FAS	C_2	0	0	1	1	0	1	1
	11/NFAS	1	1	A	S a4	S a5	S a6	S a7	S a8
	12/FAS	C_3	0	0	1	1	0	1	1
	13/NFAS	E_1	1	A	S a4	S a5	S a6	S a7	S a8
	14/FAS	C_4	0	0	1	1	0	1	1
	15/NFAS	E_2	1	A	S a4	S a5	S a6	S a7	S a8

Table 7 - FAS and NFAS Structure

☐ indicates position of CRC-4 multiframe alignment signal.

Table 8 illustrates the organization of the MT9075B transmit and receive national bit buffers. Each row is an addressable byte of the MT9075B national bit buffer, and each column contains the national bits of an odd numbered frame of each CRC-4 Multiframe. The transmit and receive national bit buffers are located at page 0DH and 0EH respectively.

Address able Bytes	Frames 1, 3, 5, 7, 9, 11, 13 & 15 of a CRC-4 Multiframe							
	F1	**F3**	**F5**	**F7**	**F9**	**F11**	**F13**	**F15**
NBB0	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}	S_{a4}
NBB1	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}	S_{a5}
NBB2	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}	S_{a6}
NBB3	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}	S_{a7}
NBB4	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}	S_{a8}

Table 8 - MT9075B National Bit Buffers

Note that the Data Link (DL) pin functions, if selected, override the transmit national bit buffer function.

The CRC-4 Alignment status CALN (page 03H, address 12H) and maskable interrupt CALNI (page 01H, address 1DH) indicate the beginning of every received CRC-4 multiframe.

Maskable interrupts are available for change of state of S_{a5} bits or change of state of S_{a6} nibbles. By writing the proper control bits, an interrupt can be generated on a change of state of any S_a bit (except S_{a4} - normally reserved for the data link), or any nibbles for S_{a5} through S_{a8}. See the description of page 01H, address 19H for more details.

In addition, the transparent transmission of channel 0 is supported to meet the ETS requirement. Selectable on a bit by bit basis, S_a bits in channel 0 DSTi data can be programmed using register 17H of page 01H to be sent transparently onto the line.

Data Link Operation

Timeslot 0

The MT9075B has a user defined 4, 8, 12, 16 or 20 kbit/s data link for transport of maintenance and performance monitoring information across the PCM 30 link. This channel functions using the S_a bits ($S_{a4} \sim S_{a8}$) of the PCM 30 timeslot zero non-frame alignment signal (NFAS). Since the NFAS is transmitted every other frame - a periodicity of 250 microseconds - the aggregate bit rate is a multiple of 4 kb/s. As there are five S_a bits independently available for this data link, the bit rate will be 4, 8, 12, 16 or 20 kb/s, depending on the bits selected for the Data Link (DL).

The S_a bits used for the DL are selected by setting the appropriate bits, $S_{a4} \sim S_{a8}$, to one in the Data Link Select Word (page 01H, address 10H, bits 4-0). Access to the DL is provided by pins TxDLCLK, TxDL, RxDLCLK and RxDL, which allow easy interfacing to an external controller.

Data to be transmit onto the line in the S_a bit position is clocked in from the TxDL pad (pin 65 in PLCC, pin 62 in MQFP) with the clock TxDLCLK (pin 64 in PLCC, pin 61 in MQFP). Although the aggregate clock rate equals the bit rate, it has a nominal pulse width of 244 ns, and it clocks in the TxDL as if it were a 2.048 Mb/s data stream. The clock can only be active during bit times 4 to 0 of the STBUS frame. The TxDL input signal is clocked into the MT9075B by the rising edge of TxDLCLK. If bits are selected to be a part of the DL, all other programmed functions for those S_a bit positions are overridden.

The RxDLCLK signal (pin 39 in PLCC, pin 20 in MQFP) is derived from the receive extracted clock and is aligned with the receive data link output RxDL. The HDB3 decoded receive data, at 2.048 Mbit/s, is clocked out

of the device on pin RxDL (pin 40 in PLCC, pin 21 in MQFP). In order to facilitate the attachment of this data stream to a Data Link controller, the clock signal RxDLCLK consists of positive pulses, of nominal width of 244 ns, during the S_a bit cell times that are selected for the data link. Again, this selection is made by programming address 10H of master control page 01H. No DL data will be lost or repeated when a receive frame slip occurs. See Figures 13-16 for timing requirements.

Timeslot 16

Channel 16 may be used to create a transparent 64 kb/s clear channel. In this event CSTi (pin 6 in PLCC, pin 71 in MQFP) becomes the data input pin for channel 16 transmit data, and CSTo (pin 5 in PLCC, pin 70 in MQFP) becomes a 64 kb/s serial output link. The CSTo output link is synchronous to the extracted clock timebase. The pin Rx64KCK (pin 47 in PLCC, pin 35 in MQFP) provides a 64 kHz clock for use with 64 kb/s data emanating from CSTo. The 64 kb/s input data from CSTi is clocked in with an internal 64 kHz clock synchronous to the I/O pin $\overline{C4b}$ (pin 45 in PLCC, pin 33 in MQFP) timebase. The internal clock toggles coincident with every second ST-BUS channel boundary, with the first rising edge of a frame occurring at the beginning of ST-BUS channel 2.

Dual HDLC

The MT9075B has two identical HDLC controllers (HDLC0, HDLC1) for the S_a bits and channel 16 respectively. The following features are common to both HDLC controllers:

- Independent transmit and receive FIFO's;
- Receive FIFO maskable interrupts for nearly full (programmable interrupt levels) and overflow conditions;
- Transmit FIFO maskable interrupts for nearly empty (programmable interrupt levels) and underflow conditions;
- Maskable interrupts for transmit end-of-packet and receive end-of-packet;
- Maskable interrupts for receive bad-frame (includes frame abort);
- Transmit end-of-packet and frame-abort functions.

HDLC0 Functions

When connected to the Data Link (DL) HDLC0 will operate at a selected bit rate of 4, 8, 12, 16 or 20 kbits/sec. HDLC0 can be selected by setting the control bit HDLC0 (bit 7) to one in page 01H, address 14H. When this bit is zero all interrupts from HDLC0 are masked. For more information refer to following sections.

HDLC1 Functions

This controller may be connected to time slot 16 under Common Channel Signalling (CCS) mode. It should be noted that the AIS16S function (page 03H, address 19H) will always be active and the TAIS16 function (page 01H, address 16H) will override all other transmit signalling.

HDLC1 can be selected by setting the control bit HDLC1 (bit 6) to one in page 01H, address 14H. When this bit is zero all interrupts from HDLC1 are masked.

HDLC Overview

The HDLC handles the bit oriented packetized data transmission as per X.25 level two protocol defined by CCITT. It provides flag and abort sequence generation and detection, zero insertion and deletion, and Frame Check Sequence (FCS) generation and detection. A single byte, dual byte and all call address in the received frame can be recognized. Access to the receive FCS and inhibiting of transmit FCS for terminal adaptation are also provided. Each HDLC controller has a 128 byte deep FIFO associated with it. The status and interrupt flags are programmable for FIFO depths that can vary from 16 to 128 bytes in steps of 16 bytes. These and other features are enabled through the HDLC control registers on page 0BH and 0CH.

HDLC Frame Structure

A valid HDLC frame (also referred as "packet") begins with an opening flag, contains at least 16 bits of data field, and ends with a 16 bit FCS followed by a closing flag (Table 9).

All HDLC frames start and end with a unique flag sequence "01111110_2" (7EH). The transmitter generates these flags and appends them to the packet to be transmitted. The receiver searches the incoming data stream for the flags on a bit-by-bit basis to establish frame synchronization.

Opening Flag (7EH)	Data Field	FCS	Closing Flag (7EH)
One Byte 01111110	n Bytes n ≥ 2	Two Bytes	One Byte 01111110

Table 9 - HDLC Frame Format

The data field usually consists of an address field, control field and information field. The address field consists of one or two bytes directly following the opening flag. The control field consists of one byte directly following the address field. The information field immediately follows the control field and consists of *n* bytes of data. The HDLC does not distinguish between the control and information fields and a packet does not need to contain an information field to be valid.

The FCS field, which precedes the closing flag, consists of two bytes. A cyclic redundancy check utilizing the CCITT standard polynomial "$X^{16}+X^{12}+X^5+1$" produces the 16-bit FCS. In the transmitter the FCS is calculated on all bits of the address and data field. The complement of the FCS is transmitted, most significant bit first, in the FCS field. The receiver calculates the FCS on the incoming packet address, data and FCS field and compares the result to "F0B8". If no transmission errors are detected and the packet between the flags is at least 32 bits in length then the address and data are entered into the receive FIFO minus the FCS which is discarded.

Data Transparency (Zero Insertion/Deletion)

Transparency ensures that the contents of a data packet do not imitate a flag, go-ahead, frame abort or idle channel. The contents of a transmitted frame, between the flags, is examined on a bit-by-bit basis and a 0 is inserted after all sequences of 5 contiguous 1s (including the last five bits of the FCS). Upon receiving five contiguous 1s within a frame the receiver deletes the following 0.

Invalid Frames

A frame is invalid if one of the following four conditions exists:

- If the FCS pattern generated from the received data does not match the "F0B8" pattern then the last data byte of the packet is written to the received FIFO with a 'bad packet' indication.

- A short frame exists if there are less than 25 bits between the flags. Short frames are ignored by the receiver and nothing is written to the receive FIFO.

- Packets which are at least 25 bits in length but less than 32 bits between the flags are also invalid. In this case the data is written to the FIFO but the last byte is tagged with a "bad packet" indication.

- If a frame abort sequence is detected the packet is invalid. Some or all of the current packet will reside in the receive FIFO, assuming the packet length before the abort sequence was at least 26 bits long.

Frame Abort

The transmitter will abort a current packet by substituting a zero followed by seven contiguous 1s in place of the normal packet. The receiver will abort upon reception of seven contiguous 1s occurring between the flags of a packet which contains at least 26 bits.

Note that should the last received byte before the frame abort end with contiguous 1s, these are included in the seven 1s required for a receiver abort. This means that the location of the abort sequence in the receiver may occur before the location of the abort sequence in the originally transmitted packet. If this happens then the last data written to the receive FIFO will not correspond exactly with the last byte sent before the frame abort.

Interframe Time Fill and Link Channel States

When the HDLC transmitter is not sending packets it will wait in one of two states

*   Interframe Time Fill state: This is a continuous series of flags occurring between frames indicating that the channel is active but that no data is being sent.

*   Idle state: An idle Channel occurs when at least 15 contiguous 1s are transmitted or received.

In both states the transmitter will exit the wait state when data is loaded into the transmitter FIFO.

Go-Ahead

A go-ahead is defined by a 9 bit sequence "011111110" (contiguous 7Fs) and hence is the occurrence of a frame abort sequence followed by a zero. This feature is used to distinguish a proper in-packet frame abort sequence from one occurring outside of a packet for some special applications

HDLC Functional Description

The HDLC controller can be reset by either the reset pin ($\overline{RESET}$, pin 11 in PLCC or pin 84 in MQFP) or by the control bit HRST at address 1BH in page 0BH (for HDLC0) or page 0CH (for HDLC1). When reset, the HDLC Control Registers are cleared, resulting in the transmitter and receiver being disabled. The receiver and transmitter can be enabled independent of each other through Control Register 1 at address 13H. The transceiver input and output are enabled when the enable control bits in Control Register 1 are set. Transmit to receive loopback as well as a receive to transmit loopback are also supported. Transmit and receive bit rates and enables can operate independently.

Received packets from the serial interface are sectioned into bytes by an HDLC receiver that detects flags, checks for go-ahead signals, removes inserted zeros, performs a cyclical redundancy check (CRC) on incoming data, and monitors the address if required. Packet reception begins upon detection of an opening flag. The resulting bytes are concatenated with two status bits (RQ9 and RQ8 at address 14H) and placed in a receiver first-in-first-out buffer (RX FIFO). Register 14H also contains control bits that generate status and interrupts for microprocessor read control.

In conjunction with the control circuitry, the microprocessor writes data bytes into a transmit buffer (TX FIFO) register that generates status and interrupts. Packet transmission begins when the microprocessor writes a byte to the TX FIFO. Two status bits are added to the TX FIFO for transmitter control of frame aborts (FA) and end of packet (EOP) flags. Packets have flags appended, zeros inserted, and an FCS, added automatically during serial transmission. When the TX FIFO is empty and finished sending a packet, Interframe Time Fill bytes (continuous flags (7E hex)), or Mark Idle (continuous ones) are transmitted to indicate that the channel is idle.

HDLC Transmitter

Following initialization and enabling, the transmitter is in the Idle Channel state (Mark Idle), continuously sending ones. Interframe Time Fill state (Flag Idle) is selected by setting the Mark Idle bit in Control Register 1 to one[1]. The transmitter remains in either of these two states until data is written to the TX FIFO. Control Register 1 bits EOP (End Of Packet) and FA (Frame Abort) are set as status bits before the microprocessor loads 8 bits of data into the

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1. If the MT9075B HDLC transmitter is set up in the Interframe Time Fill state (bit 2 Mark-Idle =1, page B or C, address 13H), then it will occasionally (less than 1% of the time) fail to transmit the opening flag when it is changed from the disabled state to the enabled state (bit 5 TxEN changed from 0 to 1). A missing opening flag will cause the packet to be lost at the receiving end.

This problem only affects the first packet transmitted after the HDLC transmitter is enabled. Subsequent packets are unaffected.

10 bit wide FIFO (8 bits data and 2 bits status). To change the tag bits being loaded in the FIFO, Control Register 1 must be written to before writing to the FIFO. However, EOP and FA are reset after writing to the TX FIFO. The Transmit Byte Count Register may also be used to tag an EOP. The register is loaded with the number of bytes in the packet and decrements after every write to the Tx FIFO. When a count of one is reached, the next byte written to the FIFO is tagged as an end of packet. The register may be made to cycle through the same count if the packets are of the same length by setting Control Register 2, bit Cycle (at address 15H of page 0BH for HDLC0 or 0CH for HDLC1).

If the transmitter is in the Idle Channel state when data is written to the TX FIFO, then an opening flag is sent and data from TX FIFO follows. Otherwise, data bytes are transmitted as soon as the current flag byte has been sent. TX FIFO data bytes are continuously transmitted until either the FIFO is empty or an EOP or FA status bit is read by the transmitter. After the last bit of the EOP byte has been transmitted, a 16-bit FCS is sent followed by a closing flag. When multiple packets of data are loaded into TX FIFO, only one flag is sent between packets.

Frame Aborts (FA, the transmission of 7F hex), are transmitted by tagging a byte previously written to the TX FIFO. When a byte has an FA tag, then an FA is sent instead of that tagged byte. That is, all bytes previous to but not including that byte are sent. After an FA, the transmitter returns to the Mark Idle or Interframe Time Fill state, depending on the state of the Mark idle control bit.

TX FIFO underrun will occur if the FIFO empties and the last byte did not have either an EOP or FA tag. A frame abort sequence will be sent when an underrun occurs.

Below is an example of the transmission of a three byte packet ('AA''03''77' hex) (Interframe time fill). TxEN can be enabled before or after this sequence.

(a) Write'04' to Control Register 1 - Mark Idle bit set
(b) Write'AA' to Tx FIFO -Data byte
(c) Write'03' to Tx FIFO - Data byte
(d) Write'34' to Control Register 1 - TxEN; EOP; Mark Idle bits set
(e) Write'77' to Tx FIFO - Final data byte

The transmitter may be enabled independently of the receiver. This is done by setting the TxEN bit of the Control Register. Enabling happens immediately upon writing to the register. Disabling using TxEN will occur after the completion of the transmission of the present packet; the contents of the FIFO are not cleared. Disabling will consist of stopping the transmitter clock. The Status and Interrupt Registers may still be read, and the FIFO and Control Registers may be written to while the transmitter is disabled. The transmitted FCS may be inhibited using the Tcrci bit of Control Register 2. In this mode the opening flag followed by the data and closing flag is sent and zero insertion is still included, but no FCS. That is, the FCS is injected by the microprocessor as part of the data field. This is used in V.120 terminal adaptation for synchronous protocol sensitive UI frames.

HDLC Receiver

After initialization and enabling, the receiver clocks in serial data, continuously checking for Go-Aheads (0 1111 1110), flags (0111 1110), and Idle Channel states (at least fifteen ones). When a flag is detected, the receiver synchronizes itself to the serial stream of data bits, automatically calculating the FCS. If the data length between flags after zero removal is less than 25 bits, then the packet is ignored so no bytes are loaded into Rx FIFO. When the data length after zero removal is between 25 and 31 bits, a first byte and bad FCS code are loaded into the Rx FIFO. For an error-free packet, the result in the CRC register should match the HEX pattern of "F0B8" when a closing flag is detected.

If address recognition is required, the Receiver Address Recognition Registers (address 10H and 11H) are loaded with the desired address and the Adrec bit in the Control Register 1 (address 13H) is set to one. Bit 0 of the Address Registers is used as an enable bit for that byte, thus allowing either or both of the first two bytes to be compared to the expected values. In addition, seven bits of address comparison can be realized on the first byte if this is a single byte address by setting the *Seven* bit of Control Register 2 (address 15H).

Two Status Register bits (RQ8 and RQ9) are appended to each data byte as it is written to the Rx FIFO. They indicate that a good packet has been received (good FCS and no frame abort), or a bad packet with either incorrect FCS or frame abort. The Status and Interrupt Registers should be read before reading the Rx FIFO since status and interrupt information correspond to the byte at the output of the FIFO (i.e., the byte about to be read). The Status Register bits are encoded as follows:

RQ9	RQ8	Byte status
1	1	last byte (bad packet)
0	1	bad packet
1	0	last byte (good packet)
0	0	packet byte

The end-of-packet-detect (EOPD) interrupt indicates that the last byte written to the RX FIFO was an EOP byte. The end-of-packet-read (EOPR) interrupt indicates that the byte about to be read from the RX FIFO is an EOP byte. The Status Register should be read to see if the packet is good or bad before the byte is read.

A minimum size packet has an 8-bit address, an 8-bit control byte, and a 16-bit FCS pattern between the opening and closing flags. Thus, the absence of a data transmission error and a frame length of at least 32 bits results in the receiver writing a valid packet code with the EOP byte into RX FIFO. The last 16 bits before the closing flag are regarded as the FCS pattern and will not be transferred to the receiver FIFO. Only data bytes (Address, Control, Information) are loaded into the Rx FIFO.

In the case of an RX FIFO overflow, no clocking occurs until a new opening flag is received. In other words, the remainder of the packet is not clocked into the FIFO. Also, the top byte of the FIFO will not be written over. If the FIFO is read before the reception of the next packet then reception of that packet will occur. If two beginning of packet conditions (RQ9=0; RQ8=1) are seen in the FIFO, without an intermediate EOP status, then overflow occurred for the first packet.

The receiver may be enabled independently of the transmitter. This is done by setting the RxEN bit of Control Register 1. Enabling happens immediately upon writing to the register. Disabling using RxEN will occur after the present packet has been completely loaded into the FIFO. Disabling can occur during a packet if no bytes have been written to the FIFO yet. Disabling will consist of disabling the internal receive clock. The FIFO, Status, and Interrupt Registers may still be read while the receiver is disabled. Note that the receiver requires a flag before processing a frame, thus if the receiver is enabled in the middle of an incoming packet it will ignore that packet and wait for the next complete one.

The receive CRC (FCS) can be monitored in the Rx CRC Registers (address 18H and 19H). These registers contain the actual CRC sent by the other transmitter in its original form, that is, MSB first and bits inverted. These registers are updated by each end of packet (closing flag) received and therefore should be read when an end of packet is received so that the next packet does not overwrite the registers.

Slip Buffer

In addition to the elastic buffer in the jitter attenuator(JA), another elastic buffer (two frames deep) is present, attached between the receive side and the ST-BUS (or GCI Bus) side of the MT9075B. This elastic buffer is configured as a slip buffer which absorbs wander and low frequency jitter in multi-trunk applications. The received PCM 30 data is clocked into the slip buffer with the E2o clock and is clocked out of the slip buffer with the $\overline{C4b}$ clock. The E2o extracted clock is generated from, and is therefore phase-locked with, the receive PCM 30 data. In normal operation, the E2o clock will be phase-locked to the $\overline{C4b}$ clock by an external phase locked loop (PLL). Therefore, in a single trunk system the receive data is in phase with the E2o clock, the $\overline{C4b}$ clock is phase-locked to the E2o clock, and the read and write positions of the slip buffer will remain fixed with respect to each other.

In a multi-trunk slave or loop-timed system (i.e., PABX application) a single trunk will be chosen as a network synchronizer, which will function as described in the previous paragraph. The remaining trunks will use the system timing derived from the synchronizer to clock data out of their slip buffers. Even though the PCM 30 signals from the network are synchronous to each other, due to multiplexing, transmission impairments and route diversity, these