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T1/E1/J1 3.3 V Single Chip Transceiver

Data Sheet

Features

- Combined T1/E1/J1 framer and LIU, with PLL and 3 HDLCs
- In T1/J1 mode the LIU can recover signals attenuated by up to 36 dB (at 772 kHz)
- In E1 mode the LIU can recover signals attenuated by up to 40 dB (at 1.024 MHz)
- Low jitter digital PLL (intrinsic jitter < 0.02UI)
- HDLCs can be assigned to any timeslot
- Comprehensive alarm detection, performance monitoring and error insertion functions
- 2.048 Mbit/s or 8.192 Mbit/s ST-BUS streams
- Support for Inverse Mux for ATM (IMA)
- Support for V5.1 and V5.2 Access Networks
- 3.3 V operation with 5 V tolerant inputs
- Intel or Motorola non-multiplexed 8-bit microprocessor port
- JTAG boundary scan

September 2011

Ordering Information

MT9076BPR1	68 Pin PLCC*	Tape & Reel
MT9076BB1	80 Pin LQFP*	Trays
MT9076BP1	68 Pin PLCC*	Tubes

*Pb Free Matte Tin

-40°C to +85°C

Applications

- T1/E1/J1 add/drop multiplexers
- Access networks
- Wireless base stations
- CO and CPE equipment interfaces
- Primary rate ISDN nodes
- Digital Cross-connect Systems (DCS)

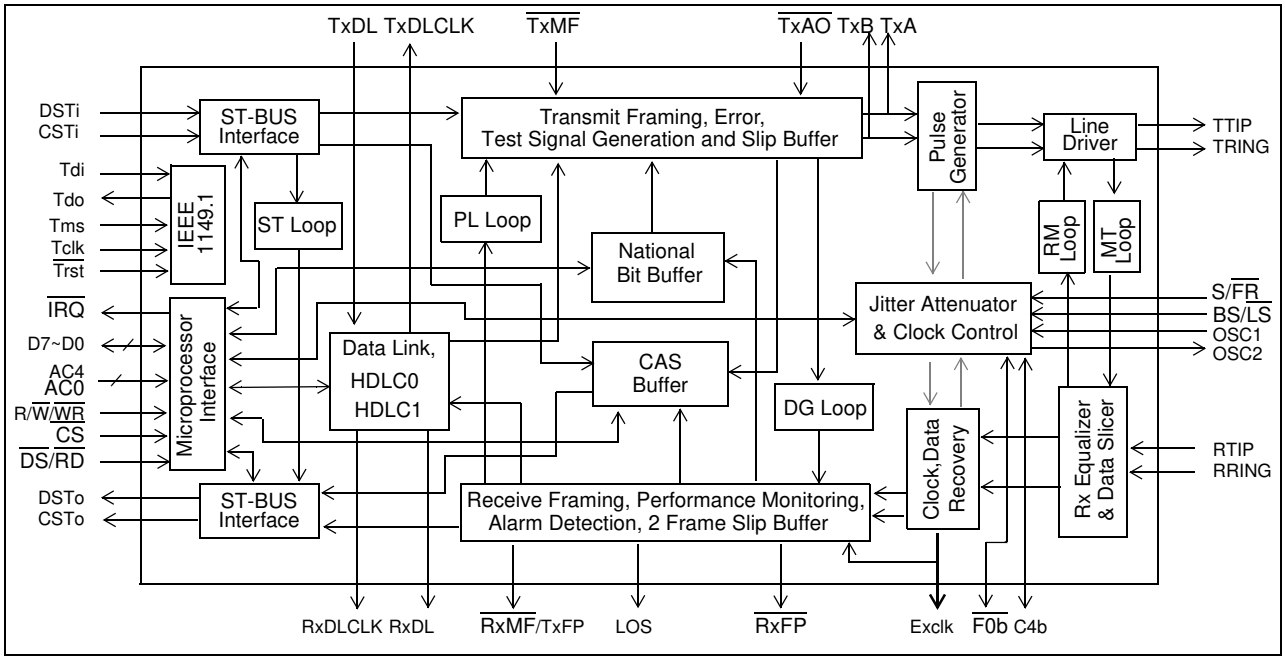

Figure 1 - MT9076 Functional Block

Description

The MT9076 is a highly featured single chip solution for terminating T1/E1/J1 trunks. It contains a long-haul LIU, an advanced framer, a high performance PLL and 3 HDLCs.

In T1 mode, the MT9076 supports D4, ESF and SLC-96 formats meeting the latest recommendations including AT&T PUB43801, TR-62411; ANSI T1.102, T1.403 and T1.408; Telcordia GR-303-CORE.

In E1 mode, the MT9076 supports the latest ITU-T Recommendations including G.703, G.704, G.706, G.732, G.775, G.796, G.823, G.964 (V5.1), G.965 (V5.2) and I.431. It also supports ETSI ETS 300 011, ETS 300 166, ETS 300 233, ETS 300 324 (V5.1) and ETS 300 347 (V5.2).

Change Summary

Changes from the June 2006 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

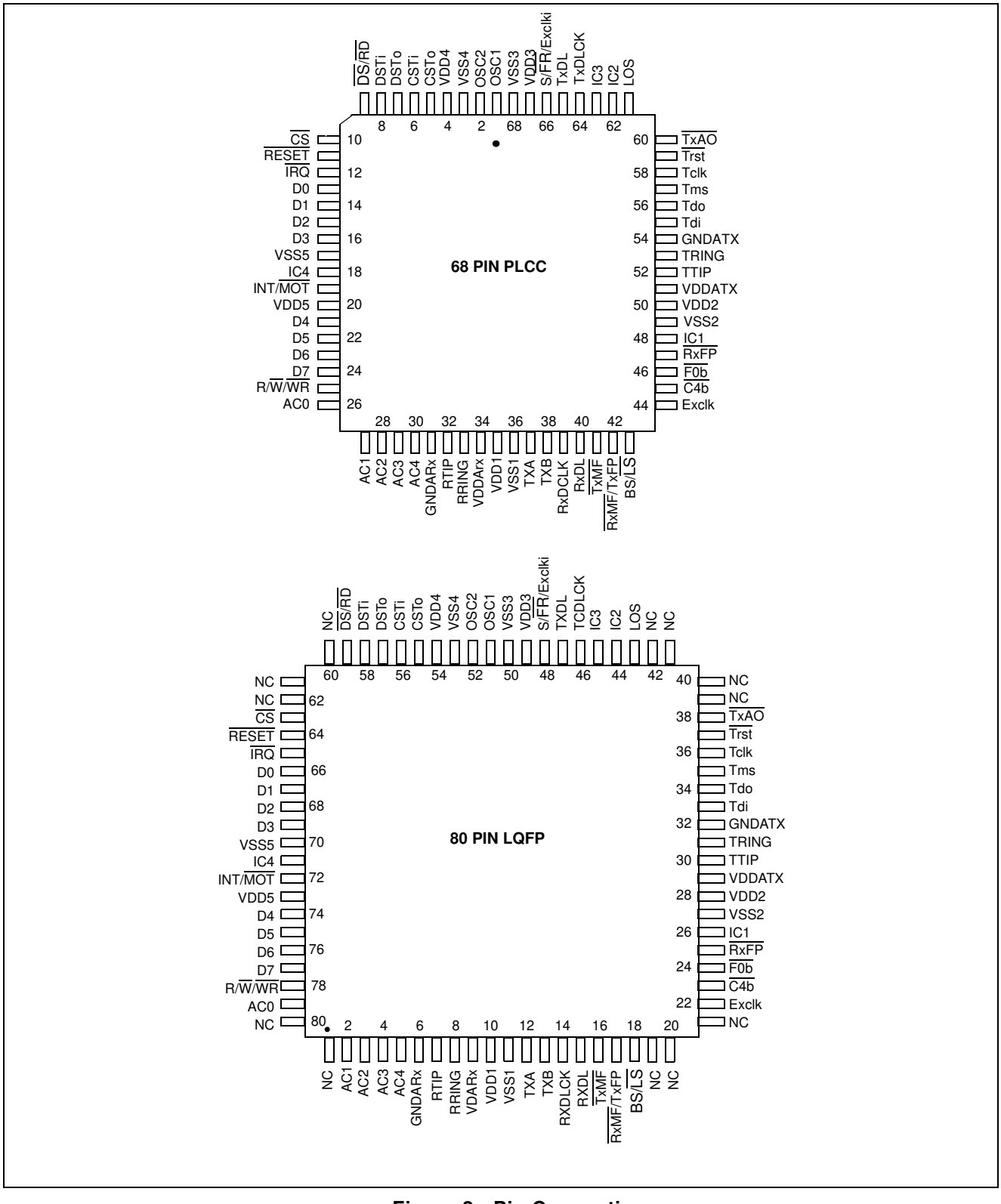

Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
PLCC	LQFP		
1	51	OSC1	**Oscillator (3 V Input).** This pin is either connected via a 20.000 MHz crystal to OSC2 where a crystal is used, or is directly driven when a 20.000 MHz. oscillator is employed.
2	52	OSC2	**Oscillator (3 V Output).** Connect a 20.0 MHz crystal between OSC1 and OSC2. Not suitable for driving other devices.
3	53	V_{SS4}	**Negative Power Supply.** Digital ground.
4	54	V_{DD4}	**Positive Power Supply.** Digital supply (+3.3 V ± 5%).
5	55	CSTo	**Control ST-BUS (5 V tolerant Output)**. CSTo carries serial streams for CAS and CCS respectively a 2.048 Mbit/s ST-BUS status stream which contains the 30 receive signaling nibbles (ABCDZZZZ or ZZZZABCD). The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are tristated when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and tristated nibbles are reversed.
6	56	CSTi	**Control ST-BUS (5 V tolerant Input)**. CSTi carries serial streams for CAS and CCS respectively a 2.048 Mbit/s ST-BUS control stream which contains the 30 transmit signaling nibbles (ABCDXXXX or XXXXABCD) when RPSIG=0. When RPSIG=1 this pin has no function. The most significant nibbles of each ST-BUS time slot are valid and the least significant nibbles of each ST-BUS time slot are ignored when control bit MSN (page 01H, address 1AH, bit 1) is set to 1. If MSN=0, the position of the valid and ignored nibbles is reversed.
7	57	DSTo	**Data ST-BUS (5 V tolerant Output).** A 2.048 Mbit/s serial stream which contains the 24/30 PCM(T1/E1) or data channels received on the PCM 24/30 (T1/E1) line.
8	58	DSTi	**Data ST-BUS (5 V tolerant Input).** A 2.048 Mbit/s serial stream which contains the 24/30 (T1/E1) PCM or data channels to be transmitted on the PCM 24/30 (T1/E1) line.
9	59	$\overline{DS}/\overline{RD}$	**Data/Read Strobe (5 V tolerant Input)**. In Motorola mode ($\overline{DS}$), this input is the active low data strobe of the processor interface. In Intel mode ($\overline{RD}$), this input is the active low read strobe of the processor interface.
10	63	$\overline{CS}$	**Chip Select (5 V tolerant Input)**. This active low input enables the non-multiplexed parallel microprocessor interface of the MT9076. When $\overline{CS}$ is set to high, the microprocessor interface is idle and all bus I/O pins will be in a high impedance state.
11	64	$\overline{RESET}$	**$\overline{RESET}$ (5 V tolerant Input).** This active low input puts the MT9076 in a reset condition. $\overline{RESET}$ should be set to high for normal operation. The MT9076 should be reset after power-up. The $\overline{RESET}$ pin must be held low for a minimum of 1 μsec. to reset the device properly.
12	65	$\overline{IRQ}$	**Interrupt Request (5 V tolerant Output).** A low on this output pin indicates that an interrupt request is presented. $\overline{IRQ}$ is an open drain output that should be connected to V_{DD} through a pull-up resistor. An active low $\overline{CS}$ signal is not required for this pin to function.
13 - 16	66-69	D0 - D3	**Data 0 to Data 3 (5 V tolerant Three-state I/O)**. These signals combined with D4-D7 form the bidirectional data bus of the parallel processor interface (D0 is the least significant bit).

Pin Description (continued)

Pin #		Name	Description
PLCC	LQFP		
17	70	VSS5	**Negative Power Supply.** Digital ground.
18	71	IC4	**Internal Connection (3 V Input).** Tie to V_{SS} (Ground) for normal operation.
19	72	INT/$\overline{\text{MOT}}$	**Intel/Motorola Mode Selection (5 V tolerant Input)**. A high on this pin configures the processor interface for the Intel parallel non-multiplexed bus type. A low configures the processor interface for the Motorola parallel non-multiplexed type.
20	73	VDD5	**Positive Power Supply.** Digital supply (+3.3 V ± 5%).
21 - 24	74-77	D4 - D7	**Data 4 to Data 7 (5 V tolerant Three-state I/O).** These signals combined with D0-D3 form the bidirectional data bus of the parallel processor interface (D7 is the most significant bit).
25	78	R/$\overline{\text{W}}$/$\overline{\text{WR}}$	**Read/Write/Write Strobe (5 V tolerant Input).** In Motorola mode (R/W), this input controls the direction of the data bus D[0:7] during a microprocessor access. When R/W is high, the parallel processor is reading data from the MT9076. When low, the parallel processor is writing data to the MT9076. For Intel mode ($\overline{\text{WR}}$), this active low write strobe configures the data bus lines as output.
26 - 30	79, 2-5	AC0 - AC4	**Address/Control 0 to 4 (5 V tolerant Inputs).** Address and control inputs for the non-multiplexed parallel processor interface. AC0 is the least significant input.
31	6	GNDARx	**Receive Analog Ground.** Analog ground for the LIU receiver.
32 33	7 8	RTIP RRING	**Receive TIP and RING (3 V Input).** Differential inputs for the receive line signal - must be transformer coupled (See Figure 5 on page 24). In digital framer mode these pins accept digital 3 volt signals from a physical layer device. They may accept a split phase unipolar signal (RTIP and RRING employed) or an NRZ signal (RTIP only used).
34	9	VDDARx	**Receive Analog Power Supply.** Analog supply for the LIU receiver (+3.3 V ± 5%).
35	10	VDD1	**Positive Power Supply.** Digital supply (+3.3 V ± 5%).
36	11	VSS1	**Negative Power Supply.** Digital ground.
37	12	TxA	**Transmit A (5 V tolerant Output).** When the internal LIU is disabled (digital framer only mode), if control bit NRZ=1, an NRZ output data is clocked out on pin TxA with the rising edge of Exclk (TxB has no function when NRZ format is selected). If NRZ=0, pins TxA and TxB are a complementary pair of signals that output digital dual-rail data clocked out with the rising edge of Exclk.
38	13	TxB	**Transmit B (5 V tolerant Output).** When the internal LIU is disabled and control bit NRZ=0, pins TxA and TxB are a complementary pair of signals that output digital dual-rail data clocked out with the rising edge of Exclk.
39	14	RxDLCLK	**Data Link Clock (5 V tolerant Output)**. A gapped clock signal derived from the extracted line clock, available for an external device to clock in RxDL data (at 4, 8, 12, 16 or 20 kHz) on the rising edge.
40	15	RxDL	**Receive Data Link (5 V tolerant Output)**. A serial bit stream containing received line data after zero code suppression. This data is clocked out with the rising edge of Exclk.
41	16	$\overline{\text{TxMF}}$	**Transmit Multiframe Boundary (5 V tolerant Input).** An active low input used to set the transmit multiframe boundary (CAS or CRC multiframe). The MT9076 will generate its own multiframe if this pin is held high. This input is usually pulled high for most applications.

Pin Description (continued)

Pin #		Name	Description
PLCC	LQFP		
42	17	$\overline{\text{RxMF}}$/TxFP	**Receive Multiframe Boundary / Transmit Frame Boundary (5 V tolerant Output).** If the control bit Tx8KEN (page 02H address 10H bit 2) is low, this negative output pulse delimits the received multiframe boundary. The next frame output on the data stream (DSTo) is basic frame zero on the T1 or PCM 30 link. In E1 mode this receive multiframe signal can be related to either the receive CRC multiframe (page 01H, address 17H, bit 6, MFSEL=1) or the receive signaling multiframe (MFSEL=0). If the control bit Tx8KEN is set high, this positive output pulse delimits the frame boundary (the first bit transmit in the frame) for the digital output stream on pins TXA and TXB.
43	18	BS/$\overline{\text{LS}}$	**Bus/Line Synchronization Mode Selection (5 V tolerant Input)**. If high, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be inputs; if low, $\overline{\text{C4b}}$ and $\overline{\text{F0b}}$ will be outputs.
44	22	Exclk	**2.048 MHz in E1 mode or 1.544 MHz in T1 mode, Extracted Clock (5 V tolerant Output).** The clock extracted from the received signal and used internally to clock in data received on RTIP and RRING.
45	23	$\overline{\text{C4b}}$	**4.096 MHz System Clock (5 V tolerant Input/Output).** $\overline{\text{C4b}}$ is the clock for the ST-BUS sections and transmit serial PCM data of the MT9076. In the free-run (S/$\overline{\text{FR}}$/Exclki=0) or line synchronous mode (S/$\overline{\text{FR}}$/Exclki=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in bus synchronous mode (S/$\overline{\text{FR}}$/Exclki=1 and BS/$\overline{\text{LS}}$=1) this signal is an input clock.
46	24	$\overline{\text{F0b}}$	**Frame Pulse (5 V tolerant Input/Output).** This is the ST-BUS frame synchronization signal, which delimits the 32 channel frame of CSTi, CSTo, DSTi, DSTo and the PCM30 link. In the free-run (S/$\overline{\text{FR}}$/Exclki=0) or line synchronous mode (S/$\overline{\text{FR}}$/Exclki=1 and BS/$\overline{\text{LS}}$=0) this signal is an output, while in bus synchronous mode (S/$\overline{\text{FR}}$/Exclki=1 and BS/$\overline{\text{LS}}$=1) this signal is an input.
47	25	$\overline{\text{RxFP}}$	**Receive Frame Pulse/Receive CCS Clock (5 V tolerant Output).** An 8kHz pulse signal, which is low for one extracted clock period. This signal is synchronized to the receive DS1 or PCM 30 basic frame boundary.
48	26	IC1	**Internal Connection.** Must be left open for normal operation.
49	27	V_{SS2}	**Negative Power Supply.** Digital ground.
50	28	V_{DD2}	**Positive Power Supply.** Digital supply (+3.3 V ± 5%).
51	29	VDD_{ATx}	**Transmit Analog Power Supply.** Analog supply for the LIU transmitter (+3.3 V ±5%).
52 53	30 31	TTIP TRING	**Transmit TIP and RING(Output).** Differential outputs for the transmit line signal - must be transformer coupled (See Figure 5 on page 24).
54	32	GND_{ATx}	**Transmit Analog Ground.** Analog ground for the LIU transmitter.
55	33	Tdi	**IEEE 1149.1a Test Data Input (3 V Input).** If not used, this pin should be pulled high.
56	34	Tdo	**IEEE 1149.1a Test Data Output (5 V tolerant Output).** If not used, this pin should be left unconnected.
57	35	Tms	**IEEE 1149.1a Test Mode Selection (3 V Input)**. If not used, this pin should be pulled high.
58	36	Tclk	**IEEE 1149.1a Test Clock Signal (3 V Input).** If not used, this pin should be pulled high.
59	37	$\overline{\text{Trst}}$	**IEEE 1149.1a Reset Signal (3 V Input).** If not used, this pin should be held low.

Pin Description (continued)

Pin #		Name	Description
PLCC	LQFP		
60	38	$\overline{\text{TxAO}}$	**Transmit All Ones (Input).** High - TTIP, TRING will transmit data normally. Low - TTIP, TRING will transmit an all ones signal.
61	43	LOS	**Loss of Signal or Synchronization (5 V tolerant Output).** When high, and LOS/LOF (page 0, this signal indicates that the receive portion of the MT9076 is either not detecting an incoming signal (bit LLOS on page 03H address 16H is one) or is detecting a loss of basic frame alignment condition (bit $\overline{\text{TSYNC}}$ (T1), $\overline{\text{SYNC}}$ (E1) on page 03H address 10H is one). If LOS/LOF=1, a high on this pin indicates a loss of signal condition.
62	44	IC2	**Internal Connection (3 V Input).** Tie to V_{SS} (Ground) for normal operation.
63	45	IC3	**Internal Connection (3 V Input).** Tie to V_{SS} (Ground) for normal operation.
64	46	TxDLCLK	**Transmit Data Link Clock (5 V tolerant Output).** A gapped clock signal derived from a gated 2.048 Mbit/s clock for transmit data link at 4, 8, 12, 16 or 20 kHz. The transmit data link data (TxDL) is clocked in on the rising edge of TxDLCLK. TxDLCLK can also be used to clock DL data out of an external serial controller.
65	47	TxDL	**Transmit Data Link (5 V tolerant Input)**. An input serial stream of transmit data link data at 4, 8, 12, 16 or 20 kbit/s.
66	48	S/$\overline{\text{FR}}$/Exclki	**Synchronization/ Freerun / Extracted Clock (5 V tolerant Input).** If low, and the internal LIU is enabled, the MT9076 is in free run mode. Pins 45 C4b and 46 F0b are outputs generating system clocks. Slips will occur in the receive slip buffer as a result of any deviation between the MT9076's internal PLL (which is free - running) and the frequency of the incoming line data. If high, and the internal LIU is enabled, the MT9076 is in Bus or Line Synchronization mode depending on the BS/$\overline{\text{LS}}$ pin. If the internal LIU is disabled, in digital framer mode, this pin (Exclki) takes an input clock 1.544 MHz (T1)/ 2.048 MHz (E1) that clocks in the received digital data on pins RXA and RXB with its rising edge.
67	49	VDD3	**Positive Power Supply.** Digital supply (+3.3 V ± 5%)**.**
68	50	VSS3	**Negative Power Supply.** Digital ground.

Device Overview

The MT9076 is a T1/E1/J1 single chip transceiver that incorporates an advanced framer, a long-haul LIU (Line Interface Unit), a low jitter PLL (Phase Locked Loop) and 3 HDLCs (High-level Data Link Controller). The T1, E1 and J1 operating modes are selectable under software control.

Standards Compliance

In T1 mode, the MT9076 meets or supports the latest recommendations including Telcordia GR-303-CORE, AT&T PUB43801, TR-62411, ANSI T1.102, T1.403 and T1.408. In T1 ESF mode the CRC-6 calculation and yellow alarm can be configured to meet the requirements of a J1 interface.

In E1 mode, the MT9076 meets or supports the latest ITU-T Recommendations for PCM 30 and ISDN primary rate including G.703, G.704, G.706, G.732, G.775, G.796, G.823, G.964 (V5.1), G.965 (V5,2) and I.431. It also meets or supports ETSI ETS 300 011, ETS 300 166, ETS 300 233, ETS 300 324 (V5.1) and ETS 300 347 (V5.2).

Microprocessor Port

The MT9076 registers are accessible via an 8-bit parallel Motorola or Intel non-multiplexed microprocessor interface.

LIU

The MT9076 LIU interfaces the digital framer functions to either the DS1 (T1 mode) or PCM 30 (E1 mode) transformer-isolated four wire line.

In T1 mode, the LIU can pre-equalize the transmit signal to meet the T1.403 and T1.102 pulse templates after attenuation by 0 - 655 feet of 22 AWG PIC cable, alternatively it can provide line build outs of 7.5 dB, 15 dB and 22.5 dB. In T1 mode the receiver can recover signals attenuated by up to 36 dB at 772 kHz.

In E1 mode, the LIU transmits signals that meet the G.703 2.048 Mbit/s pulse template and the receiver can recover signals attenuated by up to 40 dB at 1024 kHz.

Digital Framer Only Mode

To accommodate some special applications, the MT9076 supports a digital framer only mode that provides direct access to the transmit and receive data in digital format, i.e., by-passing the analog LIU front-end. In digital framer only mode, the MT9076 supports unipolar non-return to zero or bipolar return to zero data.

PLL and Slip Buffers

The MT9076 PLL attenuates jitter from 2.5 Hz with a roll-off of 20 dB/decade. The intrinsic jitter is less than 0.02 UI. The device can operate in one of three timing modes: System Bus Synchronous Mode, Line Synchronous Mode, or Free-run Mode. In all three timing modes the low jitter output of the PLL provides timing to the transmit side of the LIU.

In T1 mode, the receive and transmit paths both include two-frame slip buffers. The transmit slip buffer features programmable delay and serves as a Jitter Attenuator (JA) FIFO and a rate converter between the ST-BUS and the 1.544 Mbit/s T1 line rate.

In E1 mode, the receive path includes a two-frame slip buffer and the transmit path contains a 128 bit Jitter Attenuator (JA) FIFO with programmable depth.

Interface to the System Backplane

On the system side the MT9076 framers can interface to a 2.048 Mbit/s or 8.192 Mbit/s ST-BUS backplane.

There is an asynchronous mode for Inverse MUX for ATM (IMA) applications, this enables the framer to interface to a 1.544 Mbit/s (T1) or 2.048 Mbit/s (E1) serial bus with asynchronous transmit and receive timing.

Framing Modes

The MT9076 framers operate in termination mode or transparent mode. In the receive transparent mode, the received line data is channelled to the DSTo pin with arbitrary frame alignment. In the transmit transparent mode, no framing or signaling is imposed on the data transmitted from the DSTi pin onto the line.

In T1 mode, the framers operate in any of the following framing modes: D4, Extended Superframe (ESF) or SLC-96.

In E1 mode, the framers run three framing algorithms: basic frame alignment, signaling multiframe alignment and CRC-4 multiframe alignment. The Remote Alarm Indication (RAI) bit is automatically controlled by an internal state machine.

Access to the Maintenance Channel

The T1 ESF Facility Data Link (FDL) bits can be accessed in the following three ways: Through the data link pins TxDL, RxDL, RxDLC and TxDLC; through internal registers for Bit Oriented Messages; through an embedded HDLC.

In E1 mode, the Sa bits (bits 4-8 of the non-frame alignment signal) can be accessed in four ways: Through data link pins TxDL, RxDL, RxDLC and TxDLC, through single byte transmit and receive registers; through five byte transmit and receive national bit buffers; through an embedded HDLC.

Robbed Bit Signaling/Channel Associated Signaling

Robbed bit signaling and channel associated signaling information can be accessed two ways: Via the microport; via the CSTi and CSTo pins. Signaling information is frozen upon loss of multiframe alignment.

In T1 mode, the MT9076 supports AB and ABCD robbed bit signaling. Robbed bit signaling can be enabled on a channel by channel basis.

In E1 mode the MT9076 supports Channel Associated Signaling (CAS) multiframing.

HDLCs

The MT9076 provides three embedded HDLCs with 128 byte deep transmit and receive FIFOs.

In T1 mode, the embedded HDLCs can be assigned to any channel and can operate at 56 kbit/s or 64 kbit/s. In T1 ESF mode, HDLCO can be assigned to the 4 kbit/s FDL.

In E1 mode, the embedded HDLCs can be assigned to any timeslot and can operate at 64 kbit/s. HDLCO can be assigned to timeslot 0 Sa bits (bits 4-8 of the non-frame alignment signal) and can operate at 4,8,12,16 or 20 kbit/s.

Performance Monitoring and Debugging

The MT9076 has a comprehensive suite of performance monitoring and debugging features. These include error counters, loopbacks, deliberate error insertion and a 2^{15} –1 QRS/PRBS generator/detector.

Interrupts

The MT9076 provides a comprehensive set of maskable interrupts. Interrupt sources consist of synchronization status, alarm status, counter indication and overflow, timer status, slip indication, maintenance functions and receive signaling bit changes.

MT9076 Detailed Feature List

Standards Compliance and Support

T1/J1 Mode

ANSI:
T1.102,T1.231, T1.403, T1.408

AT&T:
TR 62411, PUB43801

Telcordia:
GR-303-CORE

TTC:
JT-G703, JT-G704, JT-G706

E1 Mode

ETSI:
ETS 300 011, ETS 300 166, ETS 300 233, ETS 300 324, ETS 300 347

ITU:
G.703, G.704, G.706, G.732 G.775, G.796, G.823, I.431, G.964, G.965

Line Interface Unit (LIU)

- T1 and E1 modes use the same 1:1 transmit and receive transformers
- Internal register allows termination impedance to be changed under software control.
- Programmable pulse shapes and pulse amplitudes
- Automatic or manual receiver equalization
- Receive signal peak amplitude is reported with 8-bit resolution
- Output pin to indicate Loss Of Signal/ Loss Of Frame synchronization
- LIU output is disabled at power-up until enabled by software
- Input pin to force transmission of AIS

T1/J1 Mode

- Reliably recovers signals with cable attenuation up to 36 dB @ 772 kHz
- Transmit pulse meets T1.403 and T1.102 pulse templates
- Indicates analog Los Of Signal if the received signal is more than 20 dB or 40 dB below nominal for more than 1 ms
- Receiver tolerates jitter as required by AT&T TR62411

E1 Mode

- Reliably recovers signals with cable attenuation up to 40 dB @ 1024 kHz
- Transmit pulse meets G.703 pulse template
- Indicates analog Los Of Signal if the received signal is more than 20 dB or 40 dB below nominal for more than 1 ms
- Receiver tolerates jitter as required by ETSI ETS 300 011

T1/J1 Mode

- Transmit Pre-equalization and Line Build Out options:

0-133 feet
133-266 feet
266-399 feet
399-533 feet
533-655 feet
-7.5 dB
-15 dB
-22.5 dB

E1 Mode

Digital Framer Mode

- The LIU can be disabled and bypassed to allow the MT9076 to be used as a digital framer
- Single phase NRZ or two phase NRZ modes are software selectable
- Line coding is software selectable

Phase Lock Loop

- Locks to a 4.096 MHz input clock, or to the 1.544 MHz / 2.048 MHz extracted clock
- IMA mode locks to 1,544 MHz or 2,048 MHz external clock
- Attenuates jitter from less than 2.5 Hz with a roll off of 20 dB/decade
- Attenuates jitter in the transmit or receive direction
- Intrinsic jitter less than 0.02 UI
- Meets the jitter characteristics as specified in AT&T TR62411
- Meets the jitter characteristics as specified in ETS 300 011
- Can be operated in Free-run, Line Synchronous or System Bus Synchronous modes

Access and Control

- MT9076 registers can be accessed via an 8-bit non-multiplexed parallel microprocessor port
- The parallel port can be configured for Motorola or Intel style control signals

Backplane Interfaces

- 2.048 Mbit/s or 8.192 Mbit/s ST-BUS
- IMA mode, 1.544 Mbit/s (T1) or 2.048 Mbit/s (E1) serial bus with asynchronous transmit and receive timing for Inverse MUX for ATM (IMA) applications. Slip buffers are bypassed and signaling is disabled.
- CSTo/CSTi pins can be used to access the receive/transmit signaling data
- RxDL pin can be used to access the entire B8ZS/HDB3 decoded receive stream including framing bits
- TxDL pin can be used to transmit data on the FDL (T1) or the Sa bits (E1)

T1/J1 Mode

- PCM-24 channels 1-24 are mapped to ST-BUS channels 0-23 respectively
- The framing-bit is mapped to ST-BUS channel 31

E1 Mode

- PCM-30 timeslots 0-31 are mapped to ST-BUS channels 0-31 respectively

Data Link

T1/J1 Mode

- Three methods are provided to access the datalink:
  1. TxDL and RxDL pins support transmit and receive datalinks
  2. Bit Oriented Messages are supported via internal registers
  3. An internal HDLC can be assigned to transmit/receive over the FDL in ESF mode

E1 Mode

- Two methods are provided to access the datalink:
  1. TxDL and RxDL pins support transmit and receive datalinks over the Sa4~Sa8 bits
  2. An internal HDLC can be assigned to transmit/receive data via the Sa4~Sa8 bits
- In transparent mode, if the Sa4 bit is used for an intermediate datalink, the CRC-4 remainder can be updated to reflect changes to the Sa4 bit

Access and Monitoring for National (Sa) Bits (E1 mode only)

- In addition to the datalink functions, the Sa bits can be accessed using:
  - Single byte register
  - Five byte transmit and receive national bit buffers
  - A maskable interrupt is generated on the change of state of any Sa bit

Three Embedded Floating HDLCs (HDLC0, HDLC1, HDLC2)

- Successive writes/reads can be made to the transmit/receive FIFOs at 160 ns or 80 ns intervals
- Flag generation and Frame Check Sequence (FCS) generation and detection, zero insertion and deletion
- Continuous flags, or continuous 1s are transmitted between frames
- Transmit frame-abort
- Transmit end-of-packet after a programmable number of bytes (up to 65,536 bytes)
- Invalid frame handling:
  - Frames yielding an incorrect FCS are tagged as bad packets
  - Frames with fewer than 25 bits are ignored
  - Frames with fewer than 32 bits between flags are tagged as bad packets
  - Frames interrupted by a Frame-Abort sequence remain in the FIFO and an interrupt is generated
  - Access is provided to the receive FCS
- FCS generation can be inhibited for terminal adaptation
- Recognizes single byte, dual byte and all call addresses
- Independent, 16-128 byte deep transmit and receive FIFOs
- Receive FIFO maskable interrupts for near full (programmable levels) and overflow conditions
- Transmit FIFO maskable interrupts for nearly empty (programmable levels) and underflow conditions
- Maskable interrupts for transmit end-of-packet and receive end-of-packet
- Maskable interrupts for receive bad-frame (includes frame abort)
- Transmit-to-receive and receive-to-transmit loopbacks are provided
- Transmit and receive bit rates and enables are independent

- Frame aborts can be sent under software control and they are automatically transmitted in the event of a transmit FIFO underrun

T1/J1 Mode

HDLC0

- Assignable to the ESF Facility Data Link or any channel
- Operates at 4 kbps, 56 kbps or 64 kbps

HDLC1, HDLC2

- Assignable to any channel
- Operates at 56 kbps or 64 kbps

E1 Mode

HDLC0

- Assigned to timeslot-0, bits Sa4~Sa8 or any other timeslot
- Operates at 4, 8, 12, 16 or 20 kbps depending on which Sa bits are selected for HDLC0 use

HDLC1, HDLC2

- Assigned to any timeslot except timeslot-0
- Operates at 64 kbps

Slip Buffers

T1/J1 Mode

Transmit Slip Buffer

- Two-frame slip buffer capable of performing a controlled slip
- Intended for rate conversion and jitter attenuation in the transmit direction
- Programmable delay
- Transmit slips are independent of receive slips
- Indication of slip direction

Receive Slip Buffer

- Two-frame slip buffer capable of performing a controlled slip
- Wander tolerance of 142 UI (92 μs) peak
- Indication of slip direction

E1 Mode

Receive Slip Buffer

- Two-frame slip buffer capable of performing a controlled slip
- Wander tolerance of 208 UI peak-to-peak
- Indication of slip direction

Jitter Attenuator FIFO

- A jitter attenuator FIFO is available on the transmit side in E1 mode and in IMA mode. The depth of the JA FIFO can be configured to be from16 bits deep to 128 bits deep in 16 bit increments

Inverse Mux for ATM (IMA) Mode

T1/J1 Mode

- Transmit and receive datastreams are independently timed
- The transmit clock synchronizes to a 1.544 MHz clock

E1 Mode

- Transmit and receive datastreams are independently timed
- Receive slip buffer is bypassed
- CAS and HDLCs are disabled

T1/J1 Mode

- Transmit and receive slip buffers are bypassed
- Robbed bit signaling and HDLCs are disabled

Framing Algorithm

T1/J1 Mode

- Synchronizes with D4 or ESF protocols
- Supports SLC-96 framing
- Framing circuit is off-line
- Transparent transmit and receive modes
- In D4 mode the Fs bits can optionally be cross checked with the Ft bits
- The start of the ESF multiframe can be determined by the following methods:
  - Free-run
  - Software reset
  - Synchronized to the incoming multiframe
- An automatic reframe is initiated if the framing bit error density exceeds the programmed threshold
- In transparent mode, no reframing is forced by the device
- Software can force a reframe at any time
- In ESF mode the CRC-6 bits can be optionally confirmed before forcing a new frame alignment
- During a reframe the signaling bits are frozen and error counting for Ft, Fs, ESF framing pattern and CRC-6 bits is suspended
- If J1 CRC-6 is selected the Fs bits are included in the CRC-6 calculation
- J1 CRC-6 and J1 Yellow Alarm can be independently selected
- Supports robbed bit signaling

E1 Mode

- MT9076 contains 3 distinct and independent framing algorithms
  1. Basic frame alignment
  2. Signaling multiframe alignment
  3. CRC-4 multiframe alignment
- Transparent transmit and receive modes
- Automatic interworking between interfaces with and without CRC-4 processing capabilities is supported
- An automatic reframe is forced if 3 consecutive frame alignment patterns or three consecutive non-frame alignment bits are received in error
- In transparent mode, no reframing is forced by the device
- Software can force a reframe at any time
- Software can force a multiframe reframe at any time
- E-bits can optionally be set to zero until CRC synchronization is achieved
- Optional automatic RAI
- Supports CAS multiframing
- Optional automatic Y-bit to indicate CAS multiframe alignment

Line Coding

T1/J1 Mode

- B8ZS or AMI line coding
- Pulse density enforcement
- Forced ones insertion

E1 Mode

- HDB3 or AMI line coding

Channel Associated Signaling

- ABCD or AB bits can be automatically inserted and extracted
- Transmit ABCD or AB bits can be passed via the microport or via the CSTi pin
- Receive ABCD or AB bits are accessible via the microport or via the CSTo pin
- Most significant or least significant CSTi/CSTo nibbles can be selected to carry signaling bits
- Unused nibble positions in the CSTi/CSTo bandwidth are tri-stated
- An interrupt is provided in the event of changes in any of the signaling bits
- Receive signaling bits are frozen if signaling multiframe alignment is lost

T1/J1 Mode

- Signaling bits can be debounced by 6 ms

E1 Mode

- Signaling bits can be debounced by 14 ms

Alarms

T1/J1 Mode

D4 Yellow Alarm, two types

1. Bit position 2 is zero for virtually every DS0 over 48ms
2. Two consecutive ones in the S-bit position of the twelfth frame

ESF Yellow Alarm, two types

1. Reception of 0000000011111111 in seven or more codewords out of ten (T1)
2. Reception of 1111111111111111 in seven or more codewords out of ten (J1)

Alarm Indication Signal (AIS)

- Declared if fewer than six zeros are detected during a 3 ms interval

Loss Of Signal (LOS)

- Analog Loss Of Signal is declared if the received signal is more than 20 dB or 40 dB below nominal for at least 1 ms
- Digital Loss Of Signal is declared if 192 or 32 consecutive zeros are received
- Output pin indicates LOS and/or loss of frame alignment

E1 Mode

Remote Alarm Indication (RAI)

- Bit 3 of the receive NFAS

Alarm Indication Signal (AIS)

- Unframed all ones signal for at least a double frame or two double frames

Timeslot 16 Alarm Indication Signal

- All ones signal in timeslot 16

Loss Of Signal (LOS)

- Analog Loss Of Signal is declared if the received signal is more than 20 dB or 40 dB below nominal for at least 1 ms
- Digital Loss Of Signal is declared if 192 or 32 consecutive zeros are received
- Output pin indicates LOS and/or loss of frame alignment

Remote Signaling Multiframe Alarm

- Y-bit of the multiframe alignment signal

Maskable Interrupts

T1/J1 Mode

- Change of state of terminal synchronization
- Change of state of multiframe synchronization
- Change of received bit oriented message
- Change of state of reception of AIS
- Change of state of reception of LOS
- Reception of a severely errored frame
- Transmit slip
- Receive slip
- Receive framing bit error
- Receive CRC-6 error
- Receive yellow alarm
- Change of receive frame alignment
- Receive line code violation
- Receive PRBS error
- Pulse density violation
- Framing bit error counter overflow
- CRC-6 error counter overflow
- Out of frame alignment counter overflow
- Change of frame alignment counter overflow
- Line code violation counter overflow
- PRBS error counter overflow
- PRBS multiframe counter overflow
- Multiframes out of alignment counter overflow
- Loop code detected
- One second timer
- Five second timer
- Receive new bit oriented message (debounced)
- Signaling (AB or ABCD) bit change

E1 Mode

- Change of state of basic frame alignment
- Change of state of multiframe synchronization
- Change of state of CRC-4 multiframe synchronization
- Change of state of reception of AIS
- Change of state of reception of LOS
- Reception of consecutively errored FASs
- Receive remote signaling multiframe alarm
- Receive slip
- Receive FAS error
- Receive CRC-4 error
- Receive E-bit
- Receive AIS in timeslot 16
- Line code violation
- Receive PRBS error
- Receive auxiliary pattern
- Receive RAI
- FAS error counter overflow
- CRC-4 error counter overflow
- Out of frame alignment counter overflow
- Receive E-bit counter overflow
- Line code violation counter overflow
- PRBS error counter overflow
- PRBS multiframe counter overflow
- Change of state of any Sa bit or Sa nibble
- Jitter attenuator within 4 bits of overflow/underflow
- One second timer
- Two second timer
- Signaling (CAS) bit change

HDLC Interrupts

- Go ahead pattern received
- End of packet received
- End of packet transmitted
- End of packet read from receive FIFO
- Transmit FIFO low
- Frame abort received
- Transmit FIFO underrun
- Receive FIFO full
- Receive FIFO overflow

Error Counters

- All counters can be preset or cleared under software control
- Maskable occurrence interrupt
- Maskable overflow interrupt
- Counters can be latched on one second intervals

T1/J1 Mode

- PRBS Error Counter (16-bit)
- CRC Multiframe Counter (16-bit)
- Framing Bit Error Counter (8-bit)
- Out of Frame Alignment Counter (4-bit)
- Change of Frame Alignment Counter (4-bit)
- Multiframes Out of Sync Counter (8-bit)
- Line Code Violation / Excessive Zeros Counter (16-bit)
- CRC-6 Error Counter (16-bit)

E1 Mode

- Errored FAS Counter (8-bit)
- E-bit Counter (10-bit)
- Line Code Violation / Excessive Zeros Counter (16-bit)
- CRC-4 Error Counter (16-bit)
- PRBS Error Counter (8-bit)
- CRC Multiframe Counter (8-bit)

Error Insertion

T1/J1 Mode

- Bipolar Violations
- CRC-6 Errors
- Ft Errors
- Fs Errors
- Payload Errors
- Loss of Signal Error

E1 Mode

- Bipolar Violations
- CRC-4 Errors
- FAS Errors
- NFAS Errors
- Payload Errors
- Loss of Signal Error

Loopbacks

- Digital loopback
- Remote loopback
- ST-BUS loopback
- Payload loopback
- Metallic loopback
- Local timeslot loopback
- Remote timeslot loopback

Per Timeslot Control

The following features can be controlled on a per timeslot basis:

- Clear Channel Capability (only used in T1/J1)
- Choice of sourcing transmit signaling bits from microport or CSTi pin
- Remote timeslot loopback
- Local timeslot loopback
- PRBS insertion and reception
- Digital milliwatt pattern insertion
- Per channel inversion
- Transmit message mode

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1.0 MT9076 Line Interface Unit (LIU)

1.1 Receiver

The receiver portion of the MT9076 LIU consists of an input signal peak detector, an optional equalizer with separate high pass sections, a smoothing filter, data and clock slicers and a clock extractor. Receive equalization gain can be set manually (i.e., software) or it can be determined automatically by peak detectors.

The output of the receive equalizer is conditioned by a smoothing filter and is passed on to the clock and data slicer. The clock slicer output signal drives a phase locked loop, which generates an extracted clock (Exclk). This extracted clock is used to sample the output of the data comparator.

In T1 mode, the receiver portion of the LIU can recover clock and data from the line signal for loop lengths of 0 - 6000 ft. of 22 AWG cable and tolerate jitter to the maximum specified by AT&T TR 62411(Figure 3).

The LOS output pin function is selectable to indicate any combination of loss of signal and/or loss of basic frame synchronization condition.

The LLOS (Loss of Signal) status bit indicates when the receive signal level is lower than the analog threshold for at least 1 millisecond, or when the number of consecutive received zeros exceeds the digital loss threshold.

In E1 mode, the analog threshold is either of -20 dB or -40 dB. The digital loss threshold is either 32 or 192.

In T1 mode, the receive LIU circuit requires a terminating resistor of 100 Ω across the device side of the receive 1:1 transformer.

In E1 mode, the receive LIU circuit requires a terminating resistor of either 120 Ω or 75 Ω across the device side of the receive 1:1 transformer.

The jitter tolerance of the clock extractor circuit exceeds the requirements of TR 62411 in T1 mode (see Figure 3) and G.823 in E1 mode (see Figure 4).

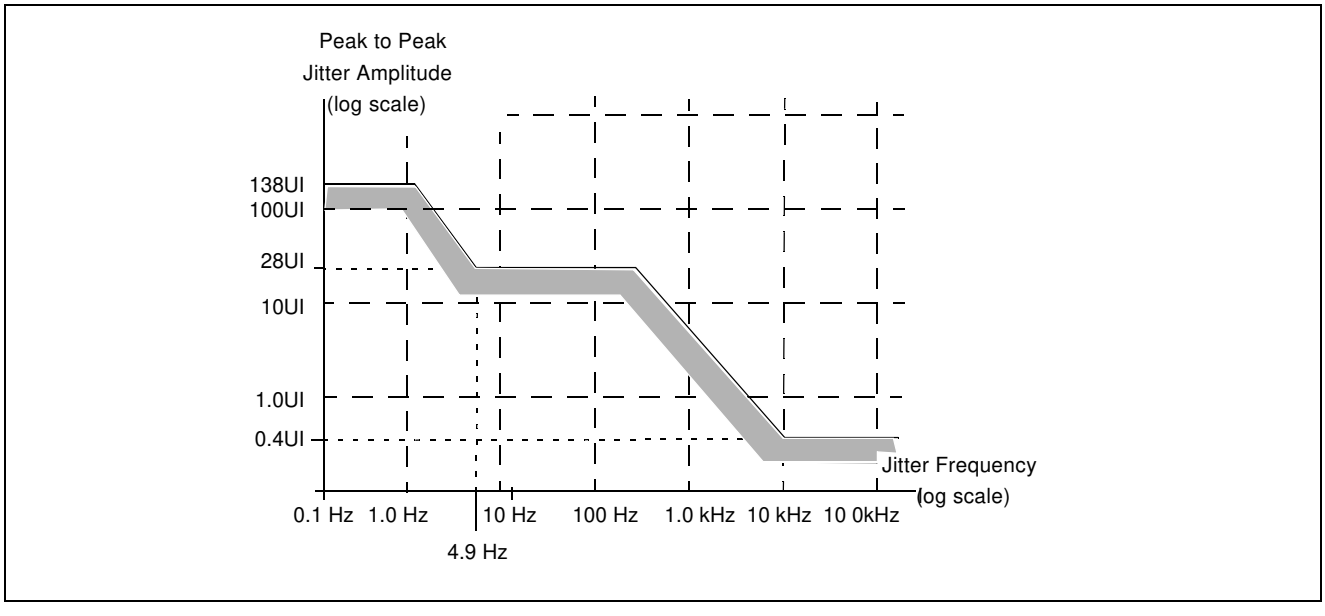


Figure 3 - Input Jitter Tolerance as Recommended by TR-62411 (T1)

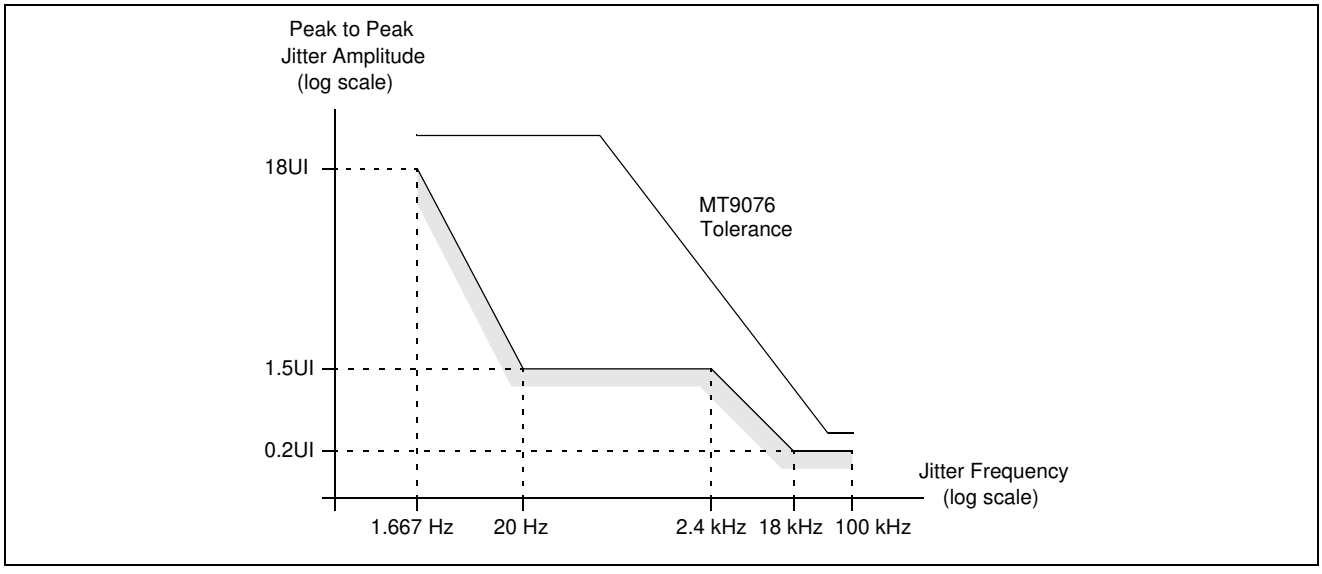


Figure 4 - Input Jitter Tolerance as Recommended by G.823 and ETSI 300 011 (E1)

1.2 Transmitter

The transmit portion of the MT9076 LIU consists of a high speed digital-to-analog converter and complementary line drivers.

When a pulse is to be transmitted, a sequence of digital values (dependent on transmit equalization) are read out of a ROM by a high speed clock. These values drive the digital-to-analog converter to produce an analog signal, which is passed to the complementary line drivers.

The complementary line drivers are designed to drive a 1:2.4 step-up transformer in T1 mode and either a 1:2 or 1:2.4 step-up transformer in E1 mode (see Figure 5). A 0.47 uF capacitor is required between the TTIP and the transmit transformer. Resistors RT (as shown in Figure 5) are for termination for transmit return loss. The values of RT may be optimized for T1 mode, E1 120 Ω lines, E1 75 Ω lines or set at a compromise value to serve multiple applications. Program the Tx LIU Control Word (page 02H, address 11H) to adjust the pulse amplitude accordingly.

Alternatively, the pulse level and shape may be discretely programmed by writing to the Custom Pulse Level registers (page 2, addresses 1CH to 1FH) and setting the Custom Transmit Pulse bit high (bit 3 of the Tx LIU Control Word). In this case the output of each of the registers directly drives the D/A converter going to the line driver. Table 1 and Table 2 show recommended transmit pulse amplitude settings.

In T1 mode, the template for the transmitted pulse (the DSX-1 template) is shown in Figure 6. The nominal peak voltage of a mark is 3 volts. The ratio of the amplitude of the transmit pulses generated by TTIP and TRING lie between 0.95 and 1.05.

In E1 mode, the template for the transmitted pulse, as specified in G.703, is shown in Figure 7. The nominal peak voltage of a mark is 3 volts for 120 Ω twisted pair applications and 2.37 volts for 75 Ω coax applications. The ratio of the amplitude of the transmit pulses generated by TTIP and TRING lie between 0.95 and 1.05.

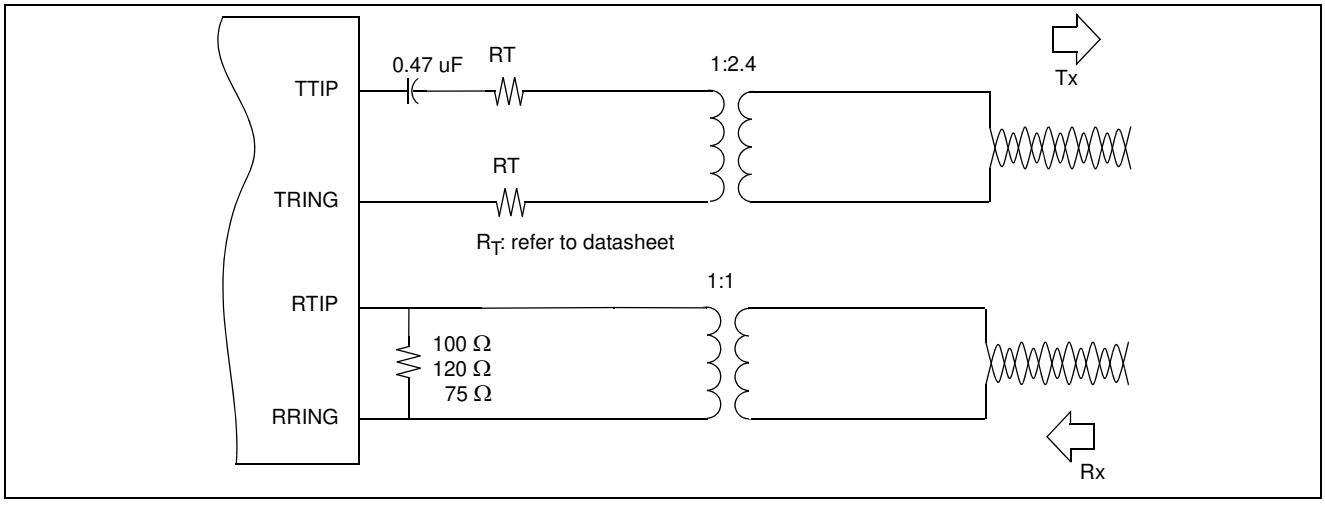


Figure 5 - Analog Line Interface

Notes:

1) Protection circuitry (i.e., voltage clamps, line fuses, common mode choke etc.) depends on the application and is not shown. For a reference design, refer to the evaluation board schematic.

2) The transformer shown is a Pulse Engineering T1144.

Name	Functional Description
TXL2-0	**Transmit Line Build Out 2 - 0**. Setting these bits shapes the transmit pulse as detailed in the table below:

TXL2	TXL1	TXL0	Line Build Out
0	0	0	0 to 133 feet/ 0 dB
0	0	1	133 to 266 feet
0	1	0	266 to 399 feet
0	1	1	399 to 533 feet
1	0	0	533 to 655 feet
1	0	1	-7.5 dB
1	1	0	-15 dB
1	1	1	-22.5 dB

After reset these bits are zero.

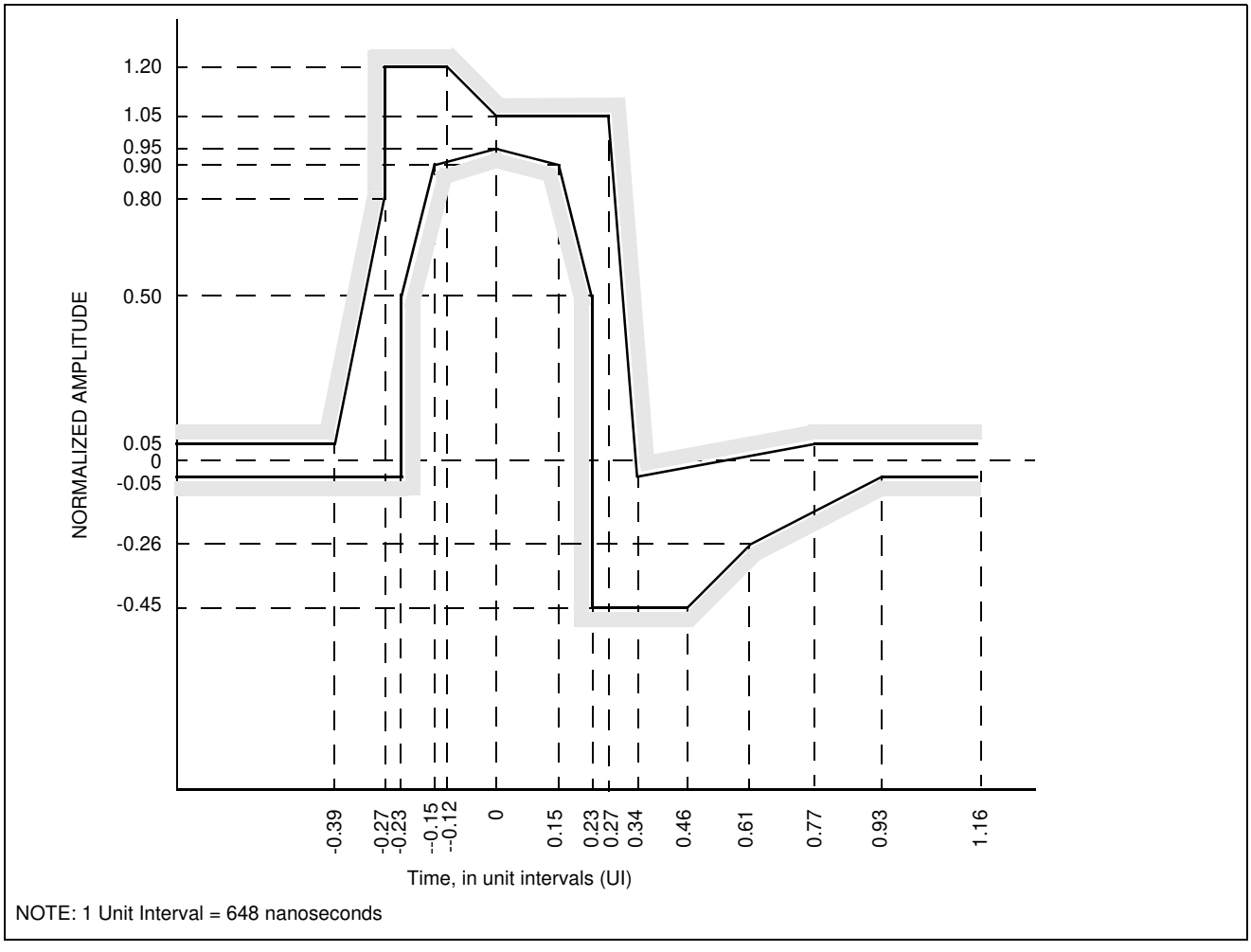
Table 1 - Transmit Line Build Out (T1)

	Name	Functional Description
WR	**Winding Ratio.** Set this pin low if a 1:2.4 transformer is used on the transmit side. Set this pin high if a 1:2 transformer is used.	
TX2-0	**Transmit pulse amplitude.** Select the TX2 –TX0 bits according to the line type, value of termination resistors (RT), and transformer turns ratio used.	

TX2	TX1	TX0	Line Impedance (ohms)	RT(ohms)	Transformer Ratio	WR (bit 7)
0	0	0	120	0	1:2.4	0
0	0	1	120	6.8	1:2.4	0
0	1	0	120	6.8	1:2.4	0
0	1	1	75	5.1	1:2.4	0
1	0	0	-	-	-	-
1	0	1	75	6	1:2	1
1	1	0	75	6	1:2	1
1	1	1	75	5.1	1:2.4	0

After reset, these bits are zero.

Table 2 - Transmit Pulse Amplitude (E1)



NOTE: 1 Unit Interval = 648 nanoseconds

Figure 6 - Pulse Template (T1.403)(T1)