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MT90812

Integrated Digital Switch (IDX)

Advance Information

Features

- 192 channel x 192 channel non-blocking switching
- 2 local bus streams @ 2Mb/s supports up to 64 channels
- In TDM mode, the expansion bus supports up to 128 channels at 8.192 Mb/s
- Rate conversion capability between local and expansion bus streams
- Integrated conference bridge, supporting 15 parties over 5 bridges
- Integrated PLL
- Frequency Shift Keying (FSK) 1200 baud transmitter, meeting Bell 202 or CCITT V.23 standards
- 32 channel dual tone generator, including 16 standard DTMF tones and tone ringer
- Expansion bus in IDX Link mode, allows the interconnection of up to 4 IDX devices
- Programmable per channel gain control from +3 to -27dB, increments of 1dB for output channels
- Supervisory signalling cadence detection capability
- HDLC resource allocator
- D-channel buffering of message information
- C-channel access for control and status registers
- Provides both variable and constant delay modes
- Parallel microprocessor port, compatible to Intel and Motorola and National CPU's
- Supports both A-law or u-law operation
- Supports both ST-BUS, GCI and HMVIP framing formats

Applications

- Computer Telephony Integration (CTI)
- Key Telephone Systems
- Private Branch Exchange (PBX) Systems

Ordering Information

MT90812AP	68 Pin PLCC	Tubes
MT90812AL	64 Pin MQFP	Trays
MT90812APR	68 Pin PLCC	Tape & Reel
MT90812AP1	68 Pin PLCC*	Tubes, Bake & Drypack
MT90812AL1	64 Pin MQFP*	Trays
MT90812APR1	68 Pin PLCC*	Tape & Reel, Bake & Drypack

*Pb Free Matte Tin
-40 to 85°C

Description

By integrating key functions needed in voice telecom application, the Integrated Digital Switch (IDX) provides a solution-on-a-chip for key telephone systems, PBX applications or CTI designs. Figure 2 shows a typical configuration.

The MT90812 provides non-blocking timeslot interchange capability for B, C and D channels, up to a maximum of 192 channels. It offers conference call capability for 15 parties over a maximum of 5 conference bridges. With its integrated PLL, the MT90812 provides the necessary clocks to support peripheral devices, such as codecs or interconnected IDX devices. Integrated into the IDX is the capability to detect supervisory signalling and to generate FSK 1200-baud signals. In addition, an integrated digital tone generator produces continuous dual tones, including standard DTMF.

With its programmable gain control, the IDX allows users to use codecs without gain control and also centrally manage conference calls.

To support both small and large switching platforms, a built-in expansion Bus allows the interconnection of up to 4 IDX devices or external components such as digital switches. When 4 IDX devices are interconnected, the array is capable of switching 256 channels (64x4), handling 60 conference parties (15x4) and generating additional tones including programmable ones. Other functions are also increased in this configuration. The functional block diagram is shown in Figure 1.

An evaluation board, MEB90812, is available complete with software and a user manual, which demonstrates the layout of a typical application board and facilitates the use of the MT90812, and peripheral devices such as Zarlink's DNIC products.
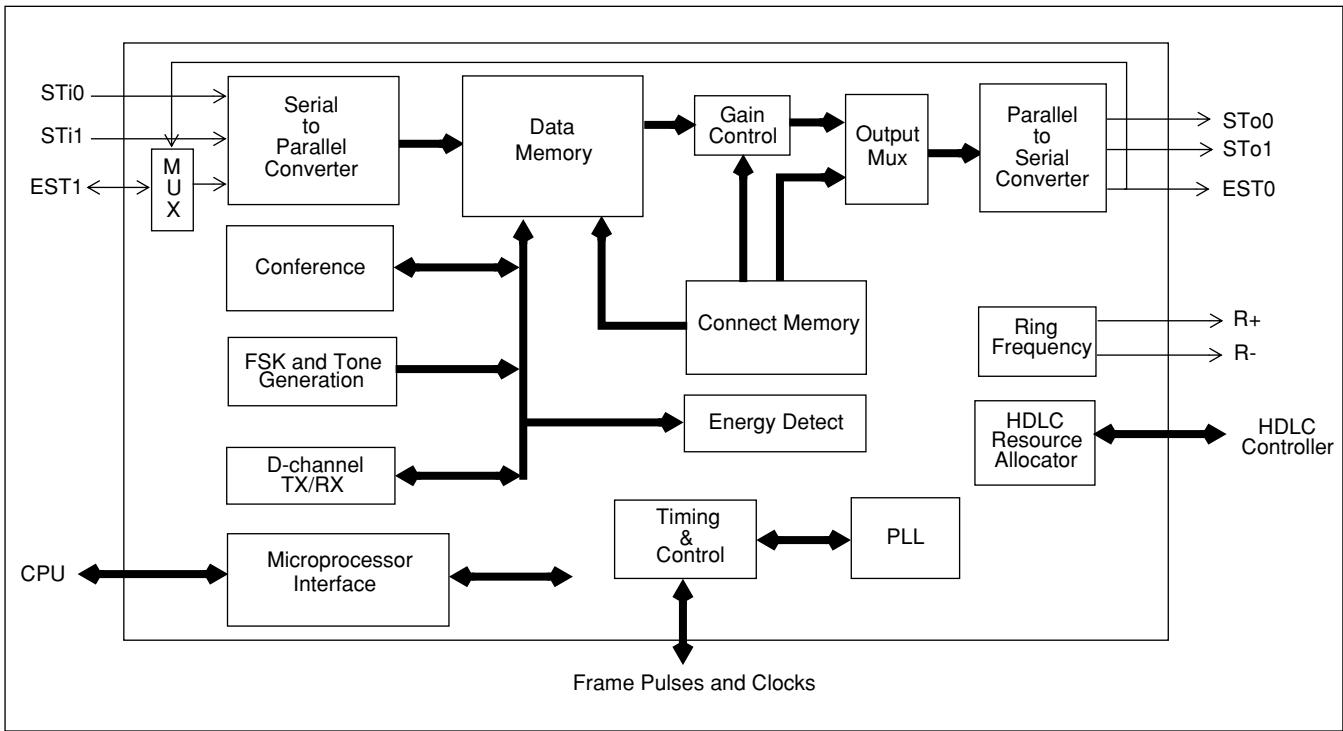
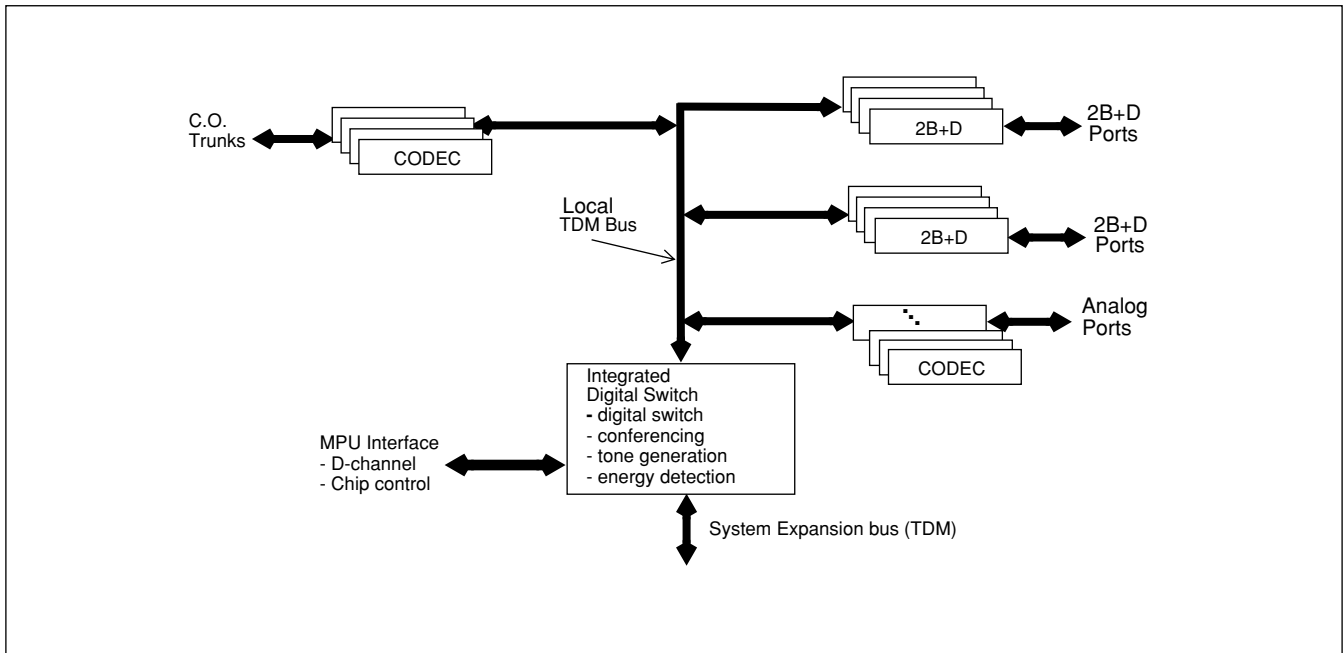**Figure 1 - Functional Block Diagram**
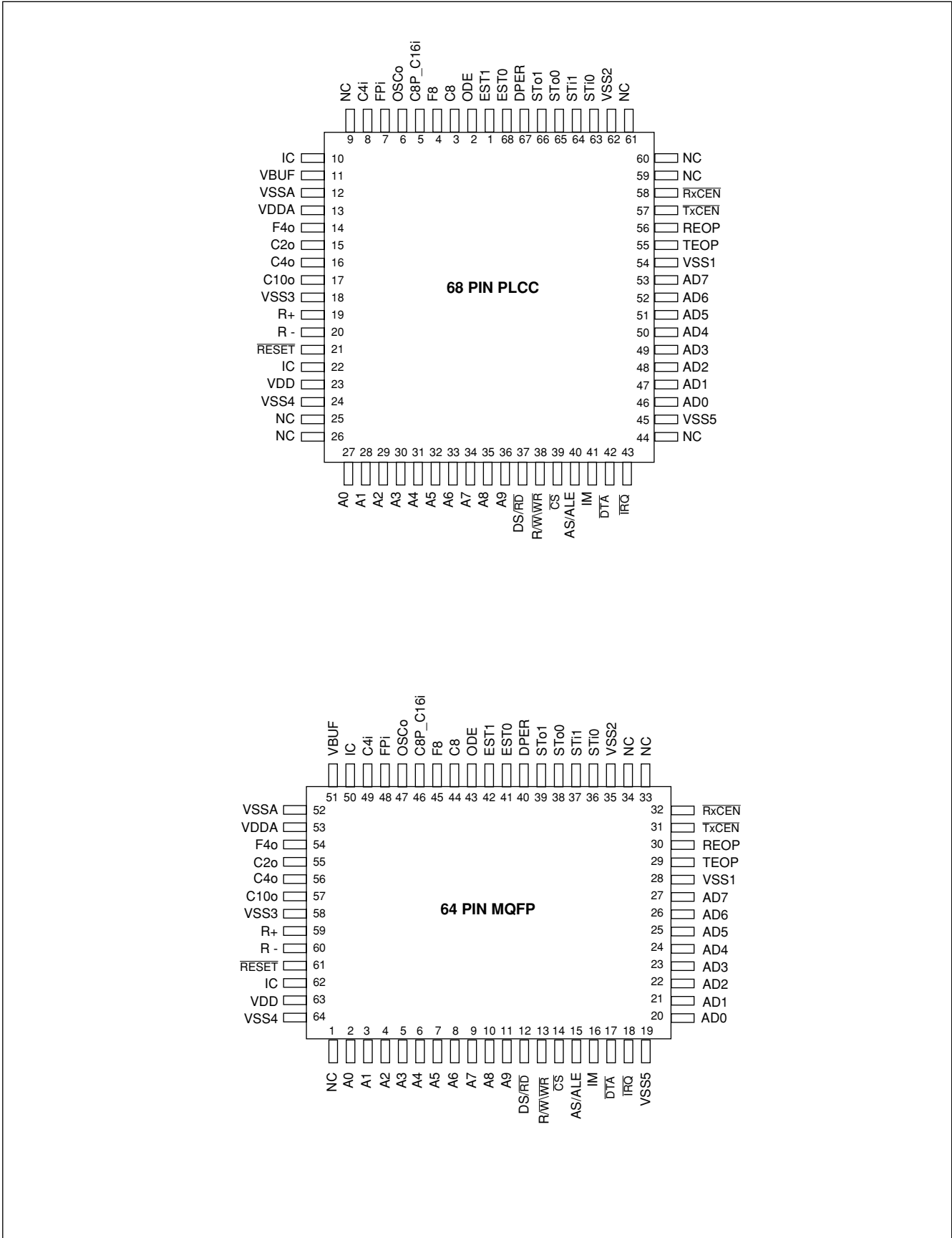

Figure 2 - System Blocks - Typical Configuration

Figure 3 - Pin Connections

Pin Description

Pin #		Name	Description
64 Pin MQFP	**68 Pin PLCC**		
1	25-26	NC	**No Connect**. Ground
2-11	27-36	A0 - A9	**Address 0 - 9 (Input)**. When non-multiplexed CPU bus is selected, these lines provide the A0 - A9 address lines to IDX internal memories.
12	37	DS/$\overline{RD}$	**Data Strobe/$\overline{Read}$ (Input)**. For Motorola multiplexed bus operation, this active high DS input works with $\overline{CS}$ to enable the read and write operations. For Motorola non-multiplexed CPU bus operation, this input is $\overline{DS}$. This active low input works in conjunction with $\overline{CS}$ to enable the read and write operations. For Intel/National multiplexed bus operations, this input is $\overline{RD}$. This active low input sets the data bus lines (AD0-AD7) as outputs.
13	38	R/$\overline{W}$ \ $\overline{WR}$	**Read/$\overline{Write}$ \ $\overline{Write}$ (Input)**. In case of non-multiplexed and Motorola multiplexed buses, this input is Read/$\overline{Write}$. This input controls the direction of the data bus lines (AD0 - AD7) during a microprocessor access. For Intel/National multiplexed bus, this input is $\overline{WR}$. This active low signal configures the data bus lines (AD0-AD7) as inputs.
14	39	$\overline{CS}$	**Chip Select (Input)**. Active low input enabling a microprocessor read or write of internal memories.
15	40	AS/ALE	**Address Strobe or Latch Enable (Input)**. This input is only used if multiplexed bus is selected via IM input pin.
16	41	IM	**CPU Interface Mode (Input)**. If High, this input sets the device in the multiplexed microprocessor mode. If this input is grounded, the device resumes non-multiplexed CPU interface.
17	42	$\overline{DTA}$	**Data Acknowledgment (Open Drain Output)**. This active low output indicates that a data bus transfer is complete. A 10Kohm pull-up resistor is required at this output.
18	43	$\overline{IRQ}$	**Interrupt Request Output (Open Drain Output)**. This active low output notifies the controlling microprocessor of an interrupt request. It goes Low only when the bits in the Interrupt Enable Register are programmed to acknowledge the source of the interrupt as defined in the Interrupt Status Register.
-	44	NC	**No Connect**. Ground
19	45	VSS5	**Ground**.
20-27	46-53	AD0 - AD7	**Data Bus (Bidirectional)**. These pins provide microprocessor access to the internal memories. In the multiplexed bus mode, these pins also provide the input address to the internal Address Latch circuit.
28	54	VSS1	**Ground**.
29	55	TEOP	**Transmit End of Packet (Input)**. This is a strobe that is generated by the HDLC controller chip for one bit period during the last bit of the closing flag of the transmit packet.
30	56	REOP	**Receive End of Packet (Input)**. A receive packet will normally be terminated when the HDLC controller asserts the REOP strobe for one bit period, one bit time after the closing flag is received.
31	57	$\overline{TxCEN}$	**Transmit Clock Enable (Output)**. The HDLC transmitter is controlled by the IDX-generated Transmit Clock Enable signal, $\overline{TxCEN}$.
32	58	$\overline{RxCEN}$	**Receive Clock Enable (Output)**. The HDLC receiver is controlled by the IDX-generated Receive Clock Enable signal, $\overline{RxCEN}$.

Pin Description (continued)

Pin #		Name	Description
64 Pin MQFP	**68 Pin PLCC**		
33-34	59-61	NC	**No Connect**. Ground
35	62	VSS2	**Ground**.
36-37	63-64	STi0-1	**Serial TDM input streams 0 and 1 (Input)**. Serial data input streams which have data rates of 2.048 Mb/s with 32 channels.
38-39	65-66	STo0-1	**Serial TDM output streams 0 and 1 (Three-state output)**. Serial data output streams which have data rates of 2.048 Mb/s with 32 channels.
40	67	DPER	**D-Channel Input in ST-BUS format (Input)**. The MT8952B CDSTo stream containing formatted D-channel data.
41	68	EST0	**Expansion Bus Serial data stream 0 (Three-state output/input)**. This is a bi-directional pin at 8.192 Mb/s in IDX Link mode. In TDM Link mode this is a 2.048, 4.096 or 8.192 Mb/s output stream.
42	1	EST1	**Expansion Bus Serial data stream 1 (Three-state output/input)**. This is a bi-directional pin at 8.192 Mb/s in IDX Link mode. In TDM Link mode this is a 2.048, 4.096 or 8.192 Mb/s input stream.
43	2	ODE	**Output Device Enable (Input)**. This is the output enable input for the serial outputs. If this input is low, STo0, STo1, EST0, EST1 are high impedance. If this input is high, each channel may still be put into high impedance state by using per channel control bit in the Connection Memory.
44	3	C8	**Clock 8.192 (Bidirectional)**. As an input this signal is used for Expansion bus and/or internal clock source at 8.192 MHz depending on the timing mode selected. As an output this signal is an 8.192 MHz output clock locked to the reference input signal.
45	4	F8	**Frame Pulse for 8.192 MHz (Bidirectional)**. As an input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI interface specifications. As an output is an 8 KHz frame pulse that indicates the start of the active frame. Either F8 or FPi are used for frame synchronization depending on the timing mode selected
46	5	C8P_C16i	**Oscillator Master Clock (CMOS Input)**. For crystal operation, a 8.192MHz crystal is connected to this pin from OSCo. For clock oscillator operation, this pin is connected to a clock source. The clock source of either 8.192 MHz or 16.384 MHz can be used as selected in the Timing Control Register (TC).
47	6	OSCo	**Oscillator Master Clock (CMOS Output)**. For crystal operation, a 8.192MHz crystal is connected from this pin to C8P_C16i. For clock oscillator operation, this pin is left unconnected.
48	7	FPi	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI interface specifications. Either F8 or FPi are used for frame synchronization depending on the timing mode selected.
49	8	C4i	**Clock 4.096 MHz (Input)**. This input is the 4.096 MHz clock input.
-	9	NC	**No Connect**. Ground
50-51	10-11	IC	**Internal Connect**. Open.
52	12	VSSA	**Analog Ground**.
53	13	VDDA	**+5 Volt Power Supply (Analog)**.

Pin Description (continued)

Pin #		Name	Description
64 Pin MQFP	68 Pin PLCC		
54	14	F4o	**Frame Pulse for 4.096 MHz (Output)**. This is an 8 KHz output frame pulse that indicates the start of the active ST-Bus/GCI frame. The pulse width is based upon the period of the C4o clock.
55	15	C2o	**Clock 2.048 MHz (Output)**. This output is an 2.048 MHz output clock locked to the reference input signal.
56	16	C4o	**Clock 4.096 MHz (Output)**. This output is an 4.096 MHz output clock locked to the reference input signal.
57	17	C10o	**Clock 10.24MHz (Output)**. This output is a 10.24 MHz clock locked to the reference input signal.
58	18	VSS3	**Ground**.
59	19	R+	**Ringing Generator +ve Output**. This output is a 16, 20, 25 or 50 Hz square wave.
60	20	R-	**Ringing Generator -ve Output**. Square wave output 180 degrees out of phase with R+.
61	21	$\overline{\text{RESET}}$	**Device Reset (Input).** When 0, reset the device internal counters, registers and tri-states STo0, STo1, EST0, EST1 and data outputs from the microport.
62	22	IC	**Internal Connection**. Tie to Vss for normal operation.
63	23	VDD	**+5 Volt Power Supply**.
64	24	VSS4	**Ground**.

Overview

The MT90812 Integrated Digital Switch (IDX) provides the integration of several functions required in a telecom application. The IDX includes a digital switch for switching up to 192 x 192 channels, five conference bridges, a DTMF/supervisory-tone bus and two digital energy detector circuits for trunk call progress tone detection. There are two 2.048 Mbit/s Serial Links and an Expansion Bus that can operate at 2.048, 4.096 or 8.192 Mb/s. A digital Frequency Shift Keying (FSK) transmitter, compatible to Bell 202 or CCITT V.23 1200 baud is provided. D-Channel control is realized by microprocessor access to the MT90812. D-Channel messages are relayed to and from the 2B+D line transceivers via the local TDM link. In D-channel Basic Receive/Transmit mode a 32 byte buffer is provided for each of the transmit and receive directions, and these can be independently assigned to specific D-channels. Alternatively, the HDLC controller mode can be selected, providing an interface to the MT8952 HDLC. The HDLC controller mode provides the necessary control signals to operate the MT8952 HDLC in external timing mode, allowing multiplexing of the MT8952 over the local TDM links.

The MT90812 also provides an interface to the Expansion Bus capable of linking a number of MT90812 devices together directly or in a larger matrix through other digital switches. Each MT90812 can route any of the 64 channels associated with the local TDM streams onto the Expansion Bus. Thus, system growth is easily achieved via the addition of a MT90812 device onto the Expansion Bus. Very little hardware overhead is required to enable cost effective system growth.

In a multi-IDX system functions including Conferencing, Tone generation, Supervisory Signal Detection, D-channel Receiver and Transmitter, Tone Ringer and FSK Transmitter can be shared across the system. For example, in a system consisting of four MT90812 devices, 20 three party conferences can be supported, independent of which MT90812 the party originated. For Tone Generation, 6 programmable tones per MT90812 translates to 24 programmable tones in a four MT90812 system, all of which can be routed to any channel in the system.

1.0   **Functional Description**

The functional block diagram of Fig. 1 depicts the main operations performed by the MT90812. The integrated digital switch has three TDM streams. The two local TDM serial streams, STi/o0 and STi/o1, operate at 2048kbit/s and are arranged in 125us wide frames each containing 32 8-bit channels. The third TDM stream, comprised of EST0 and EST1 can be used as an additional serial stream at 2.048, 4.096 or 8.192 Mb/s, supporting 32, 64 or 128 channels, respectively.

The expansion bus, EST0/1 operates in two modes, TDM Link and IDX Link modes. IDX Link mode allows multiple MT90812 devices to be linked together very efficiently. In IDX Link mode, the incoming data on the local TDM streams of each MT90812 is transferred onto the expansion bus to enable switching channels between a maximum of four MT90812 devices. For TDM Link mode, the expansion bus is configured as a TDM serial stream which can run at 2.048, 4.096 or 8.192 Mb/s. In TDM Link mode, the MT90812 can be connected to more peripheral devices or to other digital switches (i.e. MT8980/1/2 or MT8985/6) to support larger matrices of MT90812 devices.

The MT90812 can switch data from channels on the local and expansion input streams to channels on the local and expansion output streams. The controlling microprocessor can simultaneously read channels on TDM inputs or write to channels on TDM outputs (Message Mode). To the microprocessor, the MT90812 looks like a memory peripheral. The microprocessor can write to the MT90812 to establish switched connections between input TDM channels and output TDM channels, or to transmit messages on output TDM channels. By reading from the MT90812, the microprocessor can receive messages from TDM input channels or check which switched connections have already been established.

The MT90812 provides conference call capability and supports a total of 15 parties, distributed over a maximum of 5 conferences. (i.e. 1x15 parties, 3x5 parties, 5x3 parties etc.). Conference parties can be from any of the incoming channels on the local or expansion TDM streams.

Gain Control is provided on the outgoing channels, with a range of +3 to -27 dB in steps of 1dB, as well as -∞ dB. If a channel is in a conference, incoming and/or outgoing gain control is provided. Conference incoming gain also ranges from +3 to -27 dB in steps of 1dB, as well as -∞ dB. Conference outgoing gain can range from 0 to -9 dB in steps of 3 dB.

A tone source of 32 dual tones is generated from the tone generator block and stored in Data Memory. Outgoing gain control of +3 to -27 dB in steps of 1dB, as well as -∞ dB, is provided for each tone. Seven of the thirty-two tones are programmable in frequency. The 32 locations can be switched to outgoing channels or accessed by the microprocessor.

A phase coherent FSK transmitter generates two output frequencies, representing the 'marks' and 'spaces', selectable to Bell 202 or CCITT V.23 standards at 1200 baud. The FSK transmitter output is a PCM coded signal that can be directed to any outgoing local TDM channel.

Two energy detect blocks provide monitoring capability of supervisory signalling for any of the TDM channels. D-Channel access is provided to link the microprocessor to the transceivers. There are two modes of message formats that can be selected. The D-Channel Basic Receive Transmit (DBRT) mode provides basic formatting of the data, which includes start and stop signalling and parity checking. In DBRT mode there are RX and TX buffers, 32 bytes in length, which can be allocated to any of the incoming/outgoing channels of the TDM streams. The HDLC mode provides a control interface to facilitate the multiplexing of an external HDLC controller (MT8952) over any of the local TDM streams' D-Channels.

C-Channel access for control of ST-BUS family of devices (e.g. MT9160B, MT9171/72, MT8930, MT8910) is provided through Message Mode.

Each of the programmable parameters within the functional blocks are accessed through a parallel microprocessor port compatible with CPU non-multiplexed bus and Intel[R], Motorola[R] and National[R]

multiplexed bus specifications. The MT90812 can operate in either A-Law or μ–Law as defined in Control register as specified in section "Control Register (CTL)" on page 54.

2.0   Local TDM Streams

There are two local serial Time Division Multiplexed (TDM) streams. These streams at STi/o0 and STi/o1 provide a link between the MT90812 and other peripheral devices, including those in the ST-BUS family (e.g. MT9160B, MT9171/72, MT8930, MT8910). The two serial streams operate at 2.048 Mbit/s and are arranged in 125us wide frames, each comprising 32 8-bit channels. Refer to Section 9.2, "Serial Data Interface Timing".

The MT90812 can support Primary Rate or Basic Rate devices. Using the Basic Rate devices (e.g. MT9171/72 DNIC) in dual port mode the D-Channel should be assigned to STi/o1 streams. D-channel signalling support is provided for any timeslot on the STi/o1 streams for the HDLC Controller mode. The DBRT can access any timeslot and stream. Refer to "D-Channel Signalling Support" on page 30 and "Local TDM Channel Assignment" on page 76.

3.0   Expansion Bus

The expansion bus operates in 2 modes, IDX Link and TDM Link modes. The modes will be described in the following sections. Section 24.1 describes the timing references used for both Expansion bus modes.
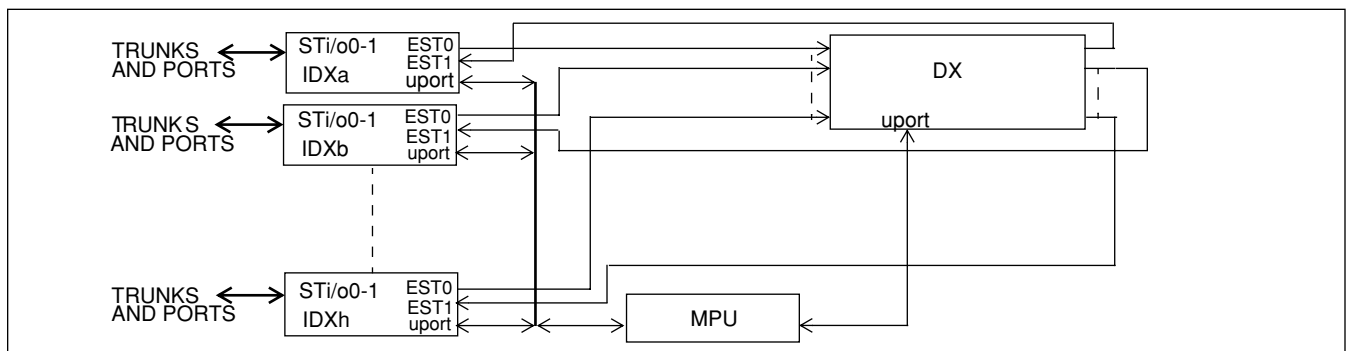
3.1   TDM Link Mode

In this mode, the expansion bus at EST0 and EST1, are regular output and input serial streams, respectively. They operate at either 2.048, 4.096 or 8.192 Mbit/s. Refer to Fig. 4.
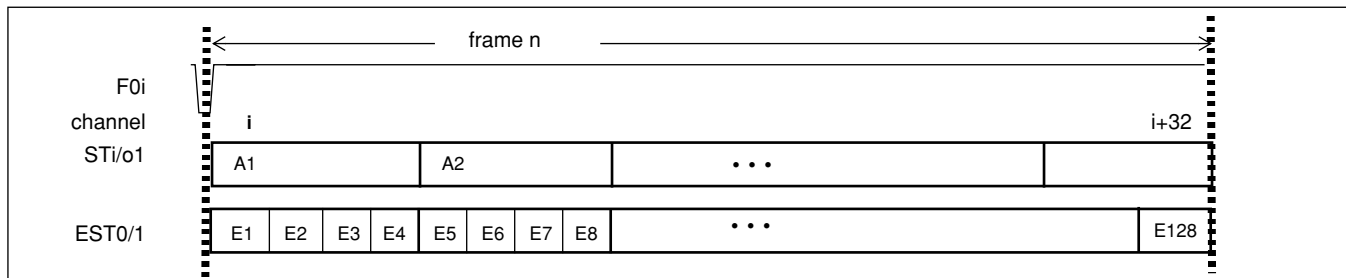
Figure 4 - Expansion Bus (TDM Link mode)

At 2.048Mb/s, the first block of 32 locations of Data Memory reserved for the expansion bus are used. The 32 incoming channels on EST1 are placed in expansion block 1 of Data Memory. At 4.096 Mb/s the 64 bytes are utilized in expansion block 1 and 2. At 8.192Mb/s all 128 locations of Data Memory reserved for the expansion bus are used. Refer to the description of the memory allocation in Section 5, "Address Memory Map".

This mode allows linking larger matrices of MT90812 devices together. For example, at 2.048 Mb/s, eight MT90812 devices can be connected together via a MT8980D (DX) switch, as shown in Fig. 5.

Figure 5 - Eight IDX Configuration using Expansion Bus TDM Link mode

Each of the 32 channels of the 8 streams connecting the DX and IDX devices can be switched to any outgoing channel and stream. This provides switching across all eight of the MT90812 devices.

3.2   IDX Link Mode

In IDX Link mode the expansion bus allows up to four IDX devices to be connected together as shown in Fig. 6. The data flow between each MT90812 is supported on EST0 and EST1, two serial streams which operate at 8.192Mbit/s and each consist of 128 8-bit channels. The four MT90812 devices are labelled A, B, C and D. TDM Link Mode can be used to link more than four MT90812 devices, refer to Section 3.1.

The expansion bus channel assignment for EST0 and EST1 in IDX Link mode is shown in Fig. 7. For the EST0 stream, each of the four MT90812 devices place data into 32 timeslots and read in data from the other 96 timeslots. The EBUS position, as defined in section "Control Register (CTL)" on page 54, designates which timeslots the MT90812 writes to and which timeslots it reads from. For example, IDX A would output Channel 1 at the timeslot shown as A1 in Fig. 7 and input data during timeslots B1, C1 and D1.

For the EST1 stream, each MT90812 reads in 32 channels and can output data to the other 96 channels. Which channels are read are also determined from the EBUS position bits. For example, IDX A will read data during timeslots EA1, EA2,... EA32.

Each MT90812 will receive a total of 128 channels from the two streams EST0 and EST1. For IDX A, the 96 channels, B1-B32, C1-C32, D1-D32 will be taken from EST0 and 32 channels EA1-EA32 will be taken from EST1.

A description of programming the switch in IDX Link mode is given in "Connection Memory" on page 10. The Data Memory allocation is described in Section 5, "Address Memory Map".

On power up, the EBUS is set to high impedance and the EBUS position bits must be programmed to avoid any contention on the two streams.
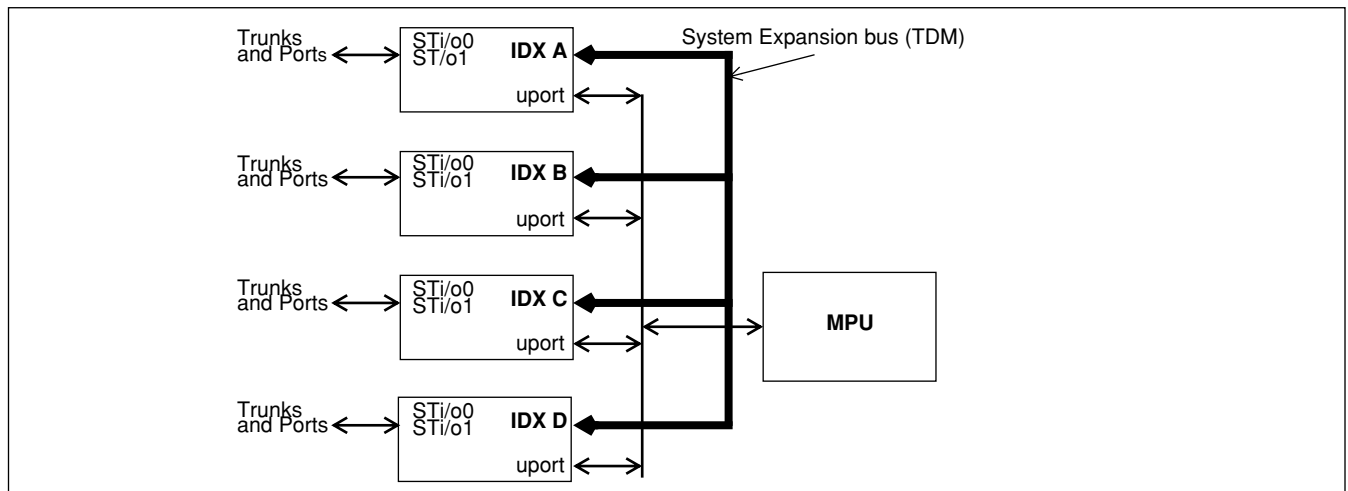
Figure 6 - Four IDX Configuration using Expansion Bus IDX Link mode
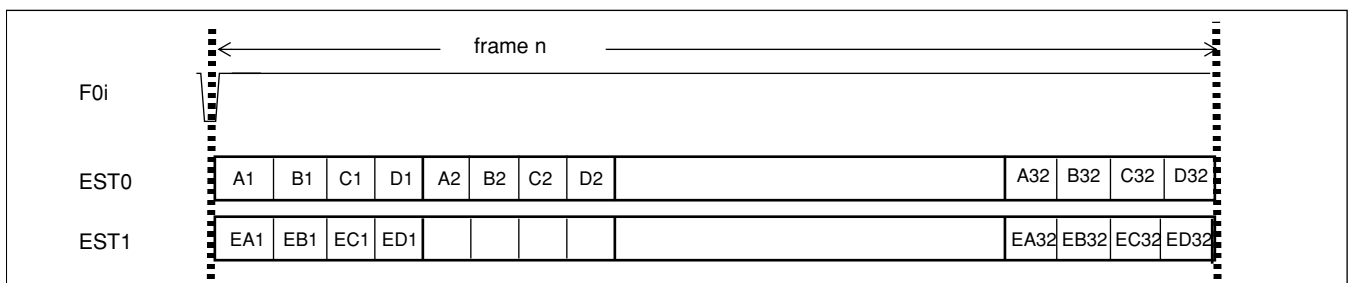
Figure 7 - Expansion Bus - IDX Link mode

4.0   Switching

The switching function of the MT90812 is described in four parts:

- How incoming data from the Local TDM streams are transferred to Data Memory.
- How incoming data from the Expansion Bus is transferred to Data Memory for both IDX Link and TDM Link modes.
- Connect Memory and Data Memory structure.
- How output data can be switched from either Data Memory or Connect Memory.

Each will be described below with reference to Figure 1 - "Functional Block Diagram". This is followed by a more detailed description of Connect Memory in Section 4.2.

4.1   Switching Functions

4.1.1   Data Transfer from Local TDM Streams to Data Memory

The serial data incoming to the MT90812 is converted into parallel format (8 bits per channel) with the parallel to serial converters for both the Local and Expansion Bus streams. This data is written to consecutive locations in Data Memory.

The two local TDM streams, STi/o0 and STi/o1, operate at 2.048 Mb/s for a total of 64 channels per frame. The 64 bytes are stored in the Local Data Memory page in locations 00_H to $3F_H$. Refer to the Memory Map in Table 2.

4.1.2   Data Transfer from the Expansion Bus to Data Memory

In TDM Link mode, the expansion bus rate can be set to 2.048, 4.096 or 8.192 Mb/s, where the number of channels used for the expansion bus stream are 32, 64 and 128, respectively. In Data Memory, 128 bytes are reserved in the Expansion Data Memory page. If there are only 32 or 64 channels (i.e. at 2.048 or 4.096 Mb/s) then the first 32 or 64 locations of the 128 reserved for the expansion bus are used.

In IDX Link mode, the Expansion Bus rate is set to 8.192 Mb/s. There are 96 channels incoming from EST0 and 32 channels from ESTI, for a total of 128 incoming channels read into Expansion Data Memory.

4.1.3   Connect Memory and Data Memory Structure

There are 64 locations in Local Data Memory reserved for the incoming channels of the Local TDM streams and 128 locations in Expansion Data Memory, for the incoming channels of the Expansion Bus. In addition, there are another 32 locations of Local Data Memory reserved for the Tone generator. Refer to the Memory Map in Table 2.

For each output channel there is an associated Connect Memory location. There are 128 locations for the outgoing expansion bus channels and 64 for the local TDM streams.

4.1.4   Switching Output Data from Either Data Memory or Connect Memory

When the MT90812 switches data from input channels to outgoing channels, the address for Data Memory is read from the Connection Memory location corresponding to the desired output channel. In Message Mode, output data is read directly from the Connection Memory location corresponding to the output channel. The details for setting up the connections are given in the following section.

4.2   Connection Memory

The use of Connection Memory in the MT90812 is described in three parts:

- Connection Memory usage for Switch Connection or Message Mode

- Control Register and the use of Connection Memory
- Connect Memory Configurations for Expansion Bus Modes

Each will be described below. A full description of addressing memory in the MT90812 is given in "Address Memory Map" starting on page 12. Refer to Section 21.0 for a definition of the Connection Memory High and Low bits.

4.2.1 Connection Memory Usage for Switch Connection or Message Mode

Locations in the Connection Memory, which is split into high and low parts, are associated with particular TDM output streams. When a channel is due to be transmitted on an TDM output stream, the data for the channel can either be switched from an TDM input stream or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory.

The Data Memory address corresponds to the channel on the input stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory High determines whether individual output channels are in Message Mode, controls individual output channels to go into a high-impedance state and specifies the gain for each outgoing channel.

4.2.2 Connection Memory Select

If the microport is operating in multiplexed mode, addressing the high and low sections of Connection Memory is done by setting the Memory Select Bits in Control Register. If the microport is operating in non-multiplexed mode, addressing the high and low sections of connection memory is done by setting the external address bits A9,A8,A7. Refer to "Address Memory Select Register (AMS)" on page 53, and "Microprocessor Port" on page 49.

The Control Register also consists of mode control bits that allows the chip to broadcast messages on all TDM output channels (i.e., to put every channel into Message Mode). Mode control bit 5, CT2:MSG bit, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the TDM output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

If CAR:MSG bit is 0, then bits 2 and 0 of each Connection Memory High location function as follows. If CMH:bit 2 is set to 1, the associated TDM output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, the serial input is transmitted and the Connection Memory Low defines the associated input stream and channel where the byte is to be found.

If the ODE pin is low, then all serial outputs are high-impedance. If the ODE pin is high and CAR:MSG bit is 1, then all outputs are active. If the ODE pin is high and CAR:MSG bit is 0, then the bit 0 in the Connection Memory High location enables the output driver for the corresponding individual output stream and channel. CMH:bit 0=1 enables the driver and CMH:bit 0=0 disables it.

4.2.3 Connect Memory Configurations for Expansion Bus Modes

In TDM Link mode, the 128 Connect Memory locations reserved for the expansion bus are associated with the outgoing channels of EST0.

In IDX Link mode, there are 32 outgoing channels for the EST0 stream. For the EST1 stream there are 96 outgoing channels. In this mode the Connection Memory is configured such that the first 32 locations are used for the EST0 stream. The next 96 locations are for the EST1 stream as selected by the Expansion Bus Position bits as described in "Address Memory Map" on page 12.

5.0   Address Memory Map

The MT90812 memory is accessed via the microport. The microport can operate in multiplexed or non-multiplexed mode as described in "Microprocessor Port" on page 49 The access to the MT90812 memory for multiplexed and non-multiplexed mode is described below.

5.1   Memory Page Select

The MT90812 memory is divided into 7 pages, as listed in Table 1.

Non-Multiplexed Mode	Multiplexed Mode		Memory Pages
External Address A9,A8,A7	Memory Select Bits	External Address A7	
111	XXX	0	Control Registers (Section 22.0)
000	000	1	Local Data Memory
001	001	1	Expansion Data Memory
010	010	1	Local Connect Memory Low
011	011	1	Expansion Connect Memory Low
100	100	1	Local Connect Memory High
101	101	1	Expansion Connect Memory High

Table 1 - MT90812 Memory Page Select

In multiplexed mode, the Memory Select bits in the Address Memory Select register (AMS) determine the page that is addressed. In non-multiplexed mode, the external address bits A9,A8,A7, determine the page that is addressed, eliminating the need to access the AMS register for memory page select.

The control registers, described in "Detailed Register Descriptions" on page 52, consist of one page of 128 locations. In multiplexed mode the control registers are accessed independent of the setting of the memory select bits in the AMS register, by setting the external address bit A7 to low. In non-multiplexed model the control registers are accessed by setting address bits A9, A8, and A7 to High. **The control register at location 61_H ($3E1_H$ in motorola non-muxed, 061_H in in multiplexed mode) must be initialized to 080_H.**

The addressing of the other blocks and memory pages are described below. Each Data and Connect Memory page consists of 128 locations, as shown in Table 2.

5.1.1   Addressing Memory Pages in Multiplexed Microport Mode

An MT90812 memory address, in multiplexed microport mode, consists of two portions. The higher order bits(3) originate from the Control Address Memory Select (AMS) register, which may be written to or read from via the Control Interface. The Control Interface receives address information at A7 to A0, data information at D7 to D0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. The lower order bits(8) originate from the address lines directly. The address lines A6-A0, on the Control Interface, give access to the MT90812 registers directly if A7 is zero, or depending on the contents of AMS register, to the High or Low sections of the Connection Memory, or to the Data Memory.

5.1.2   Addressing Memory Pages in Non-Multiplexed Microport Mode.

A MT90812 memory address, in **non-multiplexed** microport mode, consists of A9 to A0. The higher order bits(3) originating from the external address bits A9,A8,A7, control which page is accessed. The Control Interface receives address information at A9 to A0, data information at D7 to D0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. The lower order bits(7) originating from the external

address bits A6-A0, give access to the Control Registers if A9,A8,A7=111, or depending on the high order bits A9,A8,A7, to the High or Low sections of the Connection Memory, or to the Data Memory, as shown in Table 1.

5.2   Data Memory and Connect Memory

The Data Memory and Connect Memory Map, as shown in Table 2, illustrates the direct relationship between DM and CM for each of the channels. As described earlier in "Switching" on page 10, the data from the incoming TDM streams are written to Data Memory and the data is switched to the outgoing streams as programmed in CM.

	Address A6-A0	Memory Pages		
		Data Memory Pages	Connect Memory High Pages	Connect Memory Low Pages
Local Memory Page	00-1F	Sti0 32 Channels	Sto0 Outgoing Gain	Sto0 32 Channels
	20-3F	Sti1 32 Channels	Sto1 Outgoing Gain	Sto1 32 Channels
	40-5F	Tones(32), FSK	Tone Gain	(Not used)
	60-7F	Confout(15), unused(1) DCHout(1) unused(15)	Conf - Incoming Gain(15) IT - Incoming Gain(1) DCH - Incoming Gain(1) EDA -Incoming Gain(1) EDB -Incoming Gain(1) unused(13)	Conf Incoming Channel(15) Insertion Tone - Channel(1) DCH Incoming Channel(1) EDA -Incoming Channel(1) EDB -Incoming Channel(1) unused(13)
Expansion Memory Page	00-1F	Ei1 32 Channels	Ei1 Outgoing Gain	Ei1 32 Channels
	20-3F	Ei2 32 Channels	Ei2 Outgoing Gain	Ei2 32 Channels
	40-5F	Ei3 32 Channels	Ei3 Outgoing Gain	Ei3 32 Channels
	60-7F	Ei4 32 Channels	Ei4 Outgoing Gain	Ei4 32 Channels

Table 2 - Data Memory and Connect Memory Pages

In addition to holding the incoming data from the TDM streams, Data Memory holds the output of the other MT90812 blocks. This is described below in the following section. Expansion Memory page is used to hold the incoming data for the expansion bus TDM streams. Refer to "Use of Data Memory Reserved for Expansion Bus Streams" on page 15 for further description.

Connection Memory is used to specify the source for the outgoing channels and to connect the Conference, Energy Detect and DBRT blocks to incoming channels. In addition CM is used to specify the gain for the outgoing streams and the gain for the tones.

5.2.1   Local Data Memory

Table 3 details the mapping for Local Data Memory. The first block of 32 locations in Data Memory is used to store the 32 bytes of data from the STi0 stream. Locations 20-3F are used for the 32 bytes of data from the STi1 stream. The third block of 32 locations in Data Memory is used for output of the tone generator block as described in "Tone Generation" on page 42 The next 32-bytes consist of conference outputs(15), DCHout(1), and some unused locations(14).

Address A6-A0	Local Data Memory	Description
00-1F	Sti0 32 Channels	Sti0 32 Channels
20-3F	STi1 32 Channels	STi1 32 Channels

Address A6-A0	Local Data Memory	Description
40-59	DTMF Tones(26)	DTMF Tone generator output
59-5A	Tone Ringer or DTMF	Tone Ringer or Tone Generator output
5B-5E	Tones(4)	Tone generator output
5F	FSK or DTMF	FSK Transmitter output or Tone generator output
60-6E	CONFout(15)	Conference Output
6F	unused	
70	DCHout(1)	Output from the D-channel TX FIFO buffer. Allows D-channel TX buffer to be directed to any outgoing channel.
71-7F	unused(14)	unused(14)

Table 3 - Local Data Memory

5.3   Connection Memory use in Conferencing, Gain Control and specifying Incoming Sources for Energy Detect and DBR

Connection Memory is used to specify the source and gain for the 64 outgoing channels of STo0 and STo1 and the 128 outgoing channels of the expansion bus. Message mode, Minimum or Constant Delay and Output Enable are specified in CMH for each of these channels.

The conference circuit incoming channels are specified in CML 60-6E. The incoming conference gain, inversion bit and noise suppression are specified in CMH. Message mode, Minimum or Constant Delay and Output Enable are not used for locations 60-6E reserved for conference control. See the description of "Connection Memory High" on page 50. Channels are transferred from Data Memory with Constant Delay to the conference circuit.

Channels that can be included in a conference include; the 64 channels of STi0 and STi1, and the channels of the four expansion bus blocks. In fact any location in Local or Expansion Data Memory can be specified as in incoming conference source, including the 32 tones or the DBT output. The Conference Party Control registers specify which conference the channel is participating in, output attenuation levels, tone insertion and conference initialization. See the description of "Conference Party Control Register (CPC1-15)" on page 65.

CM is also used to connect the Energy detect and DBRT blocks to incoming channels. The incoming channels are specified in CML. The locations are listed below in Table 4. Channels can be transferred from Data Memory in either Minimum or Constant Delay to the Energy Detect and DBRT blocks as specified in CMH. CMH Message Mode and Output Enable bits are ignored for locations 70-72 of CM.

In addition CMH is used to specify the gain for the outgoing streams and the gain for the tones.

Hex Address A6-A0	Connect Memory Low	Description
60-6E	CONFin	Conference Incoming
6F	Insertion Tone	Insertion Tone Incoming Channel
70	DCH in(1)	Incoming channel to be transferred to the DBR FIFO.
71	EDA	Incoming channel to be transferred to the Energy Detect A block
72	EDB	Incoming channel to be transferred to the Energy Detect B block
72-7F	unused(14)	unused(14)

Table 4 - Connect Memory

Channels can be transferred from Data Memory in either Minimum or Constant Delay to the Energy Detect and DBRT blocks as specified in CMH. CMH Message Mode and Output Enable bits are ignored for locations 70-72 of CM.

In addition, CMH is used to specify the gain for the outgoing streams and the gain for the tones.

5.4   Use of Data Memory Reserved for Expansion Bus Streams

The use of the four blocks reserved for the expansion bus is dependent on the expansion bus mode set for the device. The two expansion bus modes, TDM Link and IDX Link, are described on page 8. In TDM Link mode, the four blocks are used according to the data rate set for the expansion bus. At 2.048 Mb/s the first 32 bytes, 00-1F, are used to store the incoming data. At 4.096 Mb/s the first 64 bytes, 00-3F are used. At 8.192 Mb/s all 128 locations, 00-7F, are used.

In IDX Link mode, 128 channels are read, 32 from EST1 and 96 from EST0. The positions that the MT90812 will read and write to the expansion bus are controlled by the EP1 and EP0 bits in Control Register B.

For example, a group of four MT90812 devices are labelled A, B, C, and D. The 128 channels on the expansion bus streams are identified as A1, B1, C1, D1, A2, B2, C2, D2,...., A128, B128, C128, D128. The MT90812 with EP1,EP0 set to 0,0 will read and write to EST0 and EST1 as listed in Table 5.

	Expansion Bus Channel (i=1,32)			
	Ai	**Bi**	**Ci**	**Di**
EST0	Write	Read	Read	Read
EST1	Read	Write	Write	Write

Table 5 - Expansion Bus Read/Write timeslots for IDX A

The MT90812 with EP1,EP0 set to 0,0 will output on EST0 during channel Ai and will read the next three channels Bi, Ci and Di. Channels Bi, Ci and Di go into Data Memory at Expansion Block 2, 3 and 4 respectively, as shown in Table 2. Expansion block 1 will contain incoming channels on EST1 sent to IDX A in timeslots labelled EA1,...,EA32 as shown in Figure 7 on page 9.

The MT90812 with EP1,EP0 set to 0,1 will output on EST0 and read EST1 during channel Bi and will read EST0 and output on EST1 for channels Ai, Ci and Di.

The memory map for the expansion bus timeslots are shown in the Figures 8 - 12 for each of the four settings of EP1 and EP0.
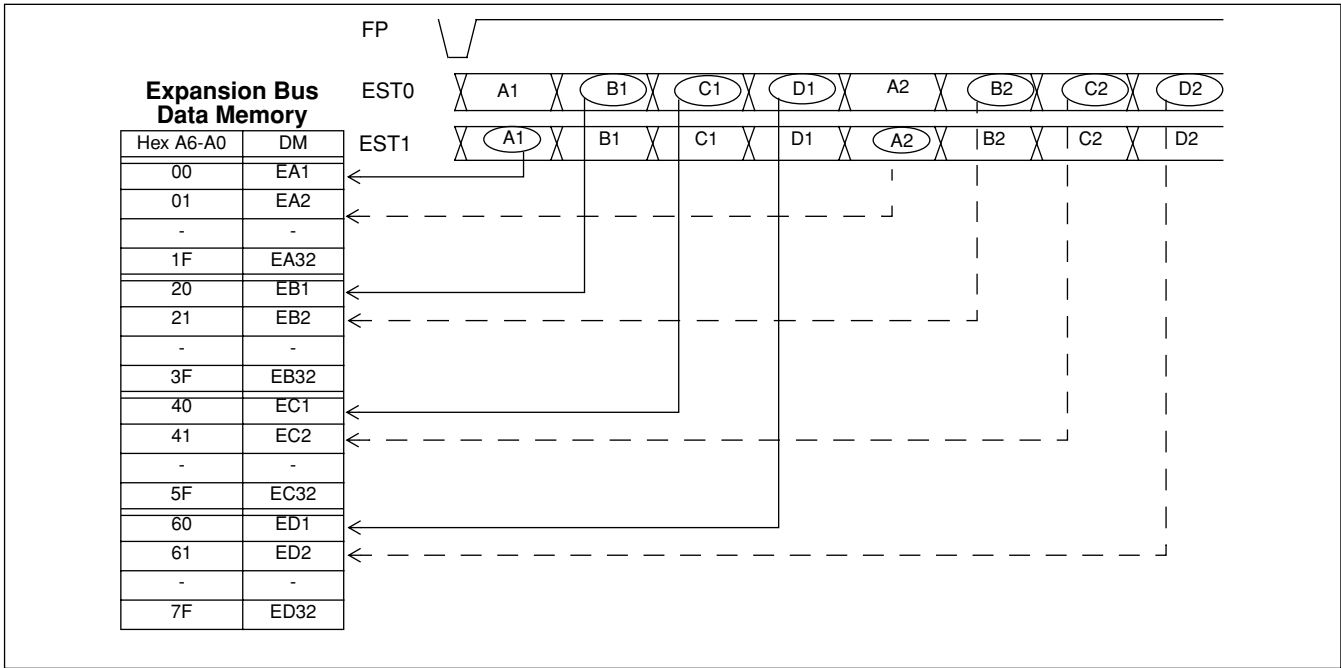
Expansion Bus Data Memory

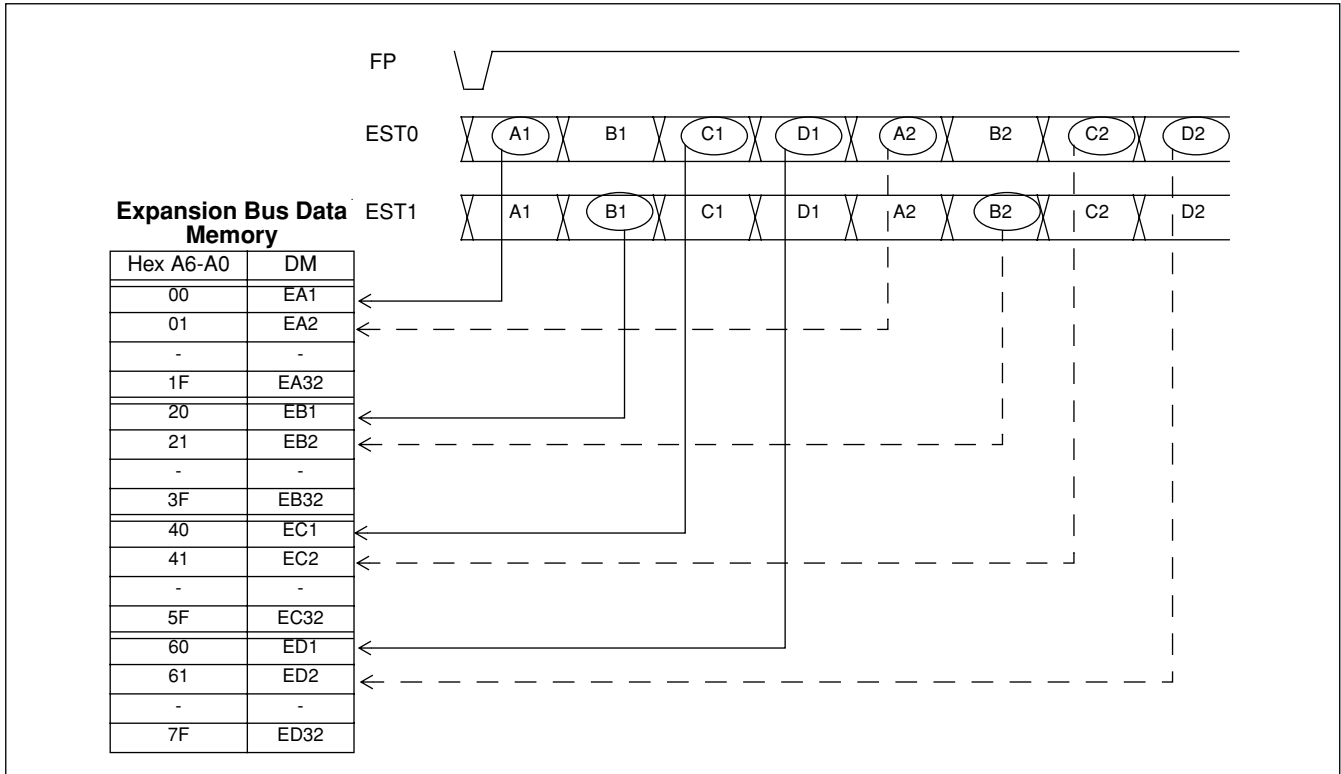| Hex A6-A0	DM
00	EA1
01	EA2
-	-
1F	EA32
20	EB1
21	EB2
-	-
3F	EB32
40	EC1
41	EC2
-	-
5F	EC32
60	ED1
61	ED2
-	-
7F	ED32

Figure 8 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 00

Expansion Bus Data Memory

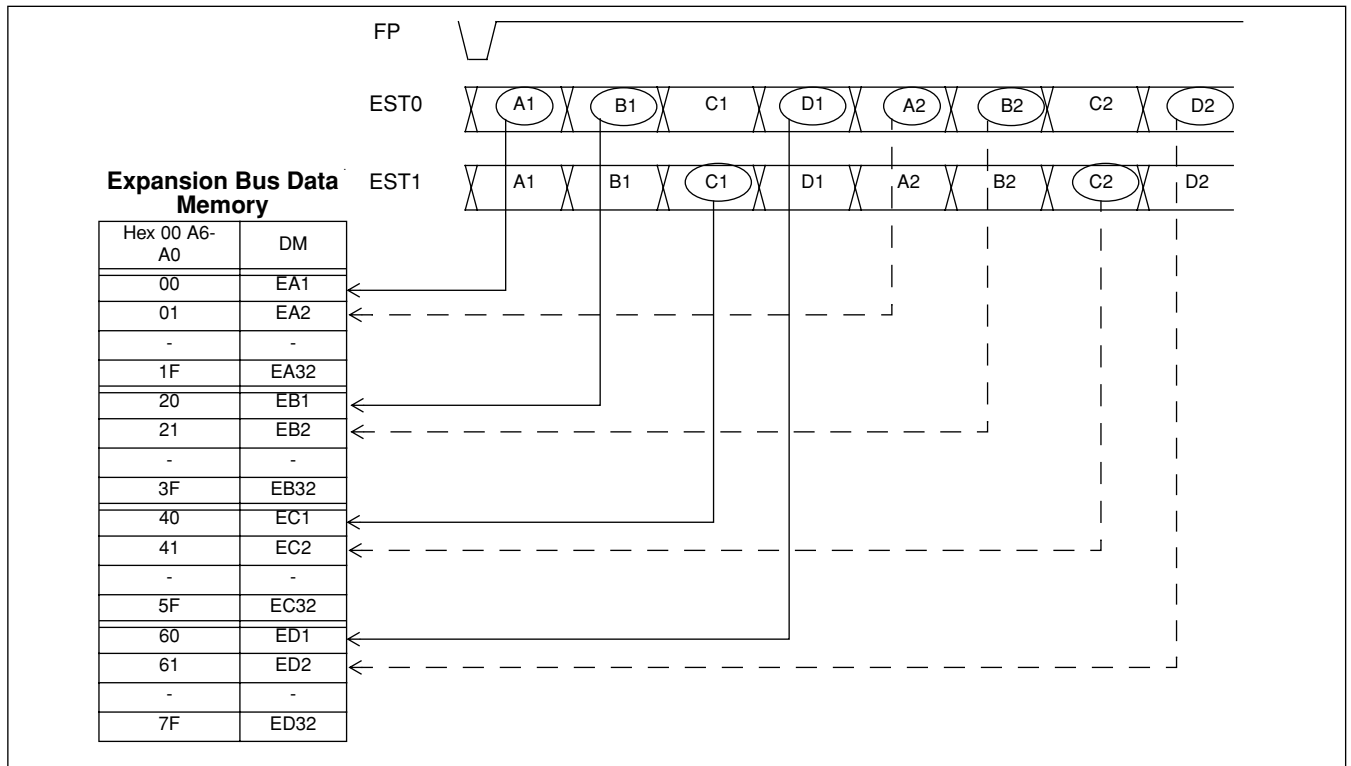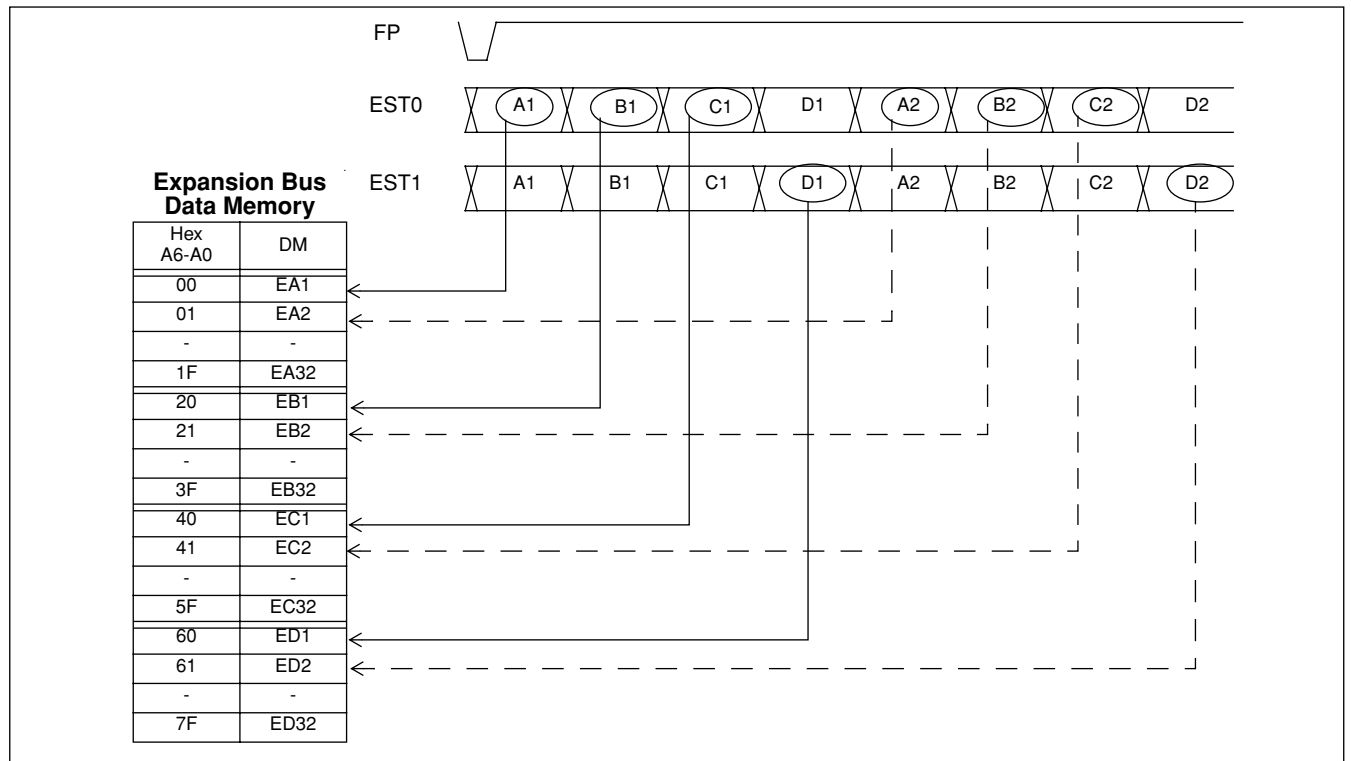| Hex A6-A0	DM
00	EA1
01	EA2
-	-
1F	EA32
20	EB1
21	EB2
-	-
3F	EB32
40	EC1
41	EC2
-	-
5F	EC32
60	ED1
61	ED2
-	-
7F	ED32

Figure 9 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 01
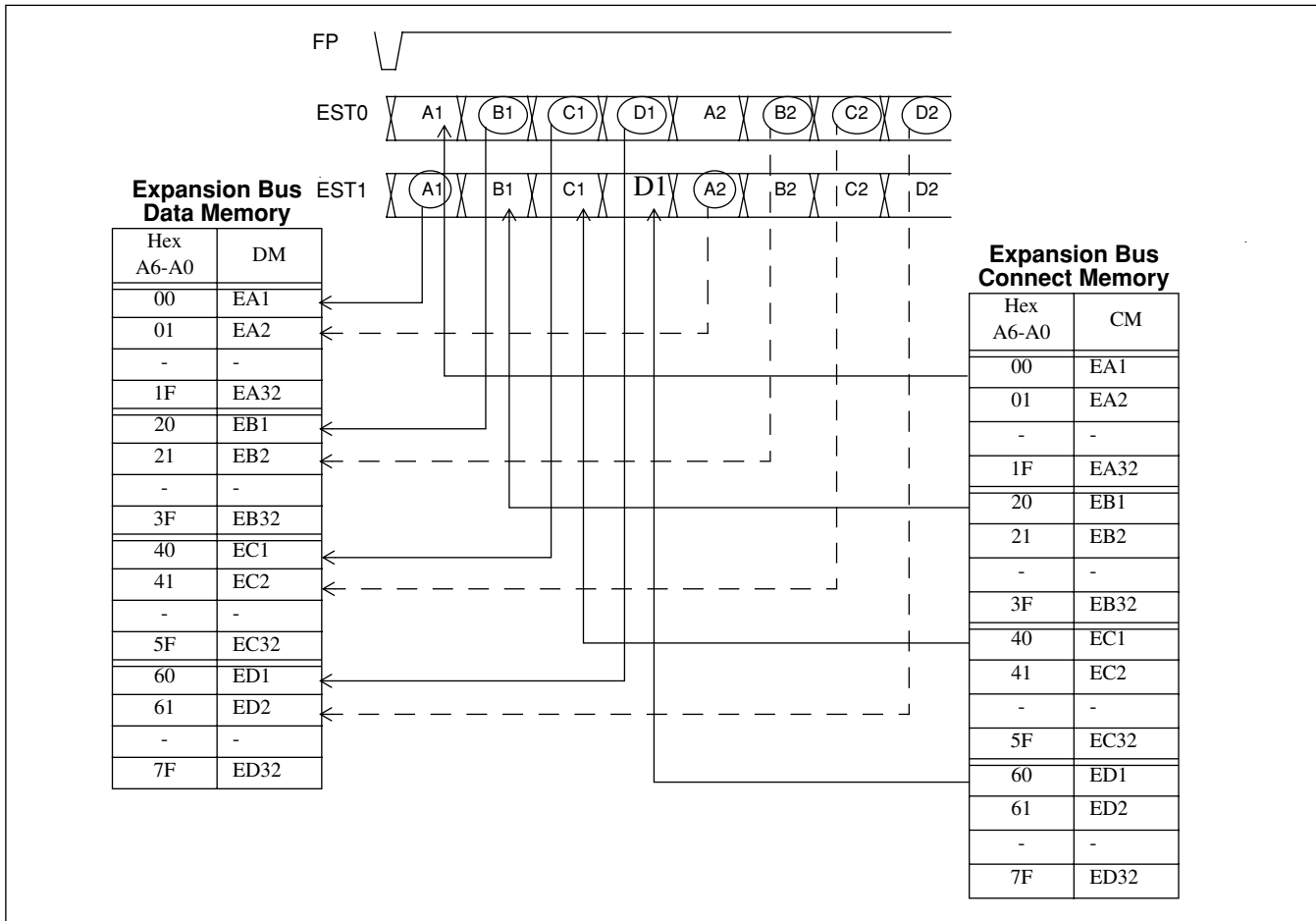
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Figure 10 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 10

Figure 11 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 11

The previous diagrams illustrate the Data Memory allocation for the timeslots on EST0 and EST1. Fig. 12 illustrates Connect Memory allocation for the timeslots on EST0 and EST1. For the IDX A, which has EP0,EP1 = 00, the circled timeslots are read as incoming data to Data Memory. The other timeslots are outgoing

timeslots, where IDX A can either write to EST0 and EST1 during these channels or place EST0 or EST1 in high impedance.

Figure 12 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 00
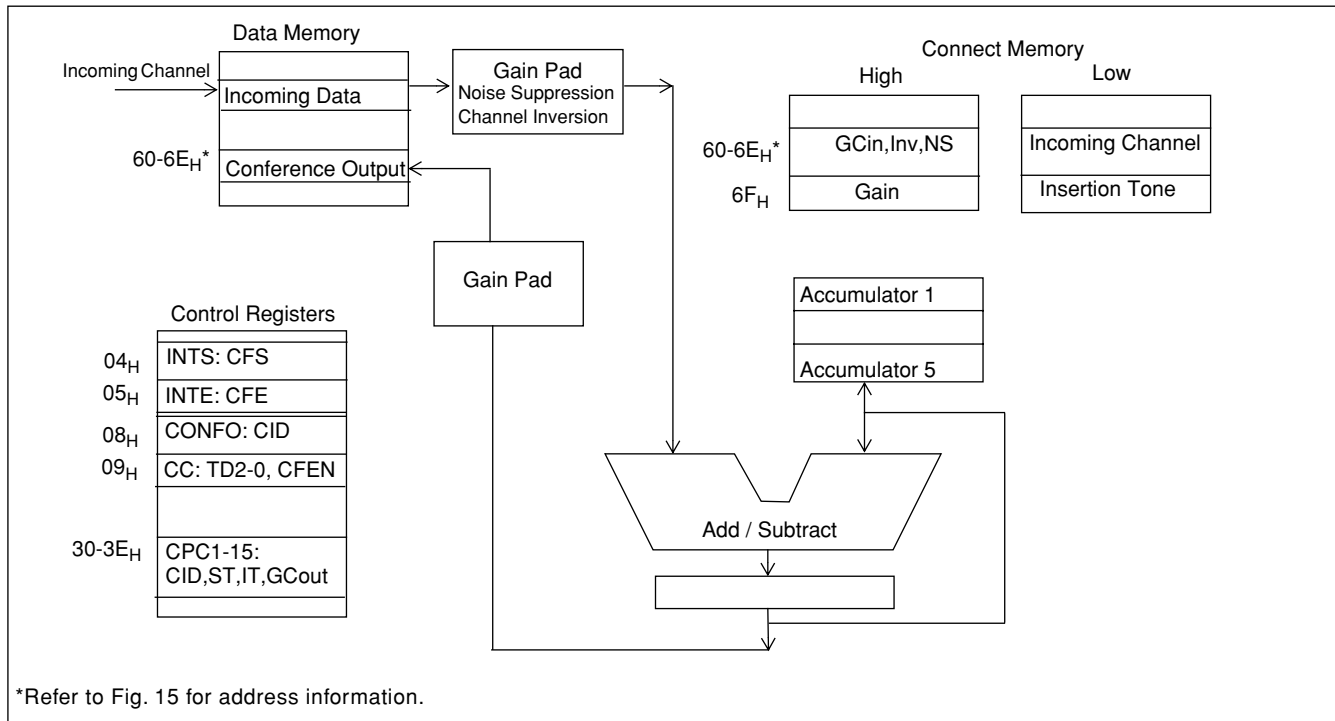
6.0   Conferencing

The conference block provides conference call capability in the MT90812 and supports a total of 15 parties, distributed over a maximum of 5 conferences. (i.e. 1x15 parties, 3x5 parties, 5x3 parties etc.). A/m-Law companded data from an incoming channel is converted to linear format, applied incoming gain, processed by a dedicated arithmetic unit, applied outgoing conference gain and stored in Data Memory in linear format. The output signal contains all the information of each channel connected in conference except its own.

For each of the 15 conference parties there is a Conference Party Control Register. The **Conference Party Control Register** contains the conference ID, start bit, insertion tone enable and outgoing channel attenuation. Refer to "Conference Party Control Register (CPC1-15)" on page 65.

The output for each conference is stored in 1 of 15 Data Memory locations which can be switched to any outgoing channel. For each of the 15 DM locations the corresponding Connect Memory Low byte is used to specify the incoming source channel.

The conference circuit incoming channels are specified in CML 60-6E. The incoming conference gain, inversion bit and noise suppression are specified in CMH. Message mode, Minimum or Constant Delay and Output Enable are not used for locations 60-6E reserved for conference control. See the description of "Connection Memory High" on page 50. Channels are transferred from Data Memory with Constant Delay to the conference circuit.

Channels that can be included in a conference include; the 64 channels of STi0 and STi1, and the channels of the four expansion bus blocks. In fact any location in Local or Expansion Data Memory can be specified as in incoming conference source, including the 32 tones or the DBT output.
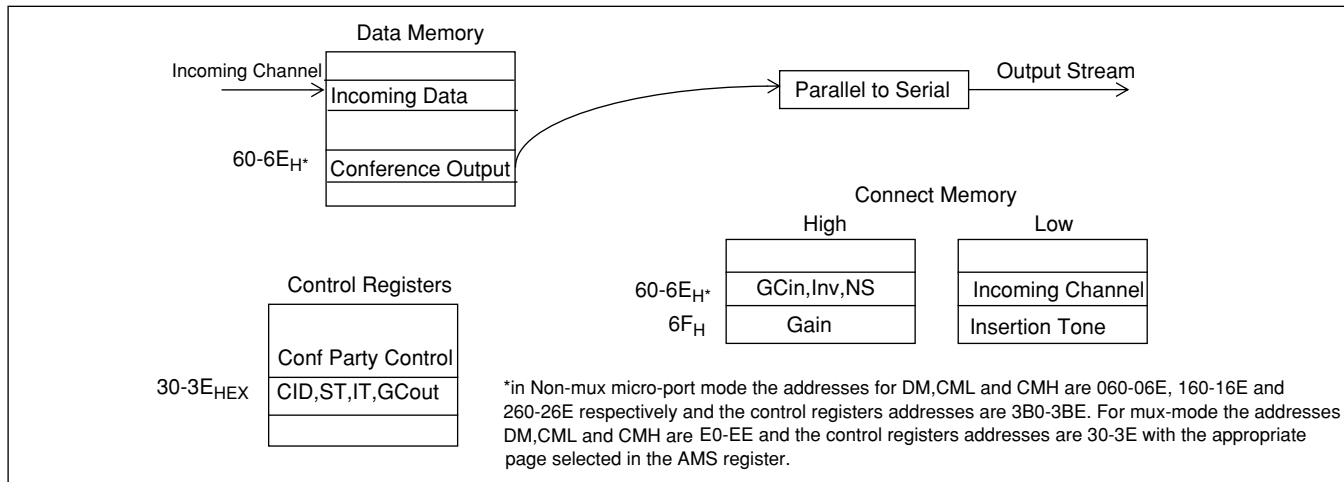

Figure 13 - Conference Circuit Block Diagram
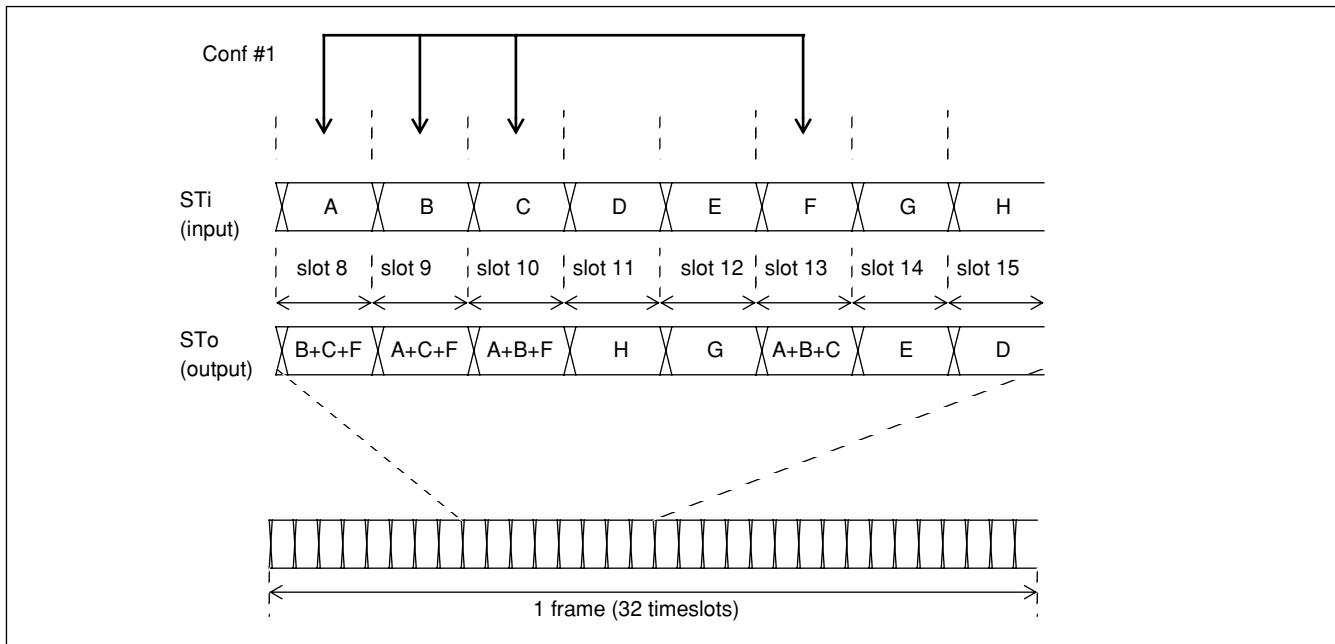
Figure 14 - Four Party Conference Example

Figure 15 - Conference Control with Conference Party Control Registers and Connect Memory

6.1   Channel Attenuation

Channel Attenuation is provided on incoming and outgoing channels that are in a conference. The gain can range from +3 to -27 dB in steps of 1dB, as well as $-\infty$ dB for the incoming PCM data and +0 to -9 dB in steps of 3dB for outgoing PCM data. If an overflow condition occurs, then the input from each channel in a conference can be independently attenuated, by setting the incoming channel attenuation bits in CMH for the specific conference party. The outgoing gain bits are in the Conference Party Control register.

6.2   Noise Suppression and Channel Inversion

Channel inversion and noise suppression bits are specified in Connect Memory High for locations $60\text{-}6E_H$.

When noise suppression is enabled for a specific input channel, then the PCM bytes for this channel, when below the selected threshold level, are converted to PCM bytes corresponding to the minimum PCM code level before being added to the conference sum. The four threshold levels available correspond to the first, fifth, ninth, and sixteenth step of the first segment. These are 1/4096, 9/4096, 16/4096, and 32/4096 with respect to full scale A-law, and 1/8159, 9/8159, 16/8159, and 32/8159 with respect to full scale ulaw. The threshold level is set using the threshold bits NS1, NS0.

The inversion bit allows for every other channel in a conference to be inverted. This reduces noise due to reflections and line impedance mismatch.

6.3   Tone Insertion

As a party is added to a conference, if the insertion tone bit (IT) is set, all channels connected in a conference will have the tone added to the conference output. This allows for conference users to be informed of a new party being added to the conference, or to be reminded that they are in a conference.

The DM address of the desired tone must be programmed at location $6F_H$ of CML, ($16F_H$ non-mux mode, EF_H for mux-mode addressing). The tone source may be from any location in DM, including any of the 32 tones from the Tone Generation block. The PCM data from the specified Data Memory location will be added to the conference output for a specified tone duration.

The tone duration is specified in the Conference Control Register (CC). Refer to Section 22.10 for a description of the Conference Control Register (CC). The tone duration can be set from 0.125 to 1.0 seconds in steps of 0.125 seconds. The tone duration is from the time the party is added to the conference by writing the Conference Party Control Register.

6.4   Conference Overflow

A peak clipping indicator identifies the conference causing conference bridge overflow whenever a 14-bit two complement overflow occurs[1]. Once a conference bridge overflow occurs an interrupt is asserted, the Conference Overflow bit in the Interrupt Status Register (INTS) is set and the conference ID is placed in the Conference Overflow Status Register (CONFO). Refer to the CONFO register description on page 59.

Reading the Interrupt Status Register (INTS) will clear the Conference Overflow bit. A conference overflow will not trigger an interrupt until the conference overflow bit is cleared. The conference overflow interrupt is maskable using the Interrupt Enable Register (INTE). The conference interrupt mask does not disable updates of the CONFO register. The Conference ID in this register will not be updated again until it is reset. The register is reset following a read of the register or resetting the conference block or Mt90812 device.

Note 1 - The overflow limit is the same whether Ulaw or Alaw companding is used. Following gain adjustment companding will then implement clipping to the Ulaw and Alaw max values of 8031 and 4032 respectively.

6.5   Starting a New Conference

In order to initiate a conference, the Conference Party Control register as well as Connection Memory Low/ High must be programmed. Setting the **ST** bit for the **first** party programmed for a conference will remove any other parties that may have been previously programmed for that conference. The following steps outline initialization of a conference.

Conference Block Initialization
1)   Perform MT90812 reset or conference reset. The Conference Party Control registers are reset and all conference ID numbers are set to null.
2)   Disable the conference overflow interrupt until after a conference is set up. Set CFE bit LOW in the Interrupt Enable Register (INTE).
3)   Enable the conference block by writing to the conference control register, setting CFEN=1 and setting the tone duration.
4)   Set up Tone Insertion: program the tone by writing the tone coefficient registers if a different programmable tone is required. Refer to "Tone Generation" on page 42 Identify the tone by writing CML location 6F with the DM address of the Tone. Write CMH location 6F with the gain setting for the insertion tone.

Conference Party Initialization
5)   Write CMH with the Incoming gain, inversion bit and noise suppression for the first party.
6)   Write CML with the Incoming channel DM address for the first party.
7)   Write the Conference Party Control register with a conference ID from 1-5. Set the **ST** bit for the **first** party programmed for a conference. Setting the ST bit will remove any other parties that may have been previously programmed for that conference. Set the Insertion Tone bit and outgoing conference gain control required.
8)   Write CML of the Incoming channel with DM address of the conference output location (60-6E$_H$). Write CMH of the location with the required outgoing gain if it has not been previously set. Also set the OE bit.
9)   Repeat steps 5 to 8 for each additional party in the conference.
10)   Enable the conference overflow interrupt if required, by setting CFE, bit 1 in the Interrupt Enable Register (INTE). Read the CONFO register to ensure it is reset allowing the next overflow to update the conference ID value.

6.6   Removing a channel from a Conference

Setting the Conference ID number, in Conference Party Control register, to '0' will disconnect the selected channel from the conference. Once the selected channel is removed from the conference, the Output Enable

(OE) bit of Local (or Expansion depending on the output stream number) Connect Memory High must be set to 0 in order to put the output driver of the corresponding stream into high-impedance state during the selected timeslot.

7.0 Gain Control

Gain Control is provided on the outgoing channels, with a range of +3 to -27 dB in steps of 1dB, as well as -∞ dB. If a channel is in a conference, incoming and/or outgoing gain control is provided, with a range of 0 to -9 dB in steps of 3 dB. Refer to Section 6.0 for a description of gain control for a conference.

Outgoing gain control of +3 to -27 dB in steps of 1dB, as well as -∞ dB is also provided on the 32 tones from the Tone generator.

The gain for each outgoing channel is specified in Connect Memory High. Refer to "Connection Memory High" on page 50. There are five bits G4-G0 which are used to set the gain. If 0 dB value is selected then the gain control circuitry is bypassed. Otherwise the 8 bit PCM value for the outgoing channel is read from Data Memory, expanded to a 14 bit linear PCM value, multiplied by the appropriate gain factor, and compressed to an 8 bit PCM value, before being output on the outgoing serial stream.

The output of the tone generator and conference blocks are multiplied by the gain factor specified for the tone or conference party and stored as a 14 bit linear PCM value in Data Memory. When the outgoing channel is connected to a tone or conference output location, the 14 bit linear PCM value is then read from DM, multiplied by the gain factor specified for the outgoing channel, and compressed to an 8 bit PCM value, before being output on the outgoing serial stream.

8.0 Delays Through the MT90812

A delay results when transferring channel information from a MT90812 local input stream to an output stream. This delay varies according to the switch mode programmed in the CST bit of connect memory high; i.e. Minimum or Constant Throughput Delay Mode.

8.1 Minimum Delay Mode (CST bit=0)

In Minimum Delay Mode the delay is dependent on the combination of source and destination channels, the input and output streams and the data rate of the expansion bus.

Data transfers between streams operating at the same data rate (i.e. Sti1 to Sto1, Est1 to Est0, etc.) can be described as follows. Channel information for a particular timeslot **n** from the input stream is sent to Data Memory in timeslot **n+1**. Channel information is queued for an output channel **n** in timeslot **n-1**. Thus, information entering the MT90812 from timeslot **n**, cannot be transmitted in the same timeslot **n** or timeslot **n+1**, without a frame delay. Information switched to a timeslot of **m=n+2** or later will be switched within the same frame. The relationship that is required between incoming and outgoing timeslots are shown in Table 6. For all but four cases, if the outgoing timeslot, m, is greater than or equal to n+2, the data is switched within the same frame. The throughput delay is m-n timeslots.

There are four cases where there are data transfers between streams operating at different data rates. This occurs when the expansion bus is running at 4.096Mb/s or 8.192 Mb/s and the data is transferred between the expansion bus and either Sto0 or Sto1. The channel numbers range from 0 to 31 for a stream operating at 2.048Mb/s, and from 0 to 63 and 0 to 127 for streams operating at 4.096Mb/s and 8.192 Mb/s, respectively.

Source and Destination Streams	Expansion Bus Data Rate		
	2.048 Mb/s	**4.096 Mb/s**	**8.192 Mb/s**
Sti0/1 -> Sto0/1		N/A	N/A
Est0/1 -> Est0/1	m>=n+2	m>=n+2	
Sti0/1 -> Est0/1		m>=2n+3	m>=4n+5
Est0/1 -> Sto0/1		m>=(n+3)/2	m>=(n+5)/4

Table 6 - Output Channels for Minimum Delay

The output channel number m, specified for minimum delay in these four cases account for there being two 4.096Mb/s channels and four 8.192Mb/s channels for every one 2.048Mb/s channel.

Table 7 lists the condition required for a throughput delay of less than one frame period, the throughput delay if this condition is met and the throughput delay expressed in timeslots when switching is made in the following frame. For cases where there are different data rates the delay is expressed in timeslots associated with the fastest data rate. i.e. with the source channel from Est1 (@8Mb/s) and destination channel on STo1 (@2Mb/s) the delay is expressed in 8Mb/s timeslots. If the incoming 8Mb/s channel, n = 119, outgoing 2Mb/s channel m =31, then the delay = 4m-n = 4(31)-119= five 8Mb/s timeslots. If m=1 the delay=128-(n-4m)=128-(119-4)=thirteen 8Mb/s timeslots.

Source and Destination Streams	Input channel, n, range	Output channel, m, range	Condition for switching within same frame	Throughput Delay within same frame	Throughput Delay if condition not met
Sti0/1 -> Sto0/1	0-31	0-31	m>=n+2	m-n t.s$_2$.	32-(n-m) t.s$_2$.
Est0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	m>=n+2	m-n t.s$_2$.	32-(n-m) t.s$_2$.
Est0/1 -> Est0/1 4.096 Mb/s	0-64	0-64		m-n t.s$_4$.	64-(n-m) t.s$_4$.
Est0/1 -> Est0/1 8.192 Mb/s	0-127	0-127		m-n t.s$_8$.	128-(n-m) t.s$_8$.
Sti0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	m>=n+2	m-n t.s$_2$.	32-(n-m) t.s$_2$.
Sti0/1 -> Est0/1 4.096 Mb/s	0-31	0-64	m>=2n+3	m-2n t.s$_4$.	64-(2n-m) t.s$_4$.
Sti0/1 -> Est0/1 8.192 Mb/s	0-31	0-127	m>=4n+5	m-4n t.s$_8$.	128-(4n-m) t.s$_8$.
Est0/1 2.048 Mb/s -> Sti0/1	0-31	0-31	m>=n+2	m-n t.s$_2$.	32-(n-m) t.s$_2$.
Est0/1 4.096 Mb/s -> Sti0/1	0-64	0-31	m>=(n+3)/2	2m-n t.s$_4$.	64-(n-2m) t.s$_4$.
Est0/1 8.192 Mb/s -> Sti0/1	0-127	0-31	m>=(n+5)/4	4m-n t.s$_8$.	128-(n-4m) t.s$_8$.

Table 7 - Throughput Delay for Minimum Delay Mode

Notes: t.s. = time-slot. t.s$_2$. =2Mb/s t.s. = 3.9 us. t.s$_4$. =4Mb/s t.s.=1.95 us. t.s$_8$.=8Mb/s t.s.=0.975 us.
Delays are measured in timeslots and at the point in time from when the input channel is completely shifted in and when the output channel is completely shifted out.

8.2 Constant Delay Mode (CST bit=1)

In Constant Delay mode, channel integrity is maintained by making use of a multiple Data Memory buffer technique. The input channels written in any of the buffers during frame N will be read out during frame N+2. Table 8 lists the throughput delay for Constant Delay mode for all combinations of source and destination streams.

Source and Destination streams	Input channel, n, range	Output channel, m, range	Throughput Delay
Sti0/1 -> Sto0/1	0-31	0-31	$2 \times 32 - (n-m)$ t.s$_2$.
Est0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	$2 \times 32 - (n-m)$ t.s$_2$.
Est0/1 -> Est0/1 4.096 Mb/s	0-64	0-64	$2 \times 64 - (n-m)$ t.s$_4$.
Est0/1 -> Est0/1 8.192 Mb/s	0-127	0-127	$2 \times 128 - (n-m)$ t.s$_8$.
Sti0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	$2 \times 32 - (n-m)$ t.s$_2$.
Sti0/1 -> Est0/1 4.096 Mb/s	0-31	0-64	$2 \times 64 - (2n-m)$ t.s$_4$.
Sti0/1 -> Est0/1 8.192 Mb/s	0-31	0-127	$2 \times 128 - (4n-m)$ t.s$_8$.
Est0/1 2.048 Mb/s -> Sti0/1	0-31	0-31	$2 \times 32 - (n-m)$ t.s$_2$.
Est0/1 4.096 Mb/s -> Sti0/1	0-64	0-31	$2 \times 64 - (n-2m)$ t.s$_4$.
Est0/1 8.192 Mb/s -> Sti0/1	0-127	0-31	$2 \times 128 - (n-4m)$ t.s$_8$.

Table 8 - Throughput Delay for Constant Delay Mode

Notes: t.s. = time-slot. t.s$_2$. =2Mb/s t.s. = 3.9 us. t.s$_4$. =4Mb/s t.s.=1.95 us. t.s$_8$.=8Mb/s t.s.=0.975 us.
Delays are measured in timeslots and at the point in time from when the input channel is completely shifted in and when the output channel is completely shifted out.

8.3 Delays in Conferencing

In a conference the data is read from Data Memory and transferred to the conference block as in constant delay mode, with a 2 frame delay. If the incoming data is in frame N, then within the first half of frame N+2 the conference output is calculated and stored in the conference output locations in Data Memory. The conference output data is then switched to the outgoing data channel in Minimum Delay mode.

The minimum delay possible in a conference is one frame + two 2Mb/s-timeslots = 34 2Mb/s-timeslots. The maximum delay possible is approximately 2 frames + 1.5 frames + two 2Mb/s-timeslots = 82 2Mb/s-timeslots.
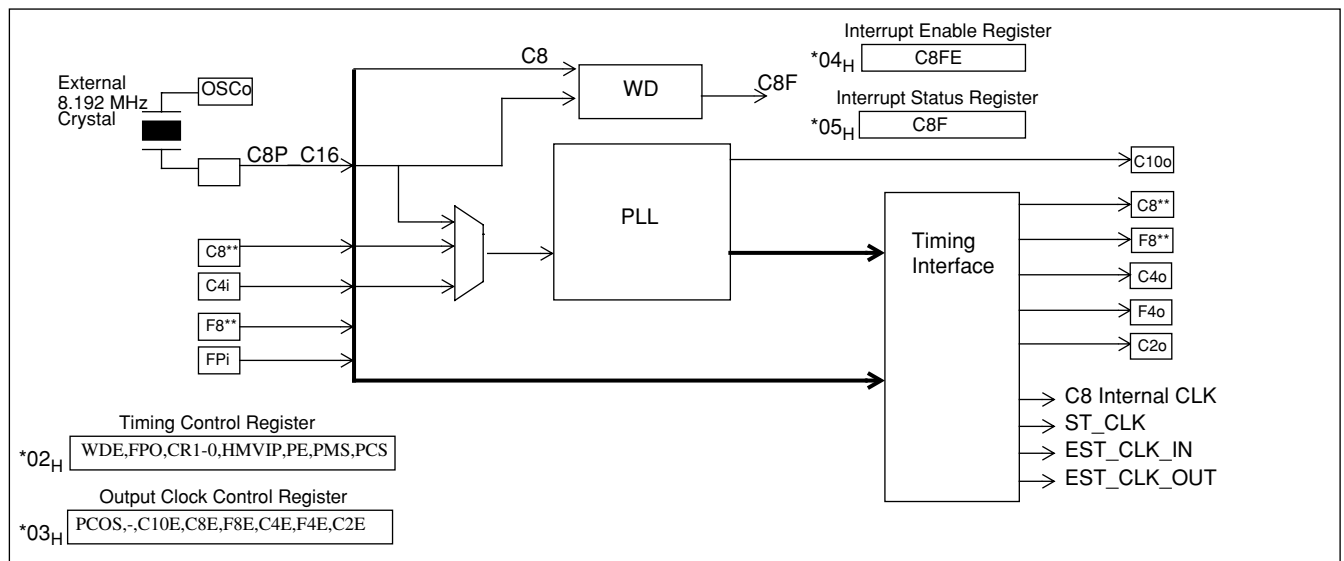
9.0 Timing and Clock Control

The MT90812 clock control circuitry selects one of five possible input clock and frame pulse references. The input clock can be either 4.092, 8.192, or 16.384 MHz as described in Section 9.1, "Input Timing Reference". Fig. 16 shows the Clock Control Functional diagram. The clock control circuitry provides an internal master clock of 8.192 MHz, generates 2.048, 4.096, 8.192, and 10.24 MHz output clocks, F4 and F8 frame pulse signals, as well as the serial interface timing for STi/o0, STi/o1 and EST0/1 serial streams. These signals are either generated directly from the input clock source or from an on-chip analog PLL.

The on-chip analog PLL may be used to generate 2.048, 4.096, 8.192, and 10.24 MHz clocks. The PLL operates in Master and Slave modes. Master mode provides more jitter attenuation while Slave mode minimizes Phase delay. The PLL can provide the required 4.096 and 10.24 MHz clocks (C4 and C10) to be supplied to the MT9171/72 DNIC devices. The C4 and C10 clocks meet the requirement that they be frequency locked and maintain a jitter of less than or equal to 15ns with respect to each other, while maintaining at least 40/60 duty cycle for C10o. Refer to Section 9.3.1, "Master and Slave PLL Modes".

Multiple IDX systems are supported by allowing the IDX to either drive or receive an 8.192 MHz clock. The master IDX in the system may supply C8 while the slave IDX derive their timing from the master. In a multi-chassis application a slave IDX may be required to generate its own C10. C8 is distributed between master and slave IDX devices and the PLL is then used to phase lock C10, C4 and C2 to the C8 input.

The MT90812 Expansion Bus can be supported with either an 8.192 MHz or 16.384 MHz clock when operating at 8.192 Mb/s. When the input clock source is selected as 16.384 MHz either HMVIP and non-HMVIP mode may be used.

In a multiple IDX system the slave IDX devices are supplied C8 from a master IDX. A watchdog timer on the IDX allows the slave IDX to monitor the C8 input. In the event of the loss of the C8 clock the slave IDX can be switched to be master IDX and supply C8 to the system. This provides redundancy for the clock source allowing IDX operation to remain independent of the other IDX devices if necessary.

Figure 16 - Clock Control Functional Diagram

*Non-mux mode addresses for TCR, OCCR, INTE and INTS are 382_H, 383_H, 384_H and 385_H, respectively.
**C8 and F8 are bi-directional pads. They are used as inputs in C8 timing mode, otherwise as output pads.

9.1 Input Timing Reference

The Input Timing Reference is selected setting CR1-0 and HMVIP bits in the Timing Control Register (TC) described on page 55. One of five possible clock and frame pulse references, C4/F4, C8/F8, C8P, or C16/F8, C16/HMVIP, can be selected, as listed in Table 9.

CR1,0	HMVIP	Clock Reference	Frame Pulse Reference
00	x	C4	FPi(F4)
01	x	C8	F8i
10	x	C8P (default)	No Frame Pulse
11	0	C16 Non-HMVIP	FPi (F8)
11	1	C16 HMVIP	FPi(F4)

Table 9 - Clock Modes

The MT90812 requires at least an 8.192 MHz clock internally. When the C4 input clock is selected the 8.192 MHz clock is derived from the PLL. C4 is not a valid clock reference when the PLL is disabled.