Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MT90840

Distributed Hyperchannel Switch

Data Sheet

Features

June 2007

- Time slot interchange function between eight pairs of ST-BUS/GCI/MVIP™ streams (512 channels) and parallel data port
- Programmable data rates on the parallel port (19.44, 16.384, or 6.480 Mbyte/s)
- Programmable data rates on the serial port (2.048 Mbps, 4.096 Mbps or 8.192 Mbps)
- Supports star and point-to-point connections, and unidirectional or bidirectional ring topologies for distributed systems
- Input-to-output bypass function on the parallel data port for use in add/drop applications
- Provides elastic buffer at parallel input port in the receive direction
- Provides byte switching for up to 2430 channels
- Per-channel direction control on the serial port side
- Per-channel message mode and high-impedance control on both parallel and serial port sides
- 8-bit multiplexed microprocessor port compatible with Intel and Motorola microcontrollers

Ordering Information

MT90840AL1	100 Pin MQFP*	Trays
MT90840AP1	84 Pin PLCC*	Tubes
MT90840APR1	84 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

- Guarantees frame integrity when switching nX64 wideband channels such as ISDN H0 channel
- Provides external control lines allowing fast parallel interface to be shared with other devices

Applications

- Bridging ST-BUS/MVIP buses to high speed Time Division Multiplexed backplanes at SONET rates (STS-1, STS-3)
- High speed isochronous backbones for distributed PBX and LAN systems
- Switch platforms of up to 2430 channels with guaranteed frame integrity for wideband channels
- Serial bus control and monitoring
- Data multiplexing
- High speed communications interface

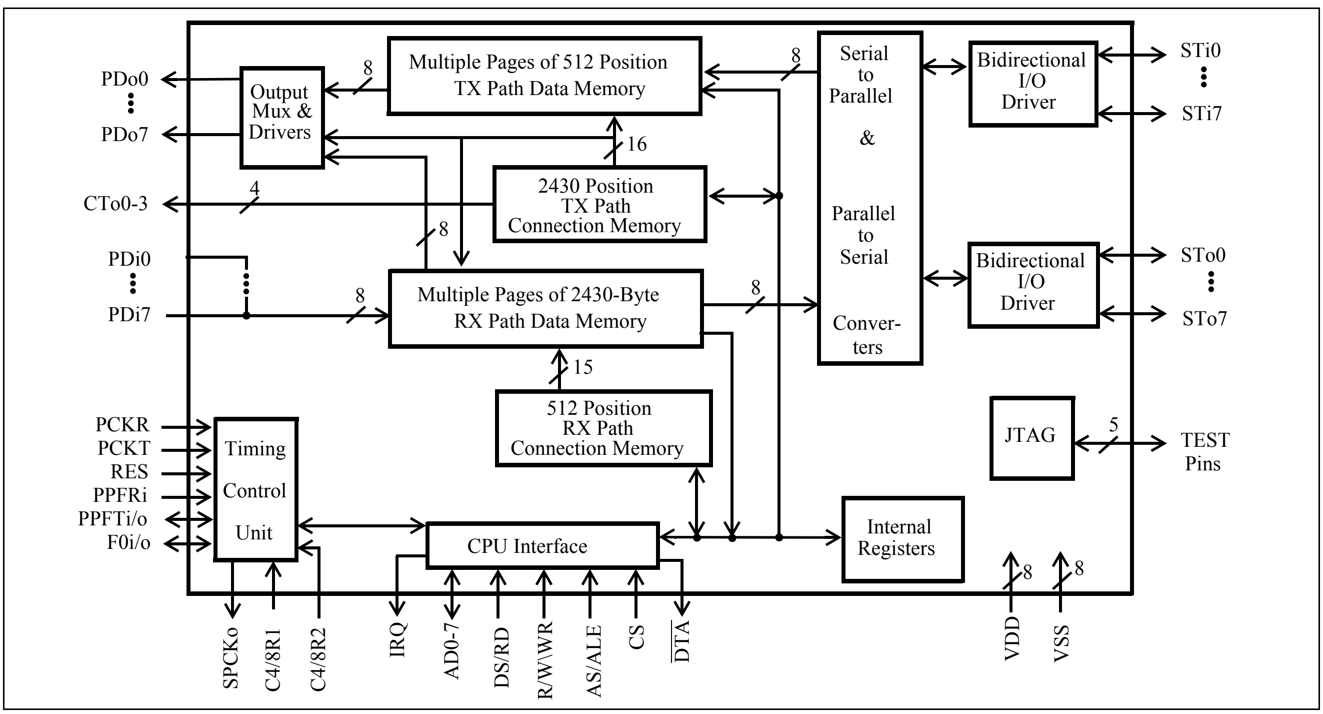

Figure 1 - Functional Block Diagram

Change Summary

Changes from April 2006 to April 2007. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information Box	Removed part numbers MT90840AL and MT90840AP from ordering information.

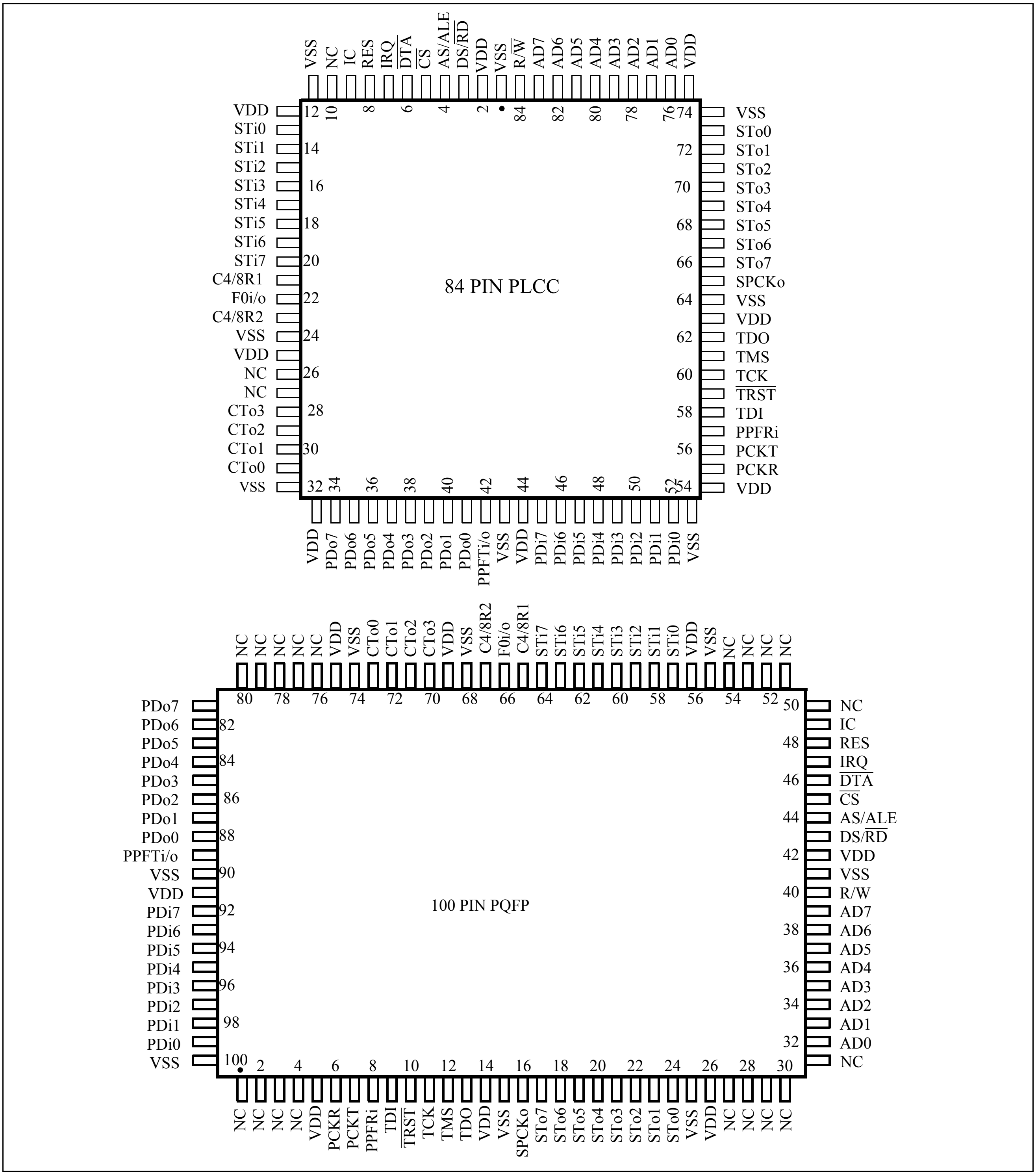

Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
84	100		
3	43	$\overline{DS}/\overline{RD}$	**Data Strobe/Read (Input**). In Motorola multiplexed-bus mode this pin is DS, an active high input which works with $\overline{CS}$ to enable read and write operation. In Intel/National multiplexed-bus mode this pin is $\overline{RD}$, an active low input which enables a read-cycle and configures the data bus lines (AD0-AD7) as outputs.
4	44	AS/ALE	**Address Strobe / Address Latch Enable (Input**). Falling edge is used to sample address into the Address Latch circuit.
5	45	$\overline{CS}$	**Chip Select (Input)**. Active low input enabling a microprocessor read or write of control or status registers.
6	46	$\overline{DTA}$	**Data Acknowledgment (Active Low Output)**. Indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then tri-states, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is tri-stated. Note that CPU read/writes from/to the Data and Connection memories occur on the serial or parallel port clock edges, and $\overline{DTA}$ will not change state if the clock is halted.
7	47	IRQ	**Interrupt Request (Active High Output)**. Output indicates that the MT90840 has detected an alarm condition. The indication of the specific condition can be read in the ALS (Alarm Status) Register. The CPU should read ALS, identify the source for the interrupt and then rewrite the mask bits to re-enable the IRQ signal.
8	48	RES	**RESET (Schmitt Input).** Asynchronous device reset. A logic-high signal should be applied during power-up to bring the MT90840 internal circuitry to a defined state. Serial and parallel TDM outputs (STo0-7, STi0-7, and PDo0-7) are held in high-impedance state after reset until programmed otherwise. This input must be held low during normal operation.
9	49	IC	Internal Connection. The user must connect this pin to V_{SS}. This pin must remain low for the MT90840 to function normally, and to comply with IEEE 1149 (JTAG) boundary scan requirements. This pin is pulled low internally when not driven.
10, 26, 27	1-4, 27-31 50-54 76-80	NC	No Connection.
13-20	57-64	STi0-STi7	**Serial Inputs 0 to 7 (Bidirectional)**. Serial TDM data-streams at 2.048, 4.096 or 8.192 Mbps, with 32, 64 or 128 channels respectively per stream. For 2.048 and 4.096 Mbps applications, streams STi0-STi7 can be used, while for 8.192 Mbps, only streams STi0-STi3 are used (512 channel limit). These eight bidirectional lines can be programmed as inputs (default) or outputs on a per-channel basis.

Pin Description (continued)

Pin #		Name	Description
84	100		
21	65	C4/8R1	**Serial Clock Reference Input 1.** When enabled by the C4/8R bit (high) in the TIM Register, this input receives the 4.096 or 8.192 MHz serial port clock reference. If the C4/8R bit is set low, or if the INTCLK bit is set high, this input is ignored by the MT90840. In Timing Mode 1 (TM1), or at 8.192 MHz, the C4/8 input is used directly to shift data in and out of the serial port. In Timing Mode 2 (TM2) at 4.096 MHz, the C4 input from an external clock source (e.g. a PLL locked to an 8 kHz reference) is phase-corrected by the MT90840, and used to generate the serial port SPCKo and F0 outputs. In Timing Modes 3 and 4 (TM3 and TM4) this input is not used. For more details on the use of this signal, see the description of Timing Mode 1 and Timing Mode 2.
22	66	F0i/o	Serial Port Frame Synchronization (Bidirectional). This 8 kHz frame pulse signal indicates the TDM 125 µsec frame boundary on the serial data port. This pin is compatible with both ST-BUS/MVIP and GCI formatted framing signals. In TM1 this pin is an input, and the MT90840 senses the polarity of this frame pulse and automatically adapts the serial data port timing to the applicable format (ST-BUS or GCI). In TM2 with SFDI =1 this signal is an input, and its expected format is determined by the SPFP bit in the GPM Register. In TM2 (with SFDI =0), and in TM3, this signal is an output, generated from the internal timing and synchronized to the SPCKo output clock. The polarity of the F0 pulse is determined by the SPFP bit in the GPM Register. In TM4 this pin is not used.
23	67	C4/8R2	**C4/8R2 Serial Clock Reference Input 2.** When enabled by the C4/8R bit (low) in the TIM Register, this input receives the 4.096 or 8.192 MHz serial port clock reference. If the C4/8R bit is set high, or if the INTCLK bit is set high, this input is ignored by the MT90840. (See pin description for C4/8R1.)
28-31	70-73	CTo3-CTo0	**External Control Lines 3 to 0 (Output).** Output signals generated from the MT90840 Transmit Path Connection Memory (TPCM). The four serial CTo output lines represent the contents of the four CT bits in the TPCM, and are clocked at the parallel port rate (up to 19.44 MHz). See Per-Channel Functions section.
34-41	81-88	PDo7-PDo0	**Parallel Data Output Port 7 to 0 (Output)**. These eight outputs carry the parallel port data bytes in the transmit direction and operate at data rates up to 19.44 Mbyte/s.

Pin Description (continued)

Pin #		Name	Description
84	**100**		
42	89	PPFTi/o	**Parallel Port Framing, Transmit (Bidirectional).** This signal delineates the start of a new data frame at the PDo0-7 lines on the transmit parallel port. Normally an output, when the PFDI bit in the TIM Register is set high PPFT becomes an input, and is used to receive the frame reference from another MT90840. Used in all timing modes except TM3.
45-52	92-99	PDi7-0	**Parallel Data Input Port 7 to 0 (Input)**. These eight inputs carry the parallel port data bytes in the receive direction and operate at data rates up to 19.44 Mbyte/s.
55	6	PCKR	**Parallel Port Clock, Receive (Input).** This is a 19.44, 16.384, or 6.48 MHz clock input. It might typically be provided by a high speed framer. PCKR clocks in data on the receive parallel port (PDi7-0 and PPFRi). In Timing Modes 2, 3, and 4, PCKR clocks both the transmit and receive parallel ports.
56	7	PCKT	**Parallel Port Clock, Transmit (Input**). This is a 19.44, 16.384, or 6.48 MHz clock input. It might typically be provided by a high speed framer. In TM1 PCKT clocks out the data on the transmit parallel port (PDo0-7, CTo0-3, and PPFTo). In TM2, TM3, & TM4, this input is ignored.
57	8	PPFRi	**Parallel Port Framing, Receive (Input)**. This 8 kHz frame pulse input determines the start of a new frame at the PDi0-7 lines of the receive parallel port. It might typically be connected to the frame pulse output of a high speed framer. In TM3, PPFRi is the frame sync reference for both the transmit and receive parallel ports.
58	9	TDI	**Test Data** (**Input**). JTAG serial test instructions and data are shifted in on this pin on rising TCK. This pin is pulled high internally when not driven.
59	10	TRST	**Test Reset** (**Input**). Asynchronously initializes the JTAG TAP controller, placing it in the *Test-Logic-Reset* state. This pin is pulled high internally when not driven. This pin should be pulsed low on power-up, or held low continuously, to ensure that the MT90840 is in the normal functional state, and not the test state.
60	11	TCK	**Test Clock** (**Input**). Provides the clock to the JTAG test logic. This pin is pulled high by an internal pull-up when not driven.
61	12	TMS	**Test Mode Select** (**Input**). JTAG signal that controls the state transitions of the TAP controller, sampled on rising TCK. This pin is pulled high by an internal pull-up when not driven.
62	13	TDO	**Test Data** (**Output**). JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG scan is not enabled.
65	16	SPCKo	**Serial Port Clock (Output)** In TM2 and TM3, this is a 4.096 MHz clock output derived from the system 4.096 MHz reference. (As controlled by the C4/8R bit and the INTCLK bit in the TIM Register.) This output is used to shift data in and out of the serial port. In TM1 and TM4, this output is automatically placed in high impedance. For applications with the serial port running at 8.192 Mbps this output is not used, and an 8.192 MHz clock source must be supplied at C4/8R1 or C4/8R2.

Pin Description (continued)

Pin #		Name	Description
84	100		
66-73	17-24	STo7-STo0	**Serial Output Streams 7 to 0 (Bidirectional)**. Serial TDM data-streams at 2.048, 4.096 or 8.192 Mbps, with 32, 64 or 128 channels respectively per stream. For 2.048 and 4.096 Mbps applications, streams STo0-STo7 can be used, while for 8.192 Mbps, only streams STo0-STo3 are used (512 channel limit). These eight bidirectional lines can be programmed as inputs or outputs (default) on a per-channel basis.
76-83	32-39	AD0-AD7	**Multiplexed Address/Data Bus (Bidirectional**). These I/O lines provide an 8-bit interface to a microprocessor for control and monitoring of the MT90840. These pins function as eight input address lines to the Address Latch circuit as well as eight data I/O lines.
84	40	$R/\overline{W}$ \ $\overline{WR}$	**Read/Write \ Write (Input)**. In Motorola multiplexed-bus mode this input is $R/\overline{W}$, which controls the direction of the data bus lines (AD0-AD7) during a microprocessor access. In Intel/National multiplexed-bus mode this input is $\overline{WR}$, an active low signal which configures the data bus lines (AD0-AD7) as inputs during a microprocessor write access.
1,11 24,32, 43,53, 64,74	15,25, 41,55, 68,74, 90,100	V_{SS}	**Ground**.
2, 12, 25,33 44,54, 63,75	5, 14, 26,42 56,69, 75,91	V_{DD}	+5 Volt Power Supply.

Functional Description

The MT90840 Distributed Hyperchannel Switch is a large switching, multiplexing, and rate-adapting device. The MT90840 bridges serial-bus telecom components, using the Zarlink ST-BUS or other industry-standard serial buses, onto a higher speed “backbone”. Mixed data, voice and video signals can be time-interchanged or multiplexed from serial Time Division Multiplexed (TDM) streams onto a high speed parallel bus. The parallel bus can be used for interconnect, or an external framer can be connected to the parallel bus to access serial isochronous backbones operating at up to 155 Mbps SONET rates (STS-3).

The MT90840 Distributed Hyperchannel Switch supports real-time multimedia applications through constant delay switching. Multimedia data at N x 64 kbps rates uses N bytes (“time slots”, or “channels”) per 125 μsec frame. This is also referred to as hyperchannel data. To ensure the integrity of data at N x 64 kbps rates, the network must ensure that the N bytes in a given input frame remain together as a frame, and arrive at the destination as a frame. The MT90840 supports this requirement by providing constant delay (frame integrity) which ensures that the multiple time slots of associated data remain in the intended order.

Total TDM channel capacity of the MT90840 at maximum data rates is:

- 512 serial input time slots,
- 512 serial output time slots,
- 2430 parallel input time slots, and

- • 2430 parallel output time slots.

The number of time slots available is dependent upon the selected data rates, and is reduced at lower data rates.

Figure 1 shows the MT90840 functional block diagram. The figure shows the TDM data paths and the device interfaces.

The MT90840 has three main TDM data paths:

- Transmit Path: serial port input (STi) to parallel port output (PDo),
- Receive Path: parallel port input (PDi) to serial port output (STo),
- Bypass and Parallel-Switching: PDi to PDo.

In addition, Zarlink Message Mode capabilities allow the user to force data on TDM output time slots and to monitor TDM input time slots through the microprocessor port.

The MT90840 has four main interfaces:

- the serial TDM bus interface (STi, STo and timing),
- the parallel TDM bus interface (PDi, PDo and timing) with programmable control outputs (CTo),
- the microprocessor (CPU) interface,
- the test interface (JTAG).

The MT90840 supports four major timing/switching modes:

- TM1/Ring Master: PDo timing slaved to STi/o timing, PDi timing elastic;
- TM2/Ring Slave: PDo and STi/o timing slaved to PDi;
- TM3/Bus Slave: PDo and PDi timing tied together, STi/o timing slaved to parallel bus;
- TM4/Parallel Switching: parallel channel switching from PDi to PDo.

Other features of the MT90840 are programmable for individual TDM channels on the serial and parallel ports (per-channel features):

- Zarlink Message Mode,
- Per-channel output enable,
- Per-channel bypass (parallel bus),
- Programmable CTo control outputs (parallel bus),
- Per-channel direction control (serial bus).

Device Operation

Time Slot Interchange Operation (Switching)

The MT90840 provides access and time slot interchange (switching) functions between the serial and parallel TDM data ports. Switching is provided on three paths: transmit (serial input to parallel output), receive (parallel input to serial output) and bypass/parallel-switching (parallel input to parallel output). Switching functions between serial data streams are not provided.

The MT90840 guarantees wideband or hyper-channel data integrity through the switch by using constant delay switching. This is done by storing a full frame (125 μsec) of data at the input rate and then, under control of the Connection Memory for that path, reading the frame at the output data rate (frame integrity). Therefore the Transmit Path and the Receive Path each have separate Data and Connection Memories.

Switching in a given data path is controlled by programming the Connection Memory for that path. Each output time slot has a control-address in the path's Connection Memory. Each input time slot has an address-value in the path's Data Memory. A given output time slot is controlled by programming the Connection Memory control-address with the address-value of the source input time slot. At the same control-address the output time slot is enabled or tri-stated and other per-channel functions set up. Thus each output time slot is individually controlled, and any given input time slot might be copied to one, several, or none of the output time slots.

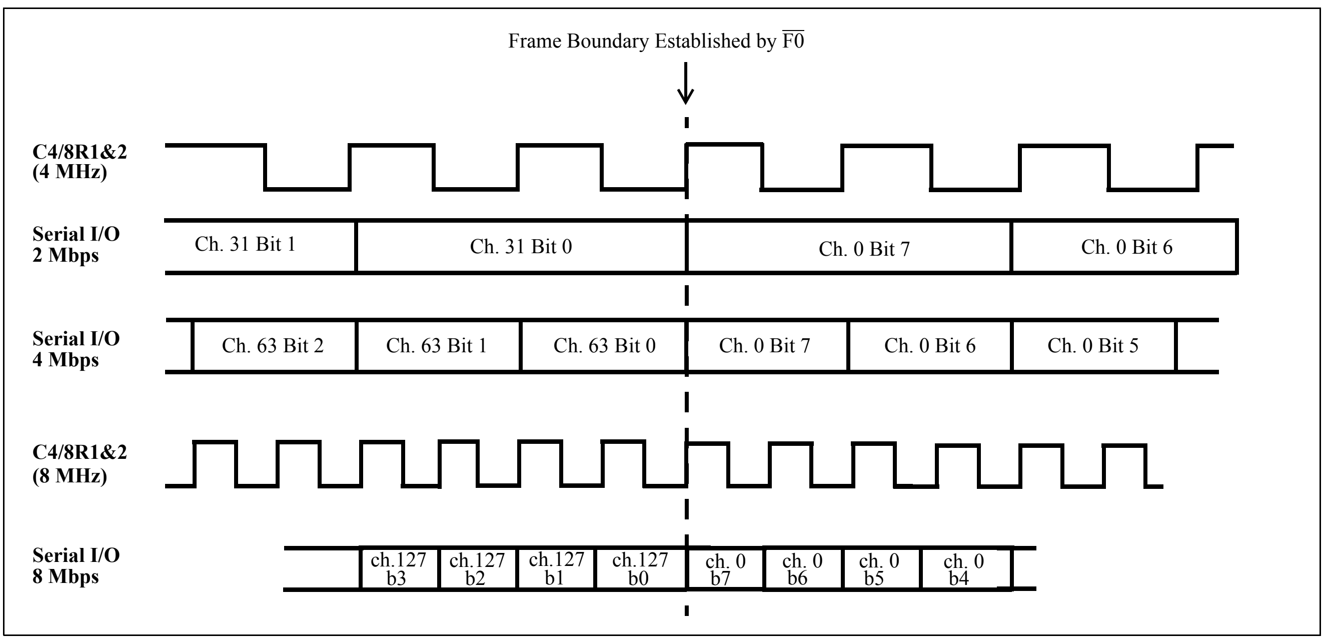

Figure 3 - Serial Port Interface Functional Timing

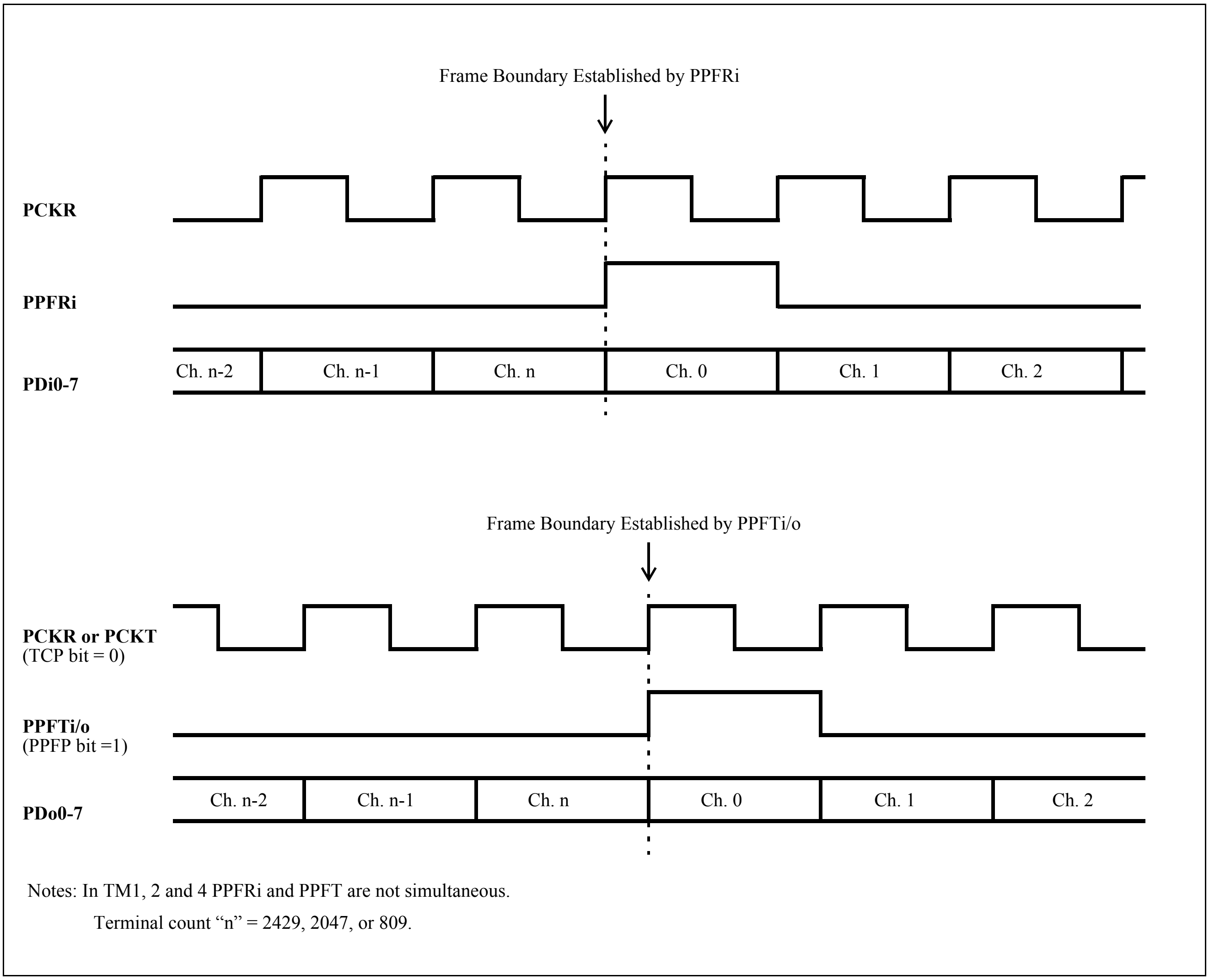

Figure 4 - Parallel Data Port Functional Timing

Transmit Path

The Transmit Path is from the serial inputs, through the Transmit (Tx) Path Data Memory, to the parallel outputs (PDo0-7). This path is controlled by the contents of the Tx Connection Memory. The Tx Connection Memory is programmed, for each output time slot, with the address-value of the source channel to be read out of the Tx Data Memory. Up to 512 channels of serial input can be switched to up to 2430 channels of parallel output.

Transmit Path Connection Memory

The Tx Path Connection Memory is structured as 2430 words of 16 bits. This supports up to 2430 DS0 channels for parallel rates up to 19.44 Mbyte/s (155 Mbps). The Tx Path Connection Memory is accessed as two-sub memories: High and Low. The Connection Memory Low (2430 X 8) is the low byte of the word, and is programmed with the address-value of the serial-input source channel. The Connection Memory High (2430 x 8) is the high byte of the word. Connection Memory High holds the high-order bit(s) of the source address-value, and is also programmed to control per-channel functions such as output driver-enable and programmable control outputs.

Transmit Path Data Memory

The Tx Path Data Memory is structured as 512 words of 8 bits. Serial input time slots are converted to parallel bytes and copied to the Tx Path Data Memory sequentially, serial-stream by serial-stream. The lowest address of the Tx Path Data Memory is STi0-channel0, the next is STi0-channel1, and so on. At 2 Mbps, with 32 channels per STi pin, STi1-channel0 would be 32 addresses higher than STi0-channel0. The Tx Path Data Memory is read out to the parallel outputs by the Tx Connection Memory.

Receive Path

The Receive Path is from the parallel inputs (PDi0-7), through the Receive (Rx) Path Data Memory, to the serial outputs. This path is controlled by the contents of the Rx Path Connection Memory. The Rx Path Connection Memory is programmed, for each output time slot, with the address-value of the source channel to be read out of the Rx Path Data Memory. Up to 2430 channels of parallel input can be switched to up to 512 channels of serial output. Each output byte, whether switched data or message mode data, is read from memory and passed to the parallel-to-serial converters, and then driven out the serial port.

Receive Path Connection Memory

The Rx Path Connection Memory is structured as 512 words of 16 bits. This supports up to 512 DS0 channels. The Rx Path Connection Memory is accessed as two sub-memories: High and Low. The Connection Memory Low (512 x 8) is the low byte of the word, and is programmed with the address-value of the parallel-input source channel. The Connection Memory High (512 x 8) is the high byte of the word. Connection Memory High holds the high-order bits of the source address-value, and is also programmed to control per-channel functions such as output driver-enable and direction-control.

Receive Path Data Memory

The Rx Path Data Memory is structured as 2430 words of 8 bits (1 byte). Parallel input time slots are copied to the Rx Path Data Memory sequentially. The Rx Path Data Memory is read out to the serial port by the Rx Path Connection Memory.

Bypass/Parallel-Switching Path

The Bypass/Parallel Switching path is from parallel input to parallel output. Data received at the parallel inputs (PDi0-7) is copied to the Rx Path Receive Memory, and may be passed to the parallel outputs (PDo0-7) under control of the Tx Path Connection Memory.

Bypass

In ring timing modes (TM1 and TM2) this is a bypass path. When the Bypass bit (PPBY) for a given parallel output channel is set in the Tx Path Connection Memory, the same-address parallel input channel is copied (bypassed) to that parallel output channel. This allows data channels not destined for the local node to be bypassed to the output port and down the ring. “Broadcast” channels destined for every node can also be bypassed, since PPBY is an output control, and it does not affect the availability of the Receive Parallel data for switching to the serial port or monitoring through the CPU interface.

Parallel Switching

In Parallel Switching Mode (TM4) this is a switching path, and the Tx Path Connection Memory is programmed to switch parallel inputs to parallel outputs. For each parallel output channel control-address, the Tx Path Connection Memory is programmed with the 12-bit address-value of the desired parallel input channel.

Serial Data Port

The serial port consists of 16 bidirectional serial data lines (STo0-7, STi0-7), two reference input clock pins (C4/8R1, C4/8R2), one serial clock output (SPCKo) and a bidirectional frame synchronization signal (F0i/o). The STi pins are the default inputs, but the user can program the direction of the pins on a per-channel basis in the Rx Path Connection Memory.

The serial port modes are controlled by the DR bits and the FDC bit in the IMS register, and are:

- 2.048 Mbps Balanced: 8 inputs and 8 outputs per serial time slot (FDC = 0),
- 2.048 Mbps Add/Drop: 16 serial I/O individually programmed per time slot (FDC = 1),
- 4.096 Mbps: 8 inputs and 8 outputs per time slot,
- 8.192 Mbps: 4 inputs and 4 outputs per time slot.

Figure 3 shows the different data rate configurations for the MT90840 serial port.

In addition the user can specify the placement and polarity of the output frame pulse F0o as ST-BUS or GCI compatible, using the SPFP bit in the GPM register. In TM1, the MT90840 automatically detects ST-BUS or GCI serial bus modes, based on the polarity of F0i. The user can also specify which of the two input clock pins - C48R1 or C48R2 - to use as the serial port clock source, using the C4/8R bit in the TIM register.

The user can define the direction of each time slot of the serial port. This per-channel direction control feature is controlled by the DC bit in the Rx Path Connection Memory High. This is ideal for applications in Computer Telephony Integration (CTI) where per-channel direction control is required within telephony servers.

2.048 Mbps Balanced Mode

The 2.048 Mbps Balanced mode has 8 inputs and 8 outputs active during each serial-byte-period or “time slot”. At 2.048 Mbps, each STi/o pin has 32 8-bit channels per 125 µsec frame, with each individual channel at 64 kbps. (1/125µsec X 8 bits = 64 kbps, 32 x 64 kbps = 2.048 Mbps). This mode supports 256 serial input channels and 256 serial output channels. This mode is “balanced” in that there are always 8 inputs and 8 outputs during a time slot. If a specific time slot in an output stream (e.g. STo0-channel7) is programmed in the Rx Path Connection Memory as an input, the corresponding time slot on the equivalent input stream (i.e. STi0-channel7) is automatically an output. The serial clock for this mode is 4.096 MHz.

2.048 Mbps Add/Drop Mode

The 2.048 Mbps Add/Drop mode (FDC bit high) has 16 bidirectional streams active during each time slot. This mode allows up to 512 input channels, or up to 512 output channels, or any mix of channels totalling 512 channels. Per-channel direction control in the Rx Connection Memory specifies the direction of all 512 serial channels from STo0-channel0 up to STi7-channel31.

4.096 Mbps Mode

The 4.096 Mbps mode has 8 inputs and 8 outputs active during each time slot. At 4.096 Mbps each STi/o pin has 64 channels of 64 kbps. This mode supports 512 serial input channels and 512 serial output channels. The serial clock is 4.096 MHz. Per-channel direction control in this mode is the same as the 2.048 Mbps balanced mode.

8.192 Mbps Mode

The 8.192 Mbps mode has 4 inputs and 4 outputs active during each serial byte period. At 8.192 Mbps, each STi/o pin has 128 channels. This mode supports 512 serial input channels and 512 serial output channels. The serial clock for this mode is 8.192 MHz. Per-channel direction control in this mode is the same as the 2.048 Mbps balanced mode.

Serial Port Clock Signals

Depending on the Timing Mode selected, the serial port clock is either an input, or an output derived from a reference clock. In modes where the serial clock is derived by the MT90840 from a reference clock, the serial port clock output appears at SPCKo. The reference clock is either PCKR (if INTCLK is high), or one of C4/8R1 or C4/8R2. The C4/8R bit of the Timing Mode Register is used to select which of C4/8R1 or C4/8R2 will be the clock source or reference pin. Switching between clock sources during device operation will cause temporary TDM data errors.

Internal 4.096 MHz Clock Generator

For TM2 applications running at 19.44 or 16.384 MHz rates on the parallel port, an internal divider can be used to generate a 4.096 MHz clock from the PCKR clock input. The internal divider can not be used in applications where the parallel port operates at 6.480 Mbyte/s rates. The INTCLK bit in the TIM Register enables the internal divider, and the SPCKo output (and internal 4.096 MHz clocks) are driven by the clock divided-down from PCKR. At 16.384 MHz, this is a simple divide-by-4, and the SPCKo output jitter will depend on the PCKR input jitter. At 19.44 MHz, the SPCKo output jitter will be larger as the divider switches between rising and falling edges of PCKR. The serial port timing and F0o frame pulse are tightly slaved to PPFRi when INTCLK is set high.

Serial Frame Pulse

In TM1, the MT90840 receives the frame reference (F0i) from an external source, and the MT90840 senses the polarity of the frame pulse and adapts the device timing to the appropriate (ST-BUS or GCI) format.

In TM2 and TM3, the MT90840 outputs the serial port frame pulse (F0o). Positive (GCI) or negative (ST-BUS) frame pulse formats, and the associated clock polarity, can be selected for the F0o signal by programming the SPFP bit in the GPM Register. This flexibility allows the MT90840 to be employed with different serial bus formats.

In applications which require a large number of serial channels in TM2, it is possible to operate multiple MT90840s in parallel using the SFDI control bit (in the TIM register). To allow the MT90840s to synchronize their internal timing, all of the MT90840s are connected to the same C4/8 reference source, and one MT90840 in normal TM2 (SFDI set low) supplies F0 to one or more MT90840s in TM2 with SFDI set high. With SFDI set high, F0 becomes an input, and this allows the MT90840 driving F0 to control the timing of one or more other MT90840s. If the internal 4.096 MHz clock divider is used (INTCLK high) it is not necessary to use the SFDI control, as the serial port timing and F0o frame pulse of each parallel MT90840 will be tightly slaved to PPFRi when INTCLK is set high.

Should the input framing at F0i cease while the C4/8 clock continues to run, the MT90840 will continue to function as if the frame pulse was asserted after the normal number of clock cycles (free run). If F0i re-commences the MT90840 will immediately sync to F0i, but changes in the F0i interval will temporarily disrupt the TDM data streams. If the F0i input is held asserted, the serial I/O will “lock up” and operation will be disrupted.

Parallel Data Port

The MT90840 parallel port is composed of an 8-bit wide Parallel Data Output Port (PDo0-7), a 4-bit wide Control output port (CTo0-3), an 8-bit wide Parallel Data Input Port (PDi0-7), a Receive Frame sync signal (PPFRi) and a Transmit Frame sync signal (PPFT), and Transmit (PCKT) and Receive (PCKR) Clocks.

The Parallel Port Rates are controlled by the PPS bits in the IMS register, and are:

- 19.44 Mbyte/s (2430 channels),
- 16.384 Mbyte/s (2048 channels), and
- 6.48 Mbyte/s (810 channels).

The user can further specify the features of the parallel TDM port, including:

- the edge of the parallel port clock used to transmit data and PPFTo (see TCP bit in the TIM register),
- the polarity of the Parallel Port Frame Transmit pulse PPFT (see PPFP bit in the GPM register),

- the use of PPFT (normally an output) as an input in TM1, if the application requires multiple MT90840 devices to operate in parallel (see PFDI bit in the TIM register).

The parallel port of the MT90840 is flexible enough to interface to a variety of applications. It can be connected to a framer to access a serial transport backbone running at up to 155 Mbps. It can be connected to a backplane-type parallel bus. It can share a parallel bus with other devices, using the control outputs (CTo0-3) and the per-channel tristate function to share access to the bus.

Parallel Port Clock Signals and Framing

The MT90840's PPFRi (Parallel Port Frame pulse Receive input) and PPFTi/o (Parallel Port Frame pulse Transmit i/o) signals synchronize the MT90840 to the high speed data frame. Receive data is clocked in at the Parallel Data inputs (PDi0-7) by the Parallel port Receive ClocK (PCKR), as framed by Receive Parallel Port Frame input (PPFRi). In TM2, TM3 and TM4, PCKR also clocks the Parallel Data outputs (PDo0-7), with the framing in TM2 and TM4 indicated by the PPFTo output. In TM1, the Parallel Data outputs are clocked out by PCKT, with the framing indicated by PPFTo. Alternatively, the Transmit framing can be controlled by the PPFTi input if the PFDI bit in the TIM register has been set high, to enable multiple MT90840s to operate in parallel in TM1.

Should the input framing at PPFRi cease while the PCKR clock continues to run, the MT90840 will continue to function as if the frame pulse was asserted after the normal number of clock cycles (free run). If PPFRi re-commences, the MT90840 will immediately sync to PPFRi, but any change in the framing interval will temporarily disrupt the TDM data streams, and trigger the PPCE interrupt bit. PPCE will be triggered by PPFRi moving from the expected time, but PPCE will not be triggered by a missing PPFRi. If the PPFRi input is held asserted, the parallel I/O will “lock up” and operation will be disrupted (including CPU access to the TPCM).

The PPFTi framing in TM1 with PFDI=1 operates similarly, using PCKT, but the PPCE interrupt does not monitor PPFTi. Instead, the TXPAA bit indicates that the PPFTi input is out of phase with F0i.

Output Driver Enable Control Capability

The MT90840 provides a bit (ODE) in the IMS Register that places all data outputs of the device (parallel and serial) in a high impedance state. The ODE bit (Output Drive Enable) is automatically set low by the reset input pulse applied to the device during system power up. When low, the ODE bit disables all TDM outputs of the MT90840 while Connection Memory initialization is performed by the CPU. This function is useful to avoid data collision when the MT90840 is sharing a transmit parallel bus with other devices. When ODE is set high, individual parallel and serial port time slots are controlled by the OE bits in TPCM High and RPCM High.

Timing and Switching Control

The MT90840 supports four major timing/switching modes:

- TM1/Ring Master: PDo timing slaved to STi/o timing, Receive Path has elastic buffer enabled;
- TM2/Ring Slave: STi/o timing slaved to PDi timing, fixed delay in Receive Path;
- TM3/Bus Slave: PDo and PDi tied together, STi/o timing slaved to parallel bus timing;
- TM4/Parallel Switching: 2430 (or 2048) channel switching from PDi to PDo.

The TM1-0 bits in the TIM Register are used to select the timing modes. The PFDI and SFDI bits in the same register can be used to enable parallel-device sub-modes of TM1 and TM2 respectively. In all MT90840 timing modes, the throughput delay when performing time interchange functions of grouped channel data is constant, maintaining the frame integrity of the input and output data.

Timing Mode 1 (TM1) - Ring Master

Asynchronous Parallel Port With ST-BUS Clock Master

Timing Mode 1 is used where the main TDM clock reference resides on the serial port side of the system. (An example is a node which is the clock master on a ring network.) Timing on the transmit parallel port is tightly tied to the serial port. The receive parallel port timing is elastic; there is an elastic buffer in the Receive Path and the Bypass Path. See Figure 5a for a connection example.

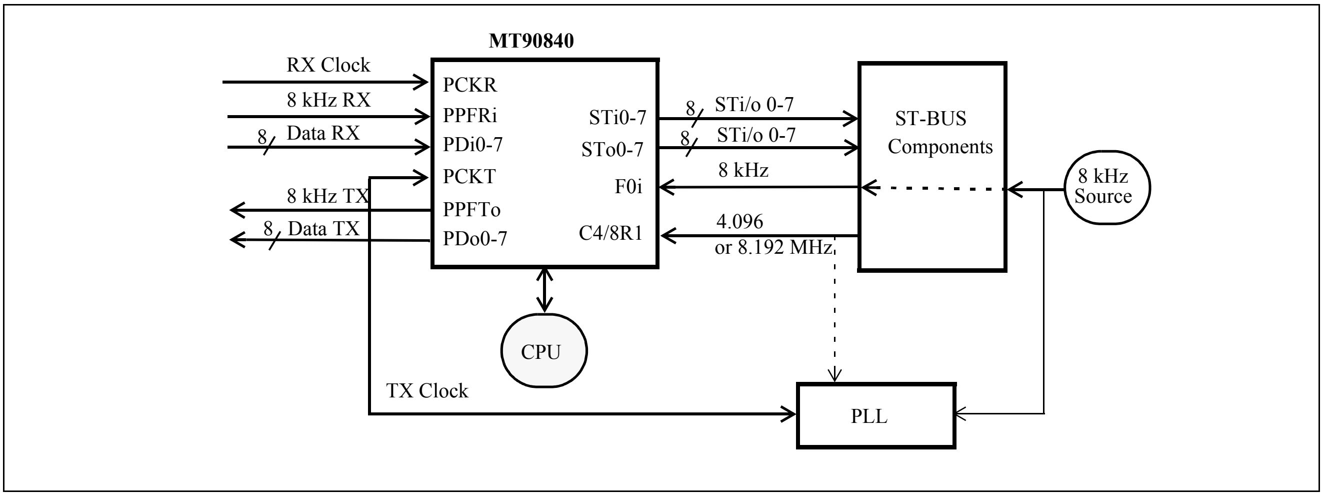

Figure 5a - Timing Mode 1 Configuration

In TM1, the MT90840 receives the serial port frame pulse (F0i) and serial clock (C4/8R1 or C4/8R2). The MT90840 then generates the parallel port output frame pulse (PPFTo) synchronized to F0i. The transmit parallel port is fixed in phase relative to the serial port. (A fixed offset of 3.8 μsec exists between F0i and PPFTo due to serial-to-parallel conversion.) The transmit path does not provide an elastic buffer, and therefore the parallel port TX clock (PCKT) must be tightly locked (in frequency) to the serial port C4/8 and F0i clocks. (Jitter less than +/- 100nsec.)

The receive parallel port timing may be of any phase relative to the serial and transmit-parallel ports in TM1. This allows for flexible round-trip data delays in star or ring type networks. An elastic buffer on the receive parallel port compensates for the difference in phase between PPFRi/PCKR and F0i/C4. The elastic buffer can also tolerate up to 50 μsec +/- 25 μsec) of clock drift and jitter before the buffer re-syncs and Rx Path data is corrupted. (Data corruption is flagged by the FSA interrupt source.) The Bypass Path data (PDi to PDo) also passes through the elastic buffer in TM1.

In TM1, the MT90840's SPCKo clock output is not used.

TM1 Multiple-MT90840 Sub-Mode (PFDI)

For TM1 applications which require more serial channels than are provided by a single MT90840, it is possible to operate multiple MT90840 in parallel. To do this, one MT90840 must control the F0i-to-PPFTo timing (normal TM1), and the remaining MT90840s must synchronize to the first by using PPFTi as an input reference. The device providing the reference will have the PFDI bit in the TIM Register set low (normal TM1). All other MT90840s will have PFDI set high (forcing PPFT to be an input).

Figure 5b shows this mode using two MT90840s; additional MT90840s (with PFDI set high) may be added. This sub-mode allows the serial ports of the multiple MT90840 to share one timing source, and the synchronized parallel output ports to be connected together on one bus.

The TM1 Multiple-MT90840 sub-mode is not available for operation at 6.48 Mbyte/s.

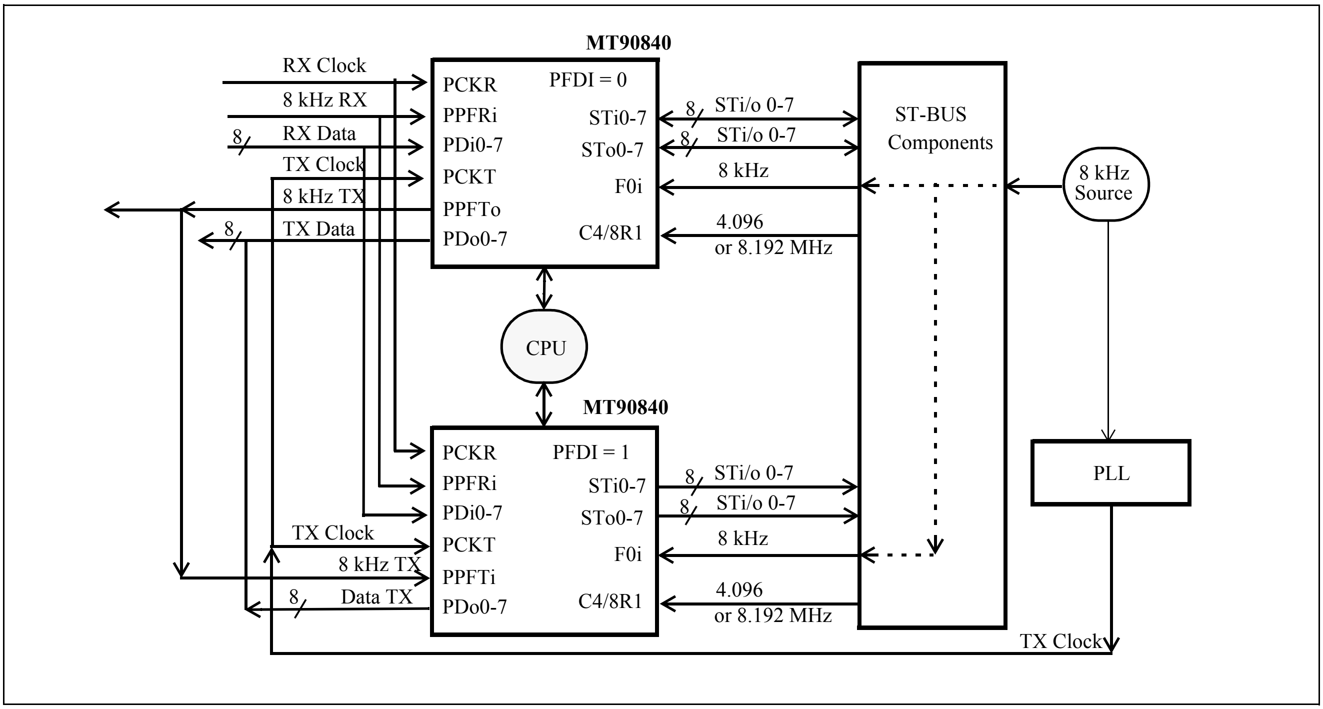

Figure 5b - TM1 Multiple-MT90840 Configuration

Timing Mode 2 (TM2) - Ring Slave

Asynchronous Parallel Port With ST-BUS Clock Slave

Timing Mode 2 is used where the main TDM clock reference resides on the parallel port side of the system. (An example is a node on a ring which is slaved to the ring clock.) Timing on the serial port is tightly tied (slaved) to the receive parallel port, and the transmit parallel port is clocked by the receive parallel port clock. In TM2, the PCKT input is not used. See Figure 6a for a connection example.

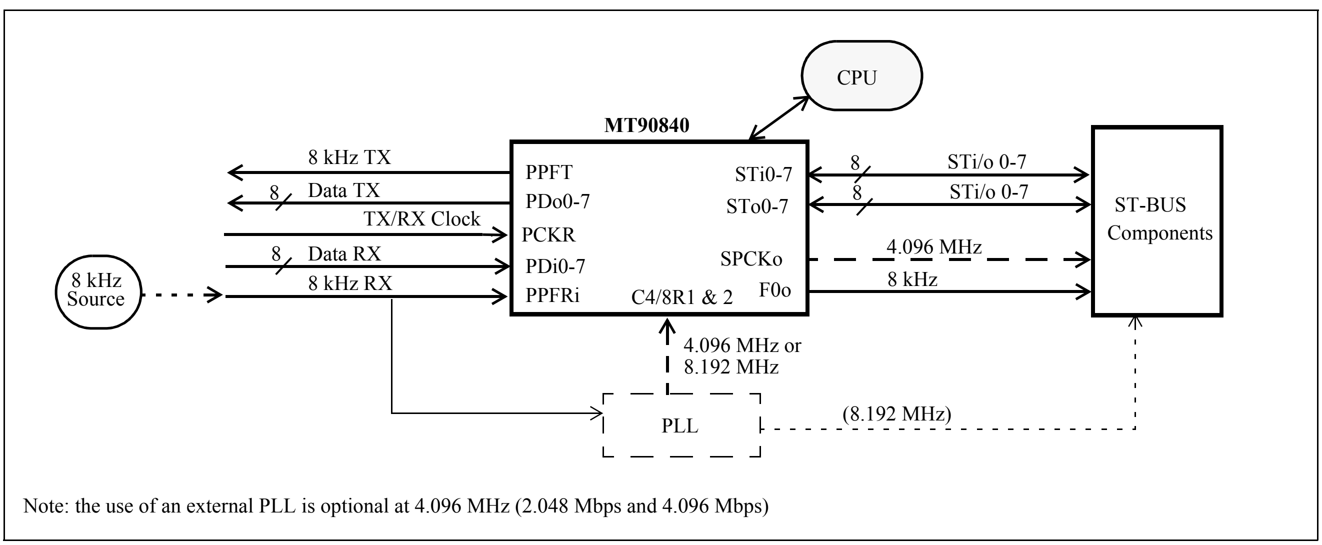

Figure 6a - Timing Mode 2 Configuration

In TM2, the MT90840 timing is controlled by the parallel port frame pulse (PPFRi) and clock (PCKR). The MT90840 generates the parallel port output frame pulse (PPFTo) and the serial port output frame pulse (F0o) locked to PPFRi. Both the transmit parallel port and the serial port are fixed in phase relative to the receive parallel port, and therefore no elastic buffer is required. A fixed offset exists between PPFRi and F0o due to parallel-to-serial conversion, and between F0o and PPFTo due to serial-to-parallel conversion delay. Total offset between PPFRi and PPFRo is about 12 μsec (and the Bypass Path data delay is therefore also about 12 μsec).

The transmit path does not provide an elastic buffer, and therefore the serial port clock must be tightly locked (in frequency) to the parallel port clock (PCKR). (Jitter less than +/- 100nsec.) This may be achieved in one of two ways: use of the internal clock divider (INTCLK set high), or use of an external PLL or DPLL, with C4 phase-correction performed by the MT90840.

Internal 4.096 MHz Clock Divider

For TM2 applications at 19.44 or 16.384 MHz rates on the parallel port, and 4.096 MHz on the serial port, the internal clock divider can be enabled. The clock divider can generate the required serial port clock outputs from the parallel port clock inputs. When enabled in TM2, the clock divider will provide 4.096 MHz (SPCKo) and 8 kHz (F0o) timing to the serial port that is rigidly locked to the PCKR and PPFRi clocks at the parallel port. The clock divider is enabled by setting the INTCLK bit high (in the TIM Register). The clock divider can not be used in applications where the parallel port operates at 6.480 Mbyte/s rates.

External PLL and C4 Phase-Correction

The MT90840 also supports the use of an external PLL (e.g. MT9041/2) to generate 4.096 or 8.192 MHz from the parallel port timing reference. At 4.096 MHz the generated clock must be input to the MT90840 (at C4/8R1 or C4/8R2) for phase monitoring and correction. The phase-corrected 4.096 MHz clock is then output on the SPCKo pin. Should the phase of the C4clock input (relative to the PPFRi framing input) drift more than approximately +/- 100nsec, the MT90840 will apply an additional correction and indicate possible data corruption with the RXPAA interrupt source. At 8.192 MHz, the generated clock is input to the MT90840 (at C4/8R1 or C4/8R2), and is also supplied directly to the serial bus (the SPCKo output is not used at 8.192 MHz). The serial port frame pulse (F0o) will be slaved to the parallel port frame pulse (PPFRi), and will be clocked out by SPCKo, or the 8.192 MHz clock, as appropriate.

TM2 Multiple-MT90840 Sub-Mode (SFDI)

For TM2 applications which require more serial channels than are provided by a single MT90840, it is possible to operate multiple MT90840s in parallel. Multiple-MT90840 operation is automatic if INTCLK is selected, but if an external PLL is used, the serial port timing of the MT90840s must be synchronized. To do this, one MT90840 controls the PPFRi-to-F0o timing and C4 phase-control (normal TM2), and the remaining MT90840s must synchronize to the first by using F0 as an input reference. The device providing the reference will have the SFDI bit in the TIM Register set low (normal TM2). All other MT90840s will have SFDI set high (forcing F0 to be an input).

Figure 6b shows this mode using two MT90840s; additional MT90840s (with SFDI set high) may be added. This sub-mode allows the serial ports of the multiple TM2 MT90840s to share one timing source. The transmit parallel port outputs are always synchronized to PPFRi in TM2, so the multiple MT90840s can also be connected together on one parallel output bus.

The TM2 Multiple-MT90840 sub-mode is not available for operation at 6.48 Mbyte/s.

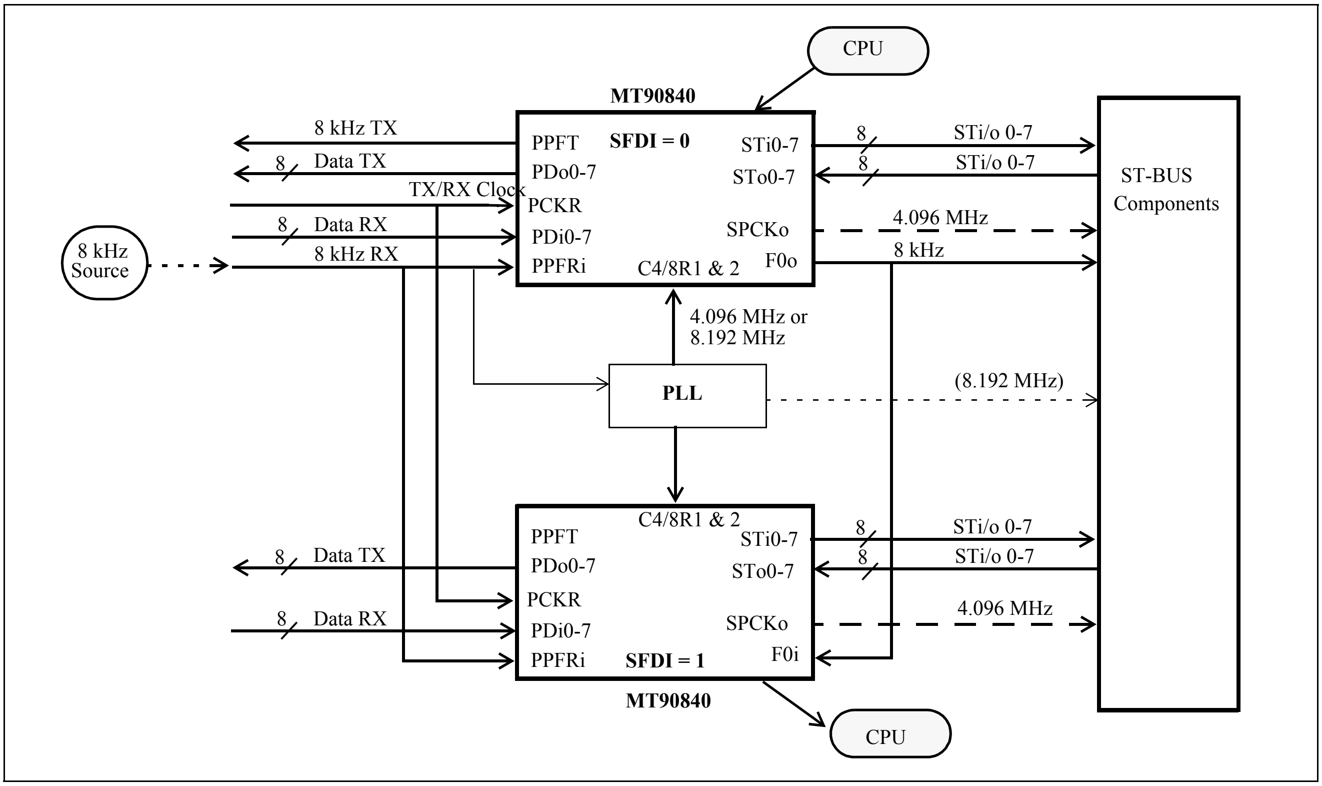

Figure 6b - TM2 Multiple-MT90840 Configuration

Timing Mode 3 (TM3) - Bus Slave

Synchronous Parallel Port With ST-BUS Clock Slave

Timing Mode 3 is used where the main TDM clock reference resides on the parallel port side of the system, and where the receive parallel port and the transmit parallel port are aligned. (An example is a node on a backplane.) Timing on the serial port is tightly tied to the receive parallel port, and the transmit parallel port is clocked by the receive parallel port clock. In TM3, PCKT and PPFTo are not used. See Figure 7 for a connection example.

In TM3, the MT90840 timing is controlled by the parallel port frame pulse (PPFRi) and clock (PCKR). The MT90840 generates the serial port output frame pulse (F0o) locked to PPFRi. TM3 is similar to TM2 with two main differences: the parallel Bypass Path is disabled, and the parallel port receive and transmit buses are synchronized and both aligned with PPFRi. A fixed offset exists between F0o and PPFRi due to serial-to-parallel conversion. The MT90840 will align F0o so that it proceeds PPFRi by 3.8 μsec.

In TM3 the internal clock divider circuit is always enabled, regardless of the state of the INTCLK bit (C4/8R1 and C4/8R2 are unused). Therefore TM3 is limited to 19.44 and 16.384 Mbyte/s parallel port rates, and 2.048 and 4.096 Mbps serial port rates.

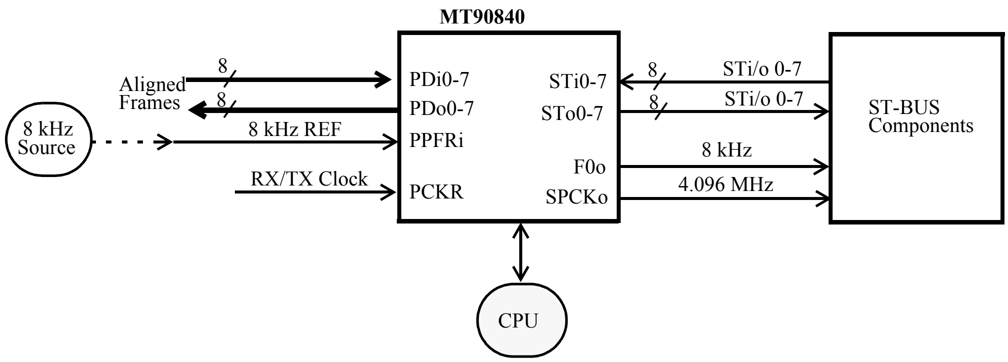

Figure 7 - Timing Mode 3 Configuration

Timing Mode 4 (TM4) - Parallel Data Switching

Timing Mode 4 is used to provide switching of up to 2430 parallel input channels to the same number of parallel output channels. Parallel TDM data is clocked in at PDi0-7 by PCKR, framed by PPFRi. Switching is performed as programmed in the Tx Path Connection Memory, and data is output on PDo0-7, framed by PPFTo and clocked by PCKR. See Figure 8 for connection details.

In TM4, PPFTo and PDo0-7 are offset (delayed) from PPFRi and PDi0-7 by a fixed 4 clock cycles (3.5 clock cycles if the TCP bit is high). All the serial port data and timing signals, and PCKT, are unused in TM4. The internal clock divider is used to generate an internal C4 clock to allow CPU reads from the RPDM. TM4 is only available for 19.44 and 16.384 Mbyte/s rates.

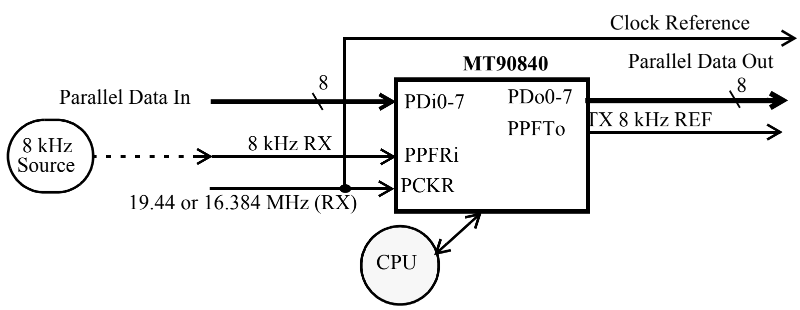

Figure 8 - Timing Mode 4 Configuration

MT90840 Throughput Delay

In many isochronous applications it is important to know and/or limit the delay of data. Table 1 summarizes the data throughput delay values for all timing modes of the MT90840. It is worth noting that the worst-case “round-trip” delays are not as large as the sum of the worst-case delays on the individual links. This is shown by the last 5 rows of Table 1, which give the delays for some representative two MT90840 setups.

MT90840 Per-channel Functions

Several functions of the MT90840 are programmable for each individual parallel channel or serial channel. Per-channel functions on the parallel port side are programmed in the Transmit Path Connection Memory High (TPCM High), and per-channel functions on the serial port interface are programmed in the Receive Path Connection Memory High (RPCM High). On the parallel port these per-channel features are Bypass, Control Outputs, Output

Enable, and Message Mode. On the serial port the per-channel features are Output Enable, Message Mode and Direction Control. These functions are generally available in all of the data rates and timing/switching modes.

Per-channel Bypass on the Parallel Port

This feature, when enabled, causes the specific individual parallel output channel at PDo to transmit the data received at the same number input channel at PDi. This can be used to perform a bypass (on a ring) or a loopback (in a star). This feature is only provided in Timing Modes 1 and 2. In TM2 the data-delay from PDi to PDo is fixed (as is the delay between PPFRi and PPFT). In TM1 the data-delay is elastic (and dependent on the timing of PPFRi and F0i).

The per-channel bypass feature is controlled by the PPBY bits of the TPCM High as explained in the register section. If the PPBY bit is HIGH at a specific TPCM address, the corresponding parallel output will transmit the data received in the corresponding input channel. When the PPBY bit is LOW, the corresponding output channel can be used for message-mode data, or for switched-data from the serial port. A bypass input channel is still copied to the Receive Path Data Memory, and may also be switched to the serial port, or read by the CPU from the Receive Path Data Memory.

The MT90840 per-channel output-enable and message-mode bits have higher priority than the PPBY bit.

Mode	Data Rates	Minimum Delay	Total Throughput Delay
TM1, TM2, or TM3 S/P	All	Dmin = 7.7 µsec Note 1	D = Dmin + 1 frame + Po - Si = 132.7 µsec + Po - Si Min. 7.7 µsec, Avg. 133 µsec, Max. 258 µsec
TM1P/S	All	Dmin = ELDmin = 4.4 µsec Note 2	D = 1 frame + ELD + So - Pi = 125 µsec + ELD + So - Pi Min. 4.4 µsec, Max. 379 µsec
TM2 P/S	All	Dmin = 4.3 µsec Note 1	D = Dmin + 1 frame + So - Pi = 129.3 µsec + So - Pi Min. 4.3 µsec, Avg. 129 µsec, Max. 254 µsec
TM3 P/S	All	Dmin = 1 frame - 7.7 µsec = 117.3 µsec	T = Dmin + 1 frame + So - Pi = 242.3 µsec + So - Pi Min. 117 µsec, Avg. 242 µsec, Max. 367 µsec
TM1 P/P (Bypass)	All	Dmin = 12 µsec + 1 frame = 137 µsec Note 2	D = 7.7 µsec + 1 frame + ELD Min.137 µsec, Max. 262 µsec
TM2 P/P (Bypass)	19.44 Mbyte/s 16.384 Mbyte/s 6.480 Mbyte/s	Note 3	D = {235 or 235.5} PCKR cycles = 12 µsec D = {199 or 199.5} PCKR cycles = 12 µsec D = {80 or 80.5} PCKR cycles = 12 µsec
TM4 P/P (Switching)	19.44 & 16.384 Mbyte/s	Dmin = {3.5 or 4} PCKR cycles (TCP bit = 1 or 0)	D = Dmin + 1 frame + Po - Pi Min. < 0.3 µsec, Avg. 125 µsec, Max. 250 µsec
TM1 S/P + TM2 P/S	All	Dmin = 12 µsec + 1 frame = 137 µsec	D = 12 µs + 2 frames + Transmission + So - Si = 262 µsec + Transmission + So - Si
TM2 S/P + TM1 P/S	All	Dmin = 12 µsec + 1 frame = 137.4 µsec	D = 12 µsec + 2 frames + Transmission + ELD + So - Si = 262 µsec + Transmission + ELD + So - Si

Mode	Data Rates	Minimum Delay	Total Throughput Delay
TM1 S/P + TM2 P/S + TM2 S/P + TM1 P/S	All	Dmin = 4 frames = 500 μsec	D = (2 X 12) μsec + 4 frames + 2 X Transmission + ELD + So - Si = {5 or more integral frames} + So - Si (Note 4)
TM1 S/P + TM2 Bypass + TM1 P/S	All	Dmin = 2 frames = 250 μsec	D = (3 X 12) μsec + 2 frames + 2 X Transmission + ELD + So - Si = {3 or more integral frames} + So - Si (Note 4)
TM3 S/P + TM3 P/S	All	Dmin = 250 μsec	D = (7.7 + 117.3) μsec + 2 frames + So - Si = 375 μsec + So - Si Min. 250 μsec, Avg. 375 μsec, Max. 500 μsec (Note 4)

Table 1 - MT90840 Throughput Delay Summary

Naming rules:
ELD: ELastic Delay, measured from PPFRi to F0i (4.4 to 129.4 μsec).
P/S: Parallel-to-Serial data path.
Pi: Parallel Input channel time, expressed in delay after PPFRi (0 to 125 μsec).
Po: Parallel Output channel time, expressed in delay after PPFTi/o (0 to 125 μsec).
S/P: Serial-to-Parallel data path.
Si: Serial Input channel time, expressed in delay after F0i/o (0 to 125 μsec).
So: Serial Output channel time, expressed in delay after F0i/o (0 to 125 μsec).
Transmission: The delay due to electronic circuits and physical media connecting the parallel ports of two MT90840s. (Assumed to be negligible in TM3.)

Note 1: Exact P/S or S/P delay depends on relative positions of PPFRi and F0 +/- 120 nsec tolerance).
Note 2: Actual TM1 P/S and P/P delay depends on elastic position of PPFRi with respect to F0i (see ELD definition).
Note 3: Bypass delay in TM2: PPFT and PDo ch.0 are co-incident with PDi ch.235 at 19.44 MHz, ch.199 at 16 MHz, and ch.80 at 6.48 MHz. (TCP = 1 delays PDo ch.0 an extra half clock-cycle in TM2).
Note 4: "Round-trip" delay from/to serial ports with the same F0 is always an integral number of frames (plus switching: So - Si).

Per-channel Control Outputs on the Parallel Port

The MT90840 provides four control outputs (CTo0-CTo3) which are synchronized to the parallel port output timing. Each of the CTo output pins is controlled by the CT0-3 bits of the TPCM High. (The CTo0 pin and bit are programmed with the Output Enable data.) The contents of the CTo bit in each TPCM High location is output on the corresponding CTo pin once every frame. See Figure 9. The control outputs can be used to control other devices, such as buffers, to allow sharing of the parallel port data bus.

Per-channel Tri-state (Serial and Parallel)

The MT90840 provides per-channel tri-state of the output pins on both the serial and parallel port. The OE bit in each address of the TPCM and RPCM determines if data will be driven during a particular time slot, or if the pin will be placed in a high-impedance state during that time slot. The OE bit overrides all other per-channel control bits.

Per-channel Message Mode (Serial and Parallel)

The MT90840 provides per-channel message mode capability on both the serial and parallel port. The MC bit in each address of the TPCM and RPCM determines if the Connection Memory Low byte is to be used as an address, or as data to be output on the particular channel (message mode). When the MC bit is HIGH, the Connection Memory Low byte is used as message data. As well as driving message data on the serial (RPCM) and parallel (TPCM) ports, the MT90840 allows the CPU to read serial or parallel data channels from the TPDM or RPDM. Applications for message mode include digital silence, proprietary signalling, and creating fixed 8 kHz framing patterns.

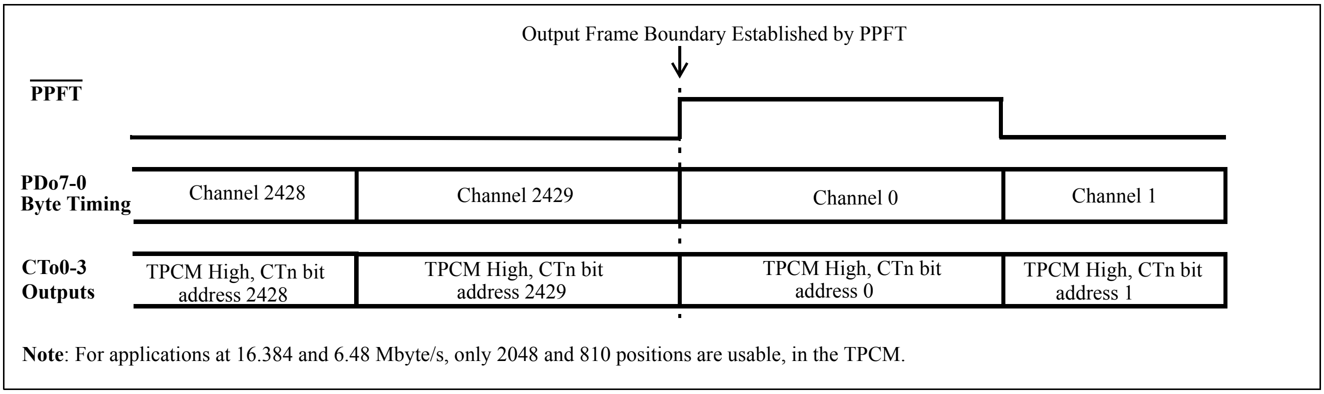

Figure 9 - Parallel Port Control Outputs, CTo0-3

Per-channel Direction Control on the Serial Port

The MT90840 provides the ability to use any nominal output serial channel as an input or as an output. The direction of each output serial channel is controlled by the DC bit in the appropriate byte of the Receive Path Connection Memory High (RPCM High). When DC is HIGH the matching channel is an output. The per-channel direction control feature of the MT90840 can be activated in one two modes: balanced, or add/drop operation.

- Balanced Operation (all serial data rates)

This mode is enabled when the FDC bit in the IMS Register is LOW. In this mode, each of the DC bits controls two serial channels: the nominal output and the nominal input. If a channel on a nominal output serial stream (STo0-7) is re-defined as an input, the same-number channel on the matching input stream (STi0-7) will be defined as an output. For example, if channel 0 on STo7 is programmed as an input (DC=0), then channel 0 on STi7 is defined as an output. Each DC-bit's state controls the direction of a channel on the nominal output stream (DC is HIGH for output), and inverse-sense controls a channel on the nominal input stream (DC is LOW for output). This is shown in Figure 10.

- Add/Drop Operation (2.048 Mbps only)

This mode is enabled when the FDC bit in the IMS Register is HIGH. In Add/Drop mode all channels on all 16 serial streams can be individually controlled, so that up to 512 channels can be either transmitted or received. As an example, if all DC bit locations of RPCM High are set HIGH, all 512 channels on STo0-7 and STi0-7 will be configured as outputs. If all DC bits are LOW, then all 512 channels will be configured as inputs. In Add/Drop mode all 512 serial channels are copied into the Transmit Path Data Memory, as inputs, regardless of the DC or OE bits. This has the effect of a “copy-back” of all serial outputs.

For more details on per-channel control functions for the serial and parallel data ports, see the TPCM High and RPCM High bits definition in the Register Description section.

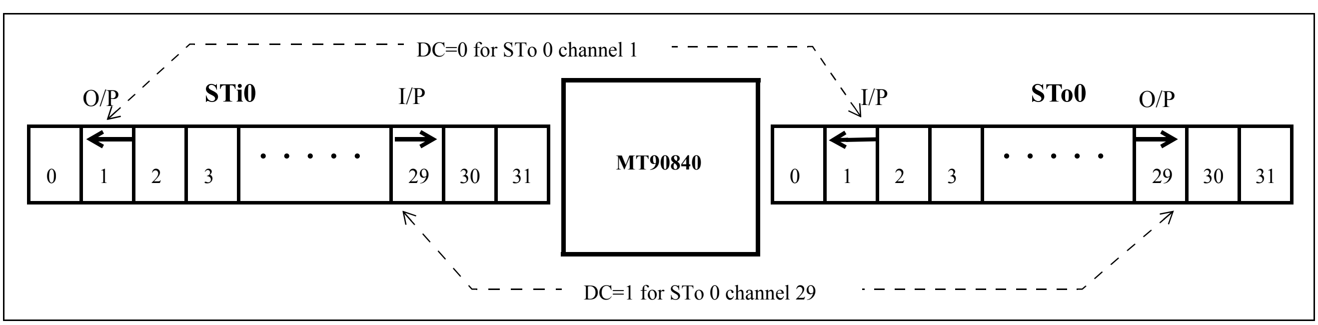

Figure 10 - Balanced Per-Channel Serial Direction Control as Determined by DC Bit

Serial Data Memory Addressing

The serial port mode determines the number of channels per stream, the number of streams, and the direction-control operation. Therefore the way in which serial data is addressed in the internal memory space must change with the serial port mode. Because of this, it is necessary to select the serial port mode (with DR1-0 and FDC in the IMS register) before programming the Receive Path Connection Memory.

2.048 Mbps Balanced Mode

The 2.048 Mbps Balanced mode has 8 serial input and 8 serial output streams, and 32 channels per stream. Therefore 3 bits are used to address the 8 streams, and 5 bits are used to address the 32 channels. Figure 11a shows how the Transmit Path Data Memory is read in this mode, by the CPU, or by the Transmit Path Connection Memory. Each of the 256 input channels is mapped to an address in the TPDM. CPU reads require the LSB (Least Significant Bit) of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 8 bits.

Figure 11b shows how the Receive Path Connection Memory is addressed by the CPU. Each of the 256 output channels has a control-address in the RPCM. CPU accesses require the LSB of the CAR Register, and the 7 LSBs of the address bus. When the DC bit for a specific output channel is LOW, that channel is output on the STi pin rather than the STo pin, and the data at the STo pin is input to the TPDM. When the DC bit is HIGH, the output channel appears at the normal STo pin.

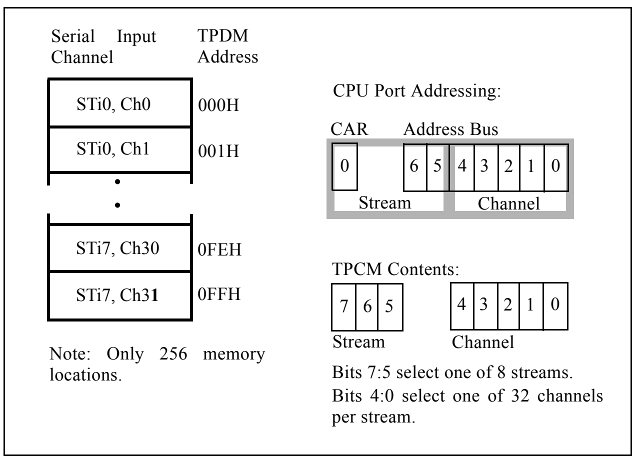

Figure 11a - 2.048 Mbps Balanced Mode TPDM Addressing

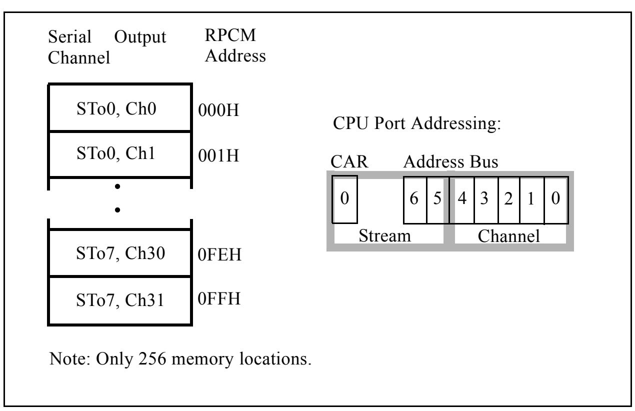

Figure 11b - 2.048 Mbps Balanced Mode RPCM Addressing

2.048 Mbps Add/Drop Mode

The 2.048 Mbps Add/Drop mode has 16 serial input/output streams, and 32 channels per stream. Therefore 4 bits are used to address the 16 streams, and 5 bits are used to address the 32 channels. Figure 12a shows how the Transmit Path Data Memory is read in this mode. Each of the 512 possible input channels is mapped to an address in the TPDM. CPU reads require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 9 bits. In this mode the TPDM reads all 512 serial channels as inputs. When a specific channel is driven by the MT90840 as an output, the output data is also copied back into the TPDM.

Figure 12b shows how the Receive Path Connection Memory is addressed by the CPU in 2.048 Mbps Add/Drop mode. Each of the 512 possible output channels has a control-address in the RPCM. CPU accesses require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. When the DC bit or the OE bit at a specific control-address is LOW, no data is driven out for that channel, and the input data at the pin is written to the TPDM.

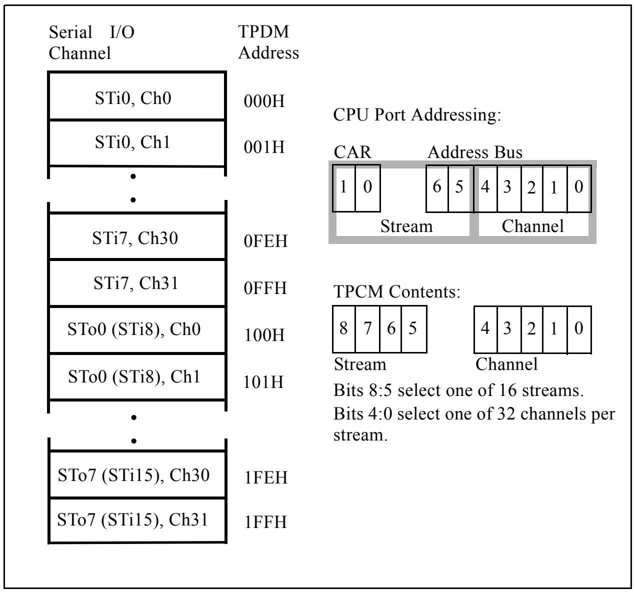

Figure 12a - 2.048 Mbps Add/Drop Mode TPDM Addressing

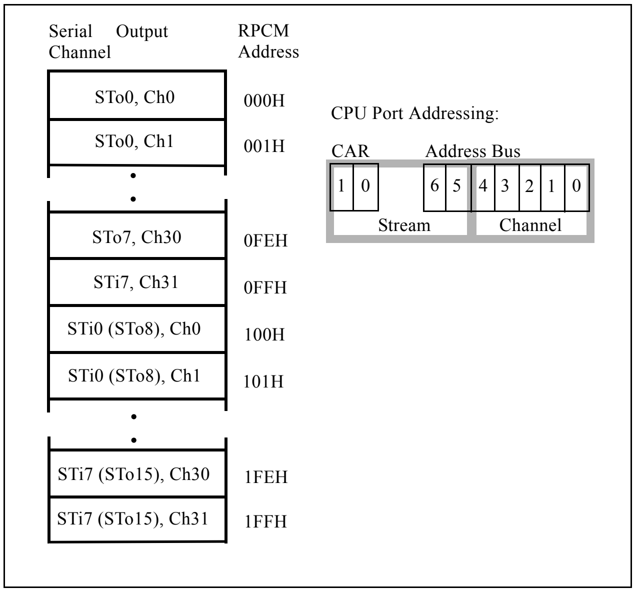

Figure 12b - 2.048 Mbps Add/Drop Mode RPCM Addressing

4.096 Mbps Mode

The 4.096 Mbps mode has 8 input and 8 output streams, and 64 channels per stream. Therefore 3 bits are used to address the 8 streams, and 6 bits are used to address the 64 channels. Figure 13a shows how the Transmit Path Data Memory is read in this mode. Each of the 512 input channels is mapped to an address in the TPDM. CPU reads require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 9 bits.

Figure 13b shows how the Receive Path Connection Memory is addressed by the CPU in 4.096 Mbps mode. Each of the 512 output channels has a control-address in the RPCM. CPU accesses require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. Per-channel direction control in this mode is the same as the 2.048 Mbps Balanced mode.

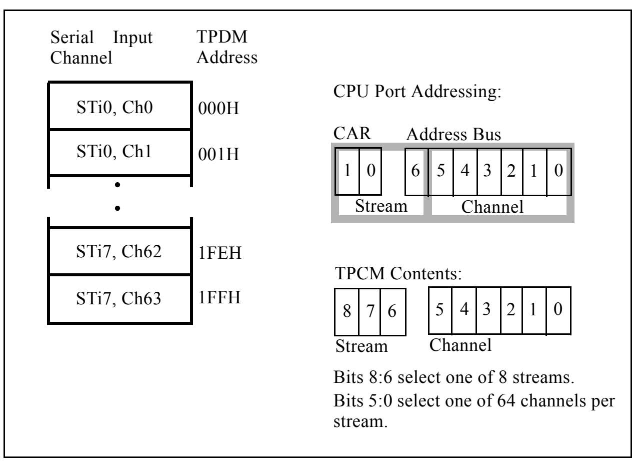

Figure 13a - 4.096 Mbps TPDM Addressing