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ZARLINK SEMICONDUCTOR

MT90863
3 V Rate Conversion Digital Switch

Data Sheet

September 2011

Features

- 2,048 × 512 and 512 x 512 switching among backplane and local streams
- Rate conversion between 2.048, 4.096 and 8.192 Mb/s
- Optional sub-rate switch configuration for 2.048 Mb/s streams
- Per-channel variable or constant throughput delay
- Compatible to HMVIP and H.100 specifications
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel message mode
- Per-channel direction control
- Per-channel high impedance output control
- Non-multiplexed microprocessor interface
- Connection memory block programming
- 3.3 V local I/O with 5 V tolerant inputs and TTL-compatible outputs
- IEEE-1149.1 (JTAG) Test Port

Ordering Information

MT90863AG	144 Pin PBGA	Trays
MT90863AL1	128 Pin MQFP*	Tubes
MT90863AG2	144 Pin PBGA**	Trays, Bake & Drypack

*Pb Free Matte Tin
**Pb Free Tin/Silver/Copper

-40°C to +85°C

Applications

- Medium and large switching platforms
- CTI application
- Voice/data multiplexer
- Support ST-BUS, HMVIP and H.100 interfaces

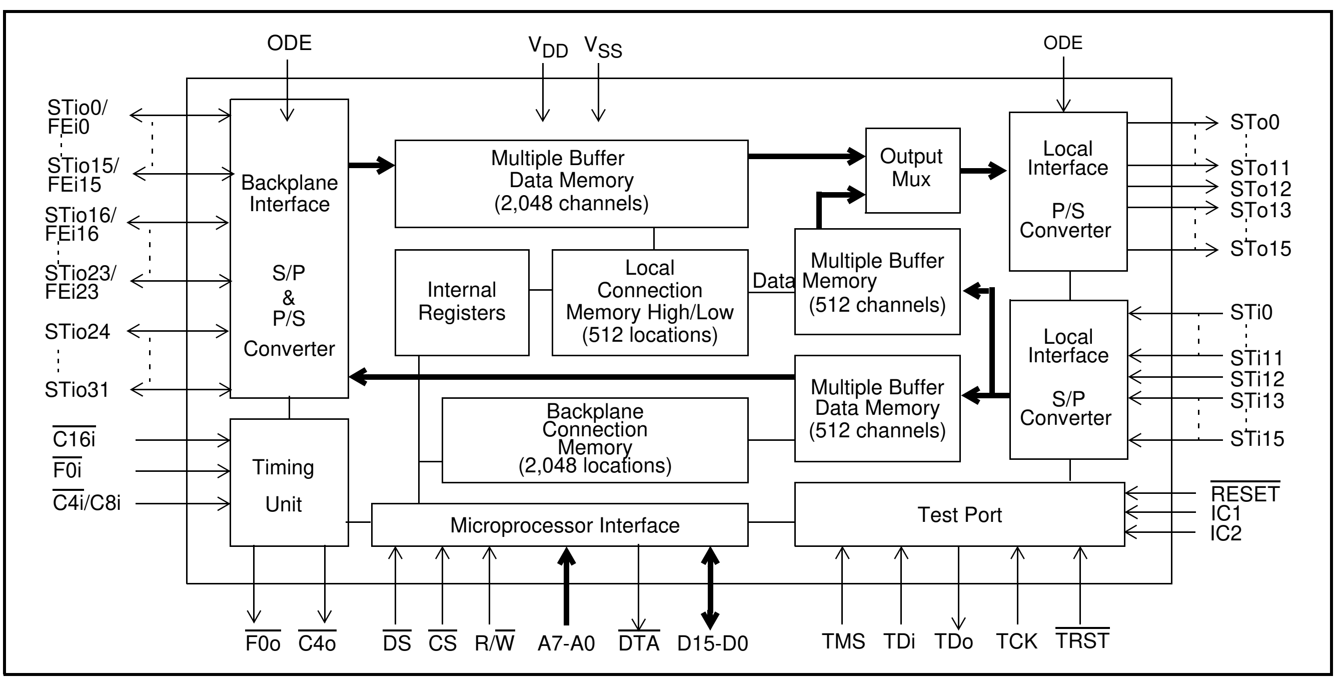

Figure 1 - Functional Block Diagram

Description

The MT90863 Rate Conversion Switch provides switching capacities of 2,048 × 512 channels between backplane and local streams, and 512 x 512 channels for local streams. The connected serial inputs and outputs may have 32, 64 and 128 64 kb/s channels per frame with data rates of 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s respectively.

The MT90863 also offers a sub-rate switching configuration which allows 2-bit wide 16 kb/s data channels to be switched within the device.

The device has features (such as: message mode; input and output offset delay; direction control; and, high impedance output control) that are programmable on per-stream or per-channel basis.

Change Summary

Changes from the May 2006 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

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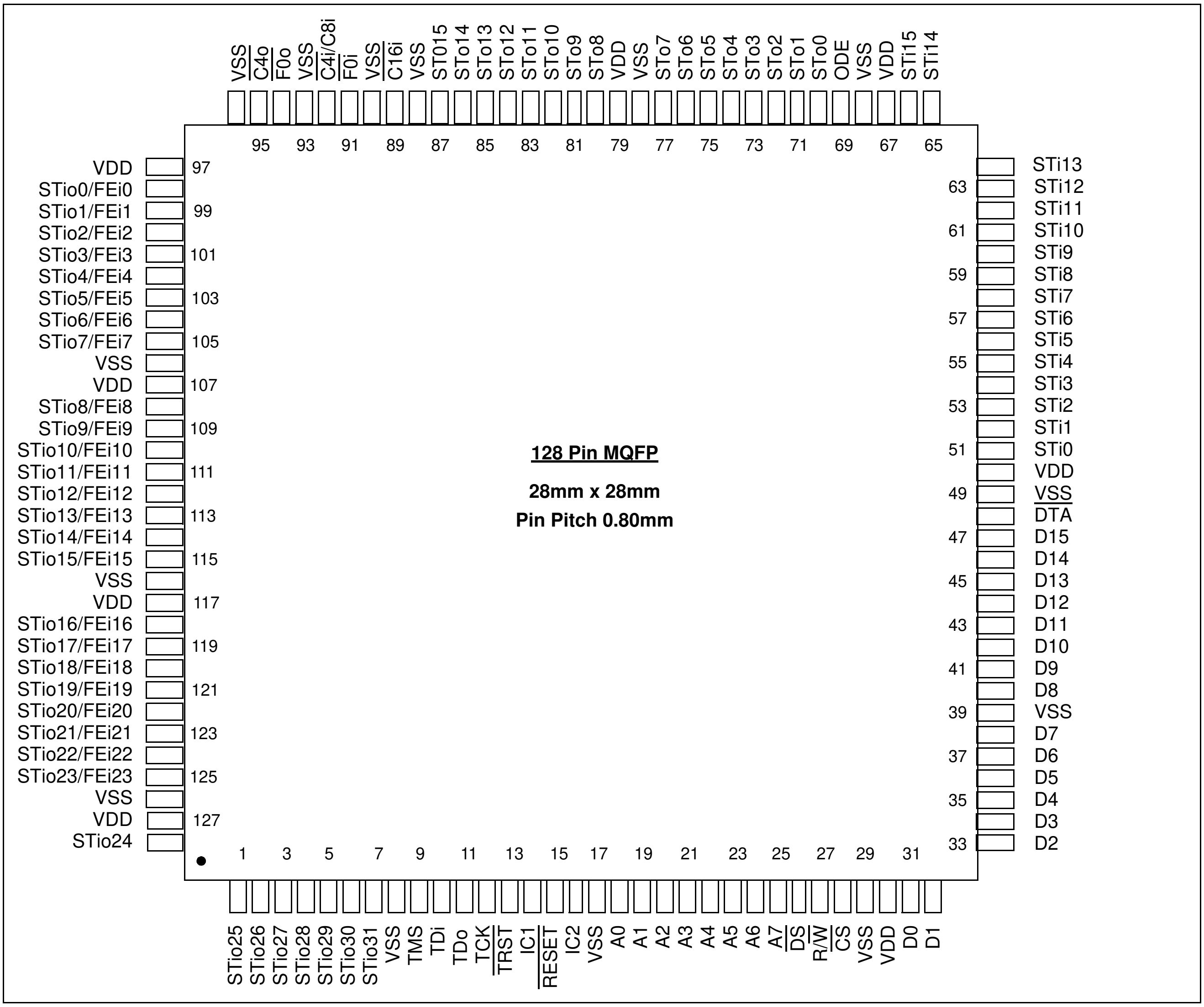

Figure 2 - MQFP Pin Connections

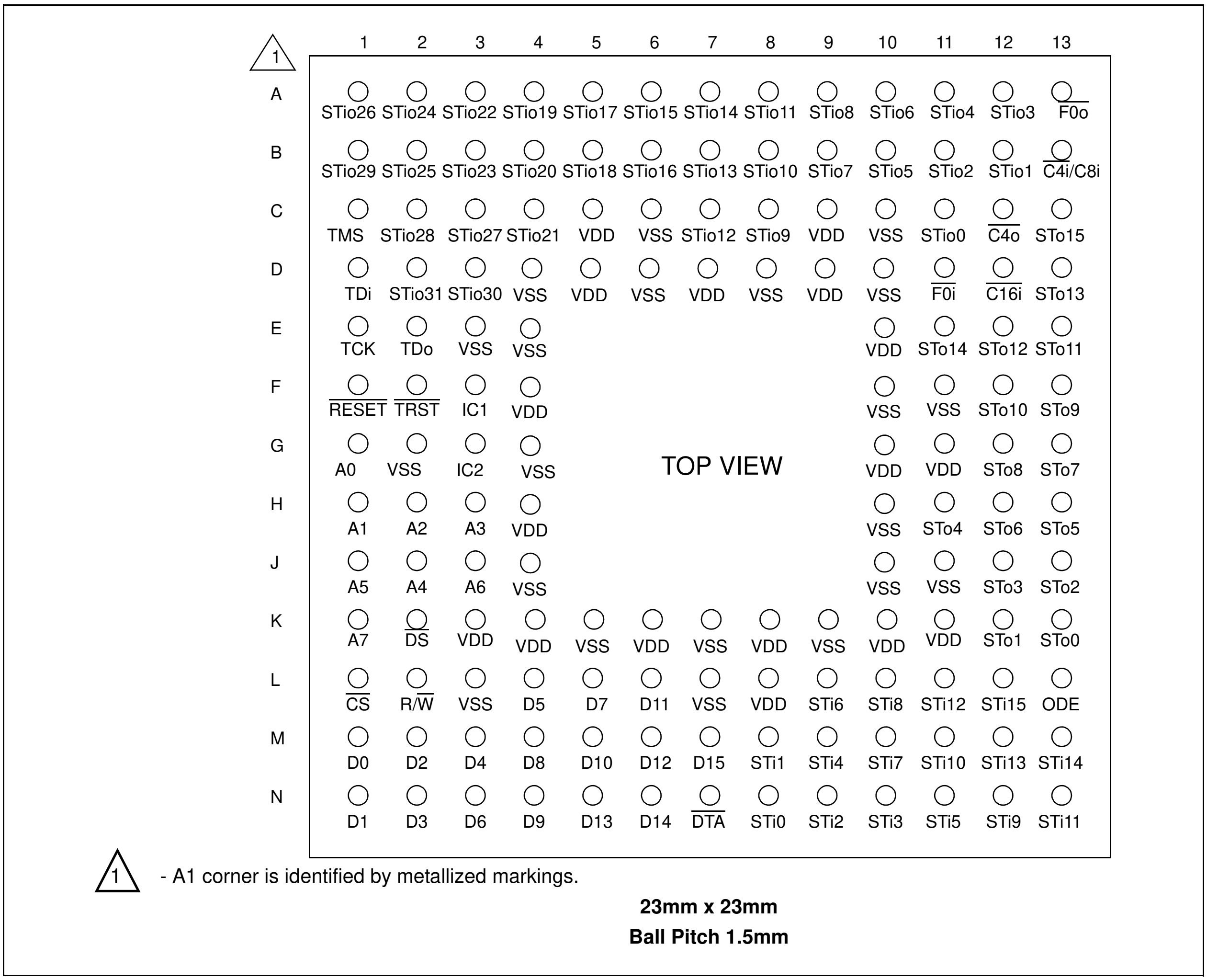

Figure 3 - BGA Pin Connections

Pin Description

128 MQFP Pin#	144 BGA Pin#	Name	Description
30,50,67, 79,97,107, 117,127	C5,C9,D5,D7, D9,E10,F4,G10 ,G11,H4, K3,K4,K6,K8 K10,K11,L8	V_{DD}	**+3.3 Volt Power Supply**
8,17,29,39, 49,68,78,8 8,90,93,96, 106, 116,126	C6,C10,D4,D6, D8,D10,E3,E4, F10,F11,G2, G4,H10,J4, J10,J11,K5 K7,K9,L3,L7	V_{ss}	**Ground**
89	D12	$\overline{\text{C16i}}$	**Master Clock (5 V Tolerant Input):** Serial clock for shifting data in/out on the serial streams. This pin accepts a 16.384 MHz clock.
91	D11	$\overline{\text{F0i}}$	**Master Frame Pulse (5 V Tolerant Input):** In ST-BUS mode, this input accepts a 61 ns wide negative frame pulse. In CT Bus mode, it accepts a 122 ns wide negative frame pulse. In HMVIP mode, it accepts a 244 ns wide negative frame pulse.
92	B13	$\overline{\text{C4i}}$/C8i	**HMVIP/CT Bus Clock (5 V Tolerant Input):** When HMVIP mode is enabled, this pin accepts a 4.096 MHz clock for HMVIP frame pulse alignment. When CT Bus mode is enabled, it accepts a 8.192 MHz clock for CT frame pulse alignment.
94	A13	$\overline{\text{F0o}}$	**Frame Pulse (5 V Tolerant Output):** A 244 ns wide negative frame pulse that is phase locked to the master frame pulse ($\overline{\text{F0i}}$).
95	C12	$\overline{\text{C4o}}$	**C4 Clock (5 V Tolerant Output):** A 4.096 MHz clock that is phase locked to the master clock ($\overline{\text{C16i}}$).
98-105, 108-115	C11, B12, B11, A12, A11, B10, A10, B9, A9, C8, B8, A8, C7, B7, A7, A6,	STio0 - 15 FEi0 - 15	**Serial Input Streams 0 to 15 / Frame Evaluation Inputs 0 to 15 (5 V Tolerant I/O).** In 2 Mb/s and HMVIP modes, these pins accept serial TDM data streams at 2.048 Mb/s with 32 channels per stream. In 4 Mb/s or 8 Mb/s mode, these pins accept serial TDM data streams at 4.096 or 8.192 Mb/s with 64 or 128 channels per stream respectively. In Frame Evaluation Mode (FEM), they are frame evaluation inputs.
118-125	B6, A5, B5, A4, B4, C4, A3, B3	STio16 - 23 FEi16 - 23	**Serial Input Streams 16 to 23 (5 V Tolerant I/O).** In 2 Mb/s or 4 Mb/s mode, these pins accept serial TDM data streams at 2.048 or 4.096 Mb/s with 32 or 64 channels per stream respectively. In HMVIP mode, these pins have a data rate of 8.192 Mb/s with 128 channels per stream. In Frame Evaluation Mode (FEM), they are frame evaluation inputs.
128, 1-7	A2, B2, A1, C3, C2, B1, D3, D2	STio24 - 31	**Serial Input Streams 24 to 31 (5 V Tolerant I/O).** These pins are only used for 2 Mb/s or 4 Mb/s mode. They accept serial TDM data streams at 2.048 or 4.096 Mb/s with 32 or 64 channels per stream respectively.
9	C1	TMS	**Test Mode Select (3.3 V Input with internal pull-up):** JTAG signal that controls the state transitions of the TAP controller.
10	D1	TDi	**Test Serial Data In (3.3 V Input with internal pull-up):** JTAG serial test instructions and data are shifted in on this pin.

Pin Description (continued)

128 MQFP Pin#	144 BGA Pin#	Name	Description
11	E2	TDo	**Test Serial Data Out (3.3 V Output):** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG scan is not enabled.
12	E1	TCK	**Test Clock (5 V Tolerant Input):** Provides the clock to the JTAG test logic.
13	F2	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with internal pull-up):** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up, or held low continuously, to ensure that the MT90863 is in the normal operation mode.
14	F3	IC1	**Internal Connection 1 (3.3 V Input with internal pull-down):** Connect to V_{SS} for normal operation.
15	F1	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input):** This input (active LOW) puts the MT90863 in its reset state. This clears the device's internal counters and registers.
16	G3	IC2	**Internal Connection 2 (3.3 V Input):** Connect to V_{SS} for normal operation.
18-25	G1, H1, H2, H3, J2, J1,J3, K1	A0 - A7	**Address 0 - 7 (5 V Tolerant Input):** These lines provide the A0 to A7 address lines to the internal memories.
26	K2	$\overline{\text{DS}}$	**Data Strobe (5 V Tolerant Input):** This active low input works in conjunction with $\overline{\text{CS}}$ to enable the read and write operations.
27	L2	R/$\overline{\text{W}}$	**Read/Write (5 V Tolerant Input):** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
28	L1	$\overline{\text{CS}}$	**Chip Select (5 V Tolerant Input):** Active low input used by a microprocessor to activate the microprocessor port.
31-38, 40-47	M1, N1, M2, N2, M3, L4, N3, L5, M4, N4, M5, L6, M6, N5, N6, M7,	D0 - 7, D8 - D15	**Data Bus 0 -15 (5 V Tolerant I/O):** These pins form the 16-bit data bus of the microprocessor port.
48	N7	$\overline{\text{DTA}}$	**Data Transfer Acknowledgment (5 V Tolerant Three-state Output):** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level when the pin is tri-stated.
51-54	N8, M8, N9, N10	STi0 - 3	**Serial Input Streams 0 to 3 (5 V Tolerant Inputs):** In 2 Mb/s or Subrate Switching mode, these inputs accept data rates of 2.048 Mb/s with 32 channels per stream. In 8 Mb/s mode, these inputs accept data rates of 8.192 Mb/s with 128 channels per stream.
55-62	M9, N11, L9, M10, L10, N12, M11, N13	STi4 - 11	**Serial Input Streams 4 to 11 (5 V Tolerant Inputs):** In 2 Mb/s or Subrate Switching mode, these inputs accept data rates of 2.048 Mb/s with 32 channels per stream.

Pin Description (continued)

128 MQFP Pin#	144 BGA Pin#	Name	Description
63	L11	STi12	**Serial Input Streams 12 (5 V Tolerant Input):** In 2 Mb/s mode, this input accepts data rate of 2.048 Mb/s with 32 channels per stream respectively. In Sub-rate Switching mode, this pin accepts 2.048 Mb/s with 128 channels per stream for Sub-rate switching application.
64-66	M12, M13, L12	STi13 - 15	**Serial Input Streams 13 to 15 (5 V Tolerant Inputs):** In 2 Mb/s mode, these inputs accept a data rate of 2.048 Mb/s with 32 channels per stream.
69	L13	ODE	**Output Drive Enable (5 V Tolerant Input):** This is the output enable control for the STo0 to STo15 serial outputs and STio0 to STio31 serial bidirectional outputs.
70-73	K13, K12, J13, J12	STo0 - 3	**Serial Output Streams 0 to 3 (5 V Tolerant Three-state Outputs):** In 2 Mb/s or Sub-rate Switching mode, these outputs have data rates of 2.048 Mb/s with 32 channels per stream respectively. In 8 Mb/s mode, these outputs have data rates of 8.192 Mb/s with 128 channels per stream
74-77, 80-83	H11, H13, H12, G13, G12, F13, F12, E13	STo4 - 7, STo8 - 11	**Serial Output Streams 4 to 11 (5 V Tolerant Three-state Outputs):** In 2 Mb/s or Sub-rate Switching mode, these outputs have data rates of 2.048 Mb/s with 32 channels per stream
84	E12	STo12	**Serial Output Streams 12 (5 V Tolerant Three-state Output):** In 2 Mb/s mode, this output has data rate of 2.048 Mb/s with 32 channels per stream. In Sub-rate Switching mode, this pin has data rate of 2.048 Mb/s with 128 channels per stream for Sub-rate switching application.
85-87	D13, E11, C13	STo13 - 15	**Serial Output Streams 13 to 15 (5 V Tolerant Three-state Outputs):** In 2 Mb/s mode, these outputs have a data rate of 2.048 Mb/s with 32 channels per stream.

1.0 Device Overview

The Rate conversion Switch (MT90863) can switch up to 2,048 $\times$ 512 channels while also providing a rate conversion capability. It is designed to switch 64 kb/s PCM or N X 64 kb/s data between the backplane and local interfaces. When the device is in the sub-rate switching mode, 2-bit wide 16 kb/s data channels can be switched within the device. The device maintains frame integrity in data applications and minimum throughput delay for voice application on a per channel basis.

The backplane interface can operate at 2.048, 4.096 or 8.192 Mb/s, arranged in 125 μs wide frames that contain 32, 64 or 128 channels, respectively. A built-in rate conversion circuit allows users to interface between backplane interface and the local interface which operates at 2.048 Mb/s or 8.192 Mb/s.

By using Zarlink's message mode capability, the microprocessor can access input and output time-slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS devices.

The frame offset calibration function allows users to measure the frame offset delay for streams STio0 to STio23. The offset calibration is activated by a frame evaluation bit in the frame evaluation register. The evaluation result is stored in the frame evaluation registers and can be used to program the input offset delay for individual streams using internal frame input offset registers.

2.0 Functional Description

A functional Block Diagram of the MT90863 is shown in Figure 1. One end of the MT90863 is used to interface with backplane applications, such as HMVIP or H.100 environments, while the other end supports the local switching environments.

2.1 Frame Alignment Timing

The Device Mode Selection (DMS) register allows users to select three different frame alignment timing modes. In ST-BUS modes, the master clock ($\overline{C16i}$) is always at 16.384 MHz. The frame pulse ($\overline{F0i}$) input accepts a negative frame pulse at 8 kHz. The frame pulse goes low at the frame boundary for 61 ns. The frame pulse output $\overline{F0o}$ provides a 244 ns wide negative frame pulse and the $\overline{C4o}$ output provides a 4.094 MHz clock. These two signals are used to support local switching applications. See Figure 4 for the ST-BUS timings.

In CT Bus mode, the $\overline{C4i}$/C8i pin accepts 8.192 MHz clock for the CT Bus frame pulse alignment. The $\overline{F0i}$ is the CT bus frame pulse input. The CT frame pulse goes low at the frame boundary for 122 ns. See Figure 5 for the CT Bus timing.

In HMVIP mode, the $\overline{C4i}$/C8i pin accepts 4.096 MHz clock for the HMVIP frame pulse alignment. The $\overline{F0i}$ is the HMVIP frame pulse input. The HMVIP frame pulse goes low at the frame boundary for 244 ns. See Figure 6 for the HMVIP timing.

Table 1 - describes the input timing requirements for ST-BUS, CT Bus and HMVIP modes.

3.0 Switching Configuration

The device has four operation modes for the backplane interface and three operation modes for the local interface. These modes can be programmed via the Device Mode Selection (DMS) register. Mode selections between the backplane and local interfaces are independent. See Table 2 and Table 3 for the selection of various operation modes via the programming of the DMS register.

3.1 Backplane Interface

The backplane interface can be programmed to accept data streams of 2 Mb/s, 4 Mb/s or 8 Mb/s. When 2 Mb/s mode is enabled, STio0 to STio31 have a data rate of 2.048 Mb/s. When 4 Mb/s mode is enabled, STio0 to STio31 have a data rate of 4.096 Mb/s. When 8 Mb/s mode is enabled, STio0 to STio15 have a data rate of 8.192 Mb/s. When HMVIP mode is enabled, STio0 to STio15 have a data rate of 2.048 Mb/s and STio16 to STio23 have a data rate of 8.192 Mb/s. Table 2 describes the data rates and mode selection for the backplane interface.

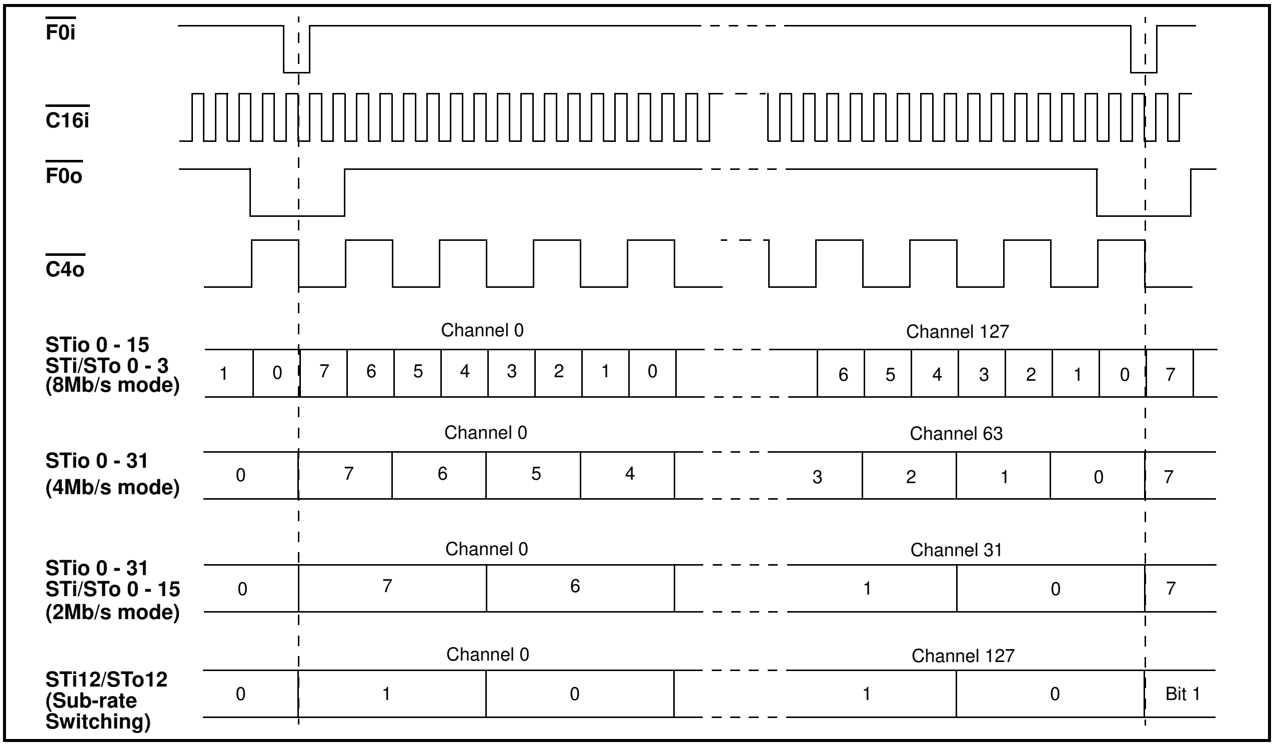

Figure 4 - ST-BUS Timing for 2, 4 and 8 Mb/s Data Streams

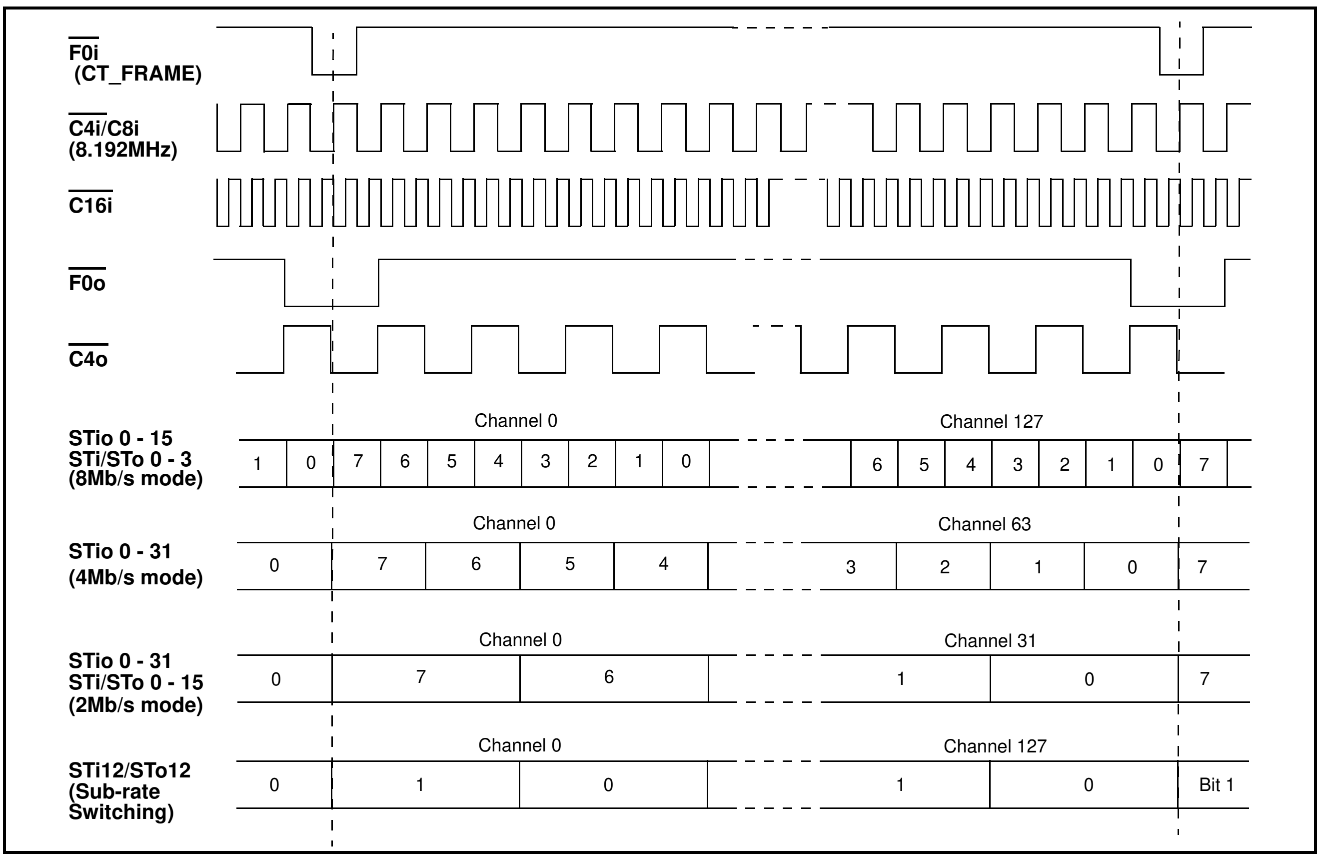

Figure 5 - CT Bus Mode Timing for 2, 4 and 8 Mb/s Data Streams

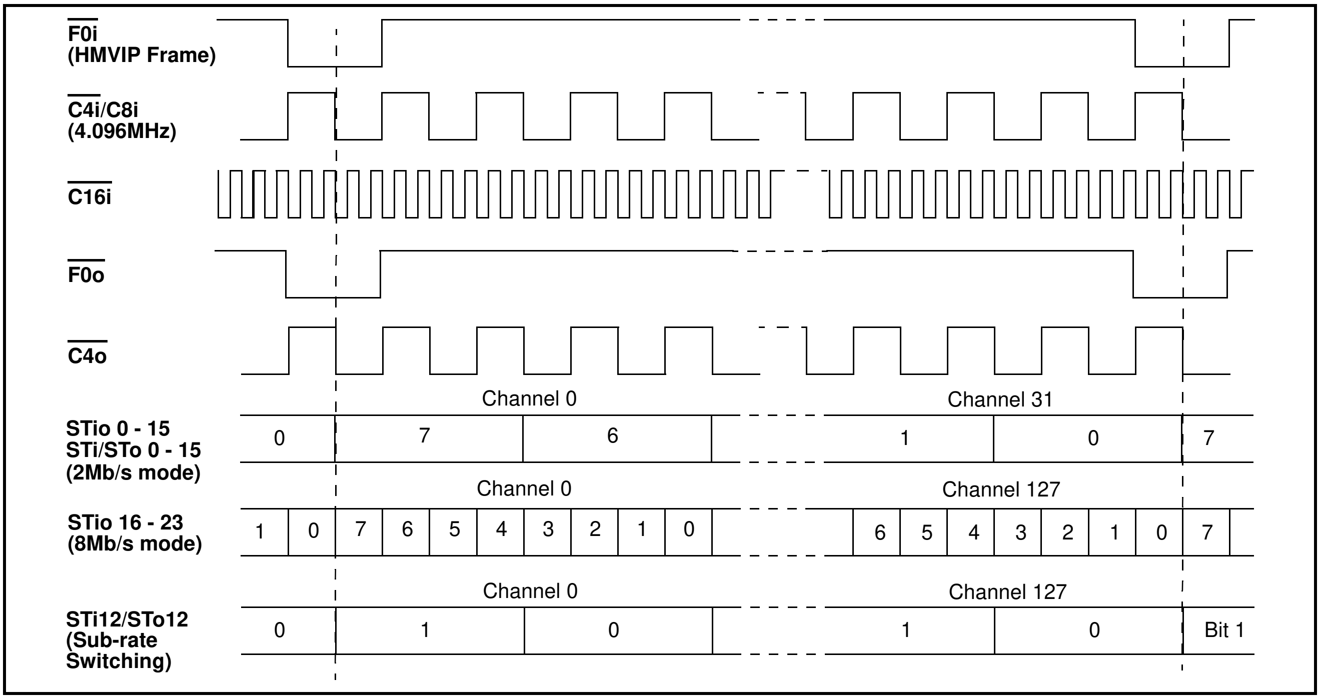

Figure 6 - HMVIP Mode Timing for 2 and 8 Mb/s Data Streams

3.2 Local Interface

Three operation modes, 2 Mb/s, 8 Mb/s and Sub-rate Switching mode, can be selected for the local interface. When 2 Mb/s mode is selected, STi0 to STi15 and STo0 to STo15 have a 2.048 Mb/s data rate. When 8 Mb/s mode is selected, STi0 to STi3 and STo0 to STo3 have an 8.192 Mb/s data rate. When Sub-rate Switching mode is selected, STi0 to STi11 and STo0 to STo11 have 2.048 Mb/s data with 64 kb/s data channels and STi12 and STo12 have a 2.048 Mb/s data rate with 16 kb/s data channels. Table 3 describes the data rates and mode selection for the local interface.

3.3 Input Frame Offset Selection

Input frame offset selection allows the channel alignment of individual backplane input streams, that operate at 8.192 Mb/s (STio0-23), to be shifted against the input frame pulse (F0i). This feature compensates for the variable path delays caused by serial backplanes of variable length. Such delays can be occur in large centralized and distributed switching systems.

Each backplane input stream can have its own delay offset value by programming the input delay offset registers (DOS0 to DOS5). Possible adjustment can range up to +4 master clock (C16i) periods forward with resolution of half master clock period. See Table 10 and Table 11, and Figure 9,Figure 9 - for frame input delay offset programming.

3.4 Output Advance Offset Selection

The MT90863 allows users to advance individual backplane output streams which operate at 8.192 Mb/s (STio0-23) by half a master clock (C16i) cycle. This feature is useful in compensating for variable output delays caused by various output loading conditions. The frame output offset registers (FOR0 & FOR1) control the output offset delays for each backplane output stream via the OFn bit programming. Table 12 and Figure 10 detail frame output offset programming.

3.5 Serial Input Frame Alignment Evaluation

The MT90863 provides the frame evaluation inputs, FEi0 to FEi23, to determine different data input delays with respect to the frame pulse $\overline{F0i}$. By using the frame evaluation input select bits (FE0 to FE4) of the frame alignment register (FAR), users can select one of the twenty-four frame evaluation inputs for the frame alignment measurement.

A measurement cycle is started by setting the start frame evaluation (SFE) bit low for at least one frame. Then the evaluation starts when the SFE bit in the Internal Mode Selection (IMS) register is changed from low to high. One frame later, the complete frame evaluation (CFE) bit of the frame alignment register changes from low to high to signal that a valid offset measurement is ready to be read from bits 0 to 9 of the FAR register. The SFE bit must be set to zero before a new measurement cycle is started.

Timing Signals	ST-BUS Mode	CT Bus Mode	HMVIP Mode
F0i Width	61 ns	122 ns	244 ns
$\overline{C4i}$/C8i	Not Required	8.192 MHz	4.096 MHz
C16i	16.384 MHz		
F0o Width	244 ns		
C4o	4.096 MHz		

Table 1 - Timing Signals Requirements for Various Operation Modes

DMS Register Bits			Modes		Backplane Interface	Data Rate
BMS2	BMS1	BMS0				
0	0	0	2 Mb/s, ST-BUS Mode		STio0 - 31	2.048 Mb/s
0	0	1	2 Mb/s, CT Bus Mode		STio0 - 31	2.048 Mb/s
0	1	0	4 Mb/s, ST-BUS Mode		STio0 - 31	4.096 Mb/s
0	1	1	4 Mb/s, CT Bus Mode		STio0 - 31	4.096 Mb/s
1	0	0	8 Mb/s, ST-BUS Mode		STio0 - 15	8.192 Mb/s
					STio16 - 31	Not available
1	0	1	8 Mb/s, CT Bus Mode		STio0 - 15	8.192 Mb/s
					STio16 - 31	Not available
1	1	0	HMVIP Mode		STio0 - 15	2.048 Mb/s
					STio16 - 23	8.192 Mb/s
					STio24 - 31	Not available

Table 2 - Mode Selection for Backplane interface

DMS Register Bits		Modes		Local Interface		Data Rate
LMS1	LMS0					
0	0	2 Mb/s Mode		STi0 - 15		2.048 Mb/s
				STo0 - 15		2.048 Mb/s
0	1	Sub-Rate Switching Mode		STi0 - 11		2.048 Mb/s
				STi12		Sub-rate Switching Input Stream at 2.048 Mb/s
				STi13 - 15		Not available
				STo0 - 11		2.048 Mb/s
				STo12		Sub-rate Switching Output Stream at 2.048 Mb/s
				STo13 - 15		Not available
1	0	8 Mb/s Mode		STi0 - 3		8.192 Mb/s
				STi4 - 15		Not available
				STo0 - 3		8.192 Mb/s
				STo4 - 15		Not available

Table 3 - Mode Selection for Local Interface

The falling edge of the frame measurement signal (FEi) is evaluated against the falling edge of the frame pulse ($\overline{F0i}$). Table 8 and Figure 8 describe the frame alignment register.

3.6 Memory Block Programming

The MT90863 has two connection memories: the backplane connection memory and the local connection memory. The local connection memory is partitioned into high and low parts. The IMS register provides users with the capability of initializing the local connection memory low and the backplane connection memory in two frames. Bit 11 to bit 13 of every backplane connection memory location will be programmed with the pattern stored in bit 7 to bit 9 of the IMS register. Bit 12 to 15 of every local connection memory low location will be programmed with the pattern stored in bits 3 to 6 of the IMS register.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register high. When the block programming enable (BPE) bit of the IMS register is set to high, the block programming data will be loaded into bits 11 to 13 of every backplane connection memory and bits 12 to 15 of every local connection memory low. The other connection memory bits are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero. See Figure 7 for the connection memory contents when the device is in block programming mode.

4.0 Delay through the MT90863

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the L$\overline{V}$/C and B$\overline{V}$/C bits of the local and backplane connection memory as described in Table 16 and Table 19.

4.1 Variable Delay Mode (L$\overline{V}$/C or B$\overline{V}$/C bit = 0)

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams.

4.2 Constant Delay Mode (L$\overline{V}$/C bit or B$\overline{V}$/C= 1)

In this mode a multiple data memory buffer is used to maintain frame integrity in all switching configurations.

5.0 Microprocessor Interface

The MT90863 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed buses. The required microprocessor signals are the 16-bit data bus (D0-D15), 8-bit address bus (A0-A7) and 4 control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 16 - Figure 16 for Motorola non-multiplexed bus timing.

The MT90863 microprocessor port provides access to the internal registers, connection and data memories. All locations provide read/write access except for the Data Memory and the Data Read Register which are read only.

5.1 Memory Mapping

The address bus on the microprocessor interface selects the internal registers and memories of the MT90863. If the A7 address input is low, then the registers are addressed by A6 to A0 as shown in Table 4.

If the A7 is high, the remaining address input lines are used to select the serial input or output data streams corresponding to the subsection of memory positions. For data memory reads, the serial inputs are selected. For connection memory writes, the serial outputs are selected.

The control, device mode selection and internal mode selection registers control all the major functions of the device. The device mode selection register and internal mode selection register should be programmed immediately after system power-up to establish the desired switching configuration as explained in the Frame Alignment Timing and Switching Configurations sections.

The control register is used to control the switching operations in the MT90863. It selects the internal memory locations that specify the input and output channels selected for switching.

Control register data consists of: the memory block programming bit (MBP): the memory select bits (MS0-2); and, the stream address bits (STA0-4). The memory block programming bit allows users to program the entire connection memory block, (see Memory Block Programming section). The memory select bits control the selection of the connection memory or the data memory. The stream address bits define an internal memory subsections corresponding to serial input or serial output streams.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	BBPD 2	BBPD 1	BBPD 0	0	0	0	0	0	0	0	0	0	0	0

Backplane Connection Memory (BCM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBPD 3	LBPD 2	LBPD 1	LBPD 0	0	0	0	0	0	0	0	0	0	0	0	0

Local Connection Memory Low (LCML)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Local Connection Memory High (LCMH)

Figure 7 - Block Programming Data in the Connection Memories

A7 (Note 1)	A6	A5	A4	A3	A2	A1	A0	Location
0	0	0	0	0	0	0	0	Control Register, CR
0	0	0	0	0	0	0	1	Device Mode Selection Register, DMS
0	0	0	0	0	0	1	0	Internal Mode Selection Register, IMS
0	0	0	0	0	0	1	1	Frame Alignment Register, FAR
0	0	0	0	0	1	0	0	Input Offset Selection Register 0, DOS0
0	0	0	0	0	1	0	1	Input Offset Selection Register 1, DOS1
0	0	0	0	0	1	1	0	Input Offset Selection Register 2, DOS2
0	0	0	0	0	1	1	1	Input Offset Selection Register 3, DOS3
0	0	0	0	1	0	0	0	Input Offset Selection Register 4, DOS4
0	0	0	0	1	0	0	1	Input Offset Selection Register 5, DOS5
0	0	0	0	1	0	1	0	Frame Output Offset Register, FOR0
0	0	0	0	1	0	1	1	Frame Output Offset Register, FOR1
0	0	0	0	1	1	0	0	Address Buffer Register, ABR
0	0	0	0	1	1	0	1	Data Write Register, DWR
0	0	0	0	1	1	1	0	Data Read Register, DRR
1 1 1 1 1	0 0 0 0 0	0 0 0 0 0	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 0 . 1 1	0 1 . 0 1	Ch 0 Ch 1 . Ch 30 Ch 31 (Note 2)

Table 4 - Address Memory Map

A7 (Note 1)	A6	A5	A4	A3	A2	A1	A0	Location
1	0	1	0	0	0	0	0	Ch 32
1	0	1	0	0	0	0	1	Ch 33
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	0	Ch 126
1	1	1	1	1	1	1	1	Ch 127 (Note 3)

Notes:
1. Bit A7 must be high for access to data and connection memory positions. Bit A7 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2 Mb/s.
3. Channels 0 to 127 are used when serial stream is at 8 Mb/s

Table 4 - Address Memory Map (continued)

The data in the DMS register consists of the local and backplane mode selection bits (LMS0-1 and BMS0-2) to enable various switching modes for local and backplane interfaces respectively.

The data in the IMS register consists of block programming bits (LBPD0-3 and BBPD0-2), block programming enable bit (BPE), output standby bit (OSB) and start frame evaluation bit (SFE). The block programming enable bit allows users to program the entire backplane and local connection memories, (see Memory Block Programming section). If the ODE pin is low, the OSB bit enables (if high) or disables (if low) all ST-BUS output drivers. If the ODE pin is high, the contents of the OSB bit is ignored and all ST-BUS output drivers are enabled.

See Table 5 for the output high impedance control.

5.2 Address Buffer Mode

The implementation of the address buffer, data read and data write registers allows faster memory read/write operation for the microprocessor port. See Table 6 and following for bit assignments.

The address buffer mode is controlled by the AB bit in the control register. The targeted memory for data read/write is selected by the MS0-2 bits in the control register.

The data write register (DWR) contains the data to be transferred to the memory. The data read register (DRR) contains the data transferred from the memory.

The address buffer register (ABR) allow users to specify the read or write address by programming the stream address bits (SA0-4) and the channel address bits (CA0-6). Data transfer from/to the memory is controlled by the read/write select bits (RS, WS). The complete data access (CDA) bit indicates the completion of data transfer between the memory and DWR or DRR register.

5.3 Write Operation using Address Buffer Mode

Enable the address buffer mode by setting the AB bit from low to high. Program the DWR register with data to be transferred to memory. Load the ABR register with proper channel and stream information. Change the WS bit in the ABR register from low to high to initiate the data transfer from the DWR register to the memory. After several master clock cycles, the CDA bit in the ABR register changes from low to high to signal the completion of data transfer and resets the WS bit to low. Repeat the above steps for subsequent memory write operations. Disable the address buffer write operation by setting the AB bit to low.

5.4 Read Operation using Address Buffer Mode

Enable the address buffer mode by setting the AB bit from low to high. Program the ABR register with proper channel and stream information. Change the RS bit in the ABR register from low to high to initiate the data transfer from the memory to the DRR register. After several master clock cycles, the CDA bit in the ABR register changes from low to high to signal the completion of data transfer and resets the RS bit to low. Read the DRR register to obtain the data transferred from the memory. Repeat the above steps for subsequent memory read operations. Disable the address buffer read operation by setting the AB bit to low.

5.5 Backplane Connection Memory Control

The backplane connection memory controls the switching configuration of the backplane interface. Locations in the backplane connection memory are associated with particular STio output streams.

The B$\overline{V}$/C (Variable/Constant Delay) bit of each backplane connection memory location allows the per-channel selection between variable and constant throughput delay modes for all STio channels.

In message mode, the message channel (BMC) bit of the backplane connection memory enables (if high) an associated STio output channel. If the BMC bit is low, the contents of the backplane connection memory stream address bit (BSAB) and channel address bit (BCAB) defines the source information (stream and channel) of the time-slot that will be switched to the STio streams. When message mode is enabled, only the lower half (8 least significant bits) of the backplane connection memory is transferred to the STio pins.

ODE pin	OSB bit in IMS register	DC bit in Backplane CM	STio0-31 Output Driver Status	OE bit in Local CM	STo0-15 Output Driver Status
Don't Care	Don't Care	0	Per Channel High Impedance	0	Per Channel High Impedance
0	0	Don't care	High Impedance	Don't care	High Impedance
0	1	1	Enable	1	Enable
1	Don't care	1	Enable	1	Enable

Table 5 - Output High Impedance Control

Read/Write Address: 00_H, Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	AB	CT	MBP	MS2	MS1	MS0	STA4	STA3	STA2	STA1	STA0

Bit	Name	Description
15-11	Unused	Must be zero for normal operation.
10	AB	**Address Buffer.** When 1, enables the address buffer, data write and data read registers for accessing various memory locations for fast microport access. When 0, disables the address buffer, data write and data read registers.
9	CT	**Channel Tri-state.** When 1, the last bit of each output channel is tri-stated for -22 ns against the channel boundary. When 0, the last bit of each channel is not tri-stated.
8	MBP	**Memory Block Program.** When 1, the connection memory block programming feature is ready for the programming of bit 11 to 13 for backplane connection memory, bit 12 to 15 for local connection memory low. When 0, this feature is disabled.

Table 6 - Control (CR) Register Bits

Read/Write Address: 00_H, Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	AB	CT	MBP	MS2	MS1	MS0	STA4	STA3	STA2	STA1	STA0

Bit	Name	Description
7 - 5	MS2-0	**Memory Select Bits.** These three bits are used to select connection and data memory functions as follows: MS2-0 Memory Selection 000 Local Connection Memory Low Read/Write, 001 Local Connection Memory High Read/Write, 010 Backplane Connection Memory Read/Write, 011 Local Data Memory Read, 100 Backplane Data Memory Read,
4 - 0	STA4-0	**Stream Address Bits**. The binary value expressed by these bits refers to the input or output data stream, which corresponds to the subsection of memory made accessible for subsequent operations. (STA4 = MSB, STA0 = LSB)

Table 6 - Control (CR) Register Bits

Read/Write Address: 01_H, Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	LMS1	LMS0	BMS2	BMS1	BMS0

Bit	Name	Description
15 - 5	unused	Reserved
4 - 3	LMS	**Local Mode Selection Bit.** The binary value expressed by these bits refers to the following backplane interface switching modes: LMS1-0 Local Switching Mode 00 2 Mb/s ST-BUS Mode 01 2 Mb/s Sub-rate Switching Mode 10 8 Mb/s ST-Bus Mode
2 - 0	BMS2-0	**Backplane Mode Selection Bits**. The binary value expressed by these bits refers to the following backplane interface switching modes: BMS2-0 Backplane Switching Mode 000 2 Mb/s ST-BUS Mode 001 2 Mb/s CT Bus Mode 010 4 Mb/s ST-BUS Mode 011 4 Mb/s CT Bus Mode 100 8 Mb/s ST-BUS Mode 101 8 Mb/s CT Bus Mode 110 HMVIP Mode
Note: Please refer to Table 1 for Timing Signal Requirements		

Table 7 - Device Mode Selection (DMS) Register Bits

5.6 Local Connection Memory Control

The local connection memory controls the local interface switching configuration. Local connection memory is split into high and low parts. Locations in local connection memory are associated with particular STo output streams.

The L/B (Local/Backplane Select) bit of each local connection memory location allows per-channel selection of source streams from local or backplane interface.

The L$\overline{\text{V}}$/C (Variable/Constant Delay) bit of each local connection memory location allows the per-channel selection between variable and constant throughput delay modes for all STo channels.

In message mode, the local connection memory message channel (LMC) bit enables (if high) an associated STo output channel. If the LMC bit is low, the contents of the stream address bit (LSAB) and the channel address bit (LCAB) of the local connection memory defines the source information (stream and channel) of the time-slot that will be switched to the STo streams. When message mode is enabled, only the lower half (8 least significant bits) of the local connection memory low bits are transferred to the STo pins.

When sub-rate switching is enabled, the LSR0-1 bits in the local connection memory high define which bit position contains the sub-rate data.

5.7 $\overline{\text{DTA}}$ Data Transfer Acknowledgment Pin

The $\overline{\text{DTA}}$ pin is driven LOW by internal logic to indicate (to the CPU) that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then switches to the high-impedance state. If a short or signal contention prevents the $\overline{\text{DTA}}$ pin from reaching a valid logic HIGH, it will continue to drive for approximately 15nsec before switching to the high-impedance state.

6.0 Initialization of the MT90863

During power up, the $\overline{\text{TRST}}$ pin should be pulsed low, or held low continuously, to ensure that the MT90863 is in the normal operation mode. A 5 KΩ pull-down resistor can be connected to this pin so that the device will not enter the JTAG test mode during power up.

After power up, the contents of the connection memory can be in any state. The ODE pin should be held low after power up to keep all serial outputs in a high impedance state until the microprocessor has initialized the switching matrix. This procedure prevents two serial outputs from driving the same stream simultaneously.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the switch. The memory block programming feature can also be used to quickly initialize the DC and OE bit in the backplane and local connection memory respectively.

When this process is complete, the microprocessor controlling the matrices can either bring the ODE pin high or enable the OSB bit in IMS register to relinquish the high impedance state control.

Read/Write Address: 02_H,
Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	BBPD 2	BBPD 1	BBPD 0	LBPD 3	LBPD 2	LBPD 1	LBPD 0	BPE	OSB	SFE

Bit	Name	Description
15-10	Unused	Must be zero for normal operation.
9-7	BBPD2-0	**Backplane Block Programming Data.** These bits carry the value to be loaded into the backplane connection memory block when the Memory Block Programming feature is active. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of bits BBPD2-0 are loaded into the bit 13 to bit 11 position of the backplane connection memory. Bit 15, bit 14 and bit 10 to bit 0 of the backplane connection memory are zeroed.
6-3	LBPD3-0	**Local Block Programming Data.** These bits carry the value to be loaded into the local connection memory block when the Memory Block Programming feature is active. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of bits LBPD3-0 are loaded into the bit 15 to bit 12 position of the local connection memory. Bit 11 to bit 0 of the local connection memory low are zeroed. Bit 15 to bit 0 of local connection memory high are zeroed.
2	BPE	**Begin Block Programming Enable.** A zero to one transition of this bit enables the memory block programming function. The BPE, BBPD2-0 and LBPD3-0 bits in the IMS register must be defined in the same write operation. Once the BPE bit is set high, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE = 1, the BPE or MBP can be set to 0 to abort the programming operation. When BPE = 1, the other bits in the IMS register must not be changed for two frames to ensure proper operation.
1	OSB	**Output Stand By.** This bit controls the device output drivers. OSB bit / ODE pin / OE bit / STio0 - 31, STo0 - 15 0 / 0 / 1 / High impedance state 1 / 0 / 1 / Enable X / 1 / 1 / Enable X / X / 0 / Per-channel high impedance
0	SFE	**Start Frame Evaluation.** A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. Set this bit to zero for at least one frame (125 µs) to start another frame evaluation.

Table 8 - Internal Mode Selection (IMS) Register Bits

Read/Write Address: 03_H,
Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE4	FE3	FE2	FE1	FE0	CFE	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Bit	Name	Description
15-11	FE4-0	**Frame Evaluation Input Select.** The binary value expressed in these bits refers to the frame evaluation inputs, FEi0 to FEi23.
10	CFE	**Complete Frame Evaluation.** When CFE = 1, the frame evaluation is completed and bits FD9 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the IMS register is changed from 1 to 0. This bit is read-only.
9	FD9	**Frame Delay Bit 11.** The falling edge of FE is sampled during the CLK-high phase (FD9 = 1) or during the CLK-low phase (FD9 = 0). This bit allows the measurement resolution to 1/2 CLK cycle. This bit is read-only.
8-0	FD8-0	**Frame Delay Bits.** The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the SFE bit of the IMS register changes from 1 to 0. (FD8 = MSB, FD0 = LSB). These bits are also read-only

Table 9 - Frame Alignment (FAR) Register Bit

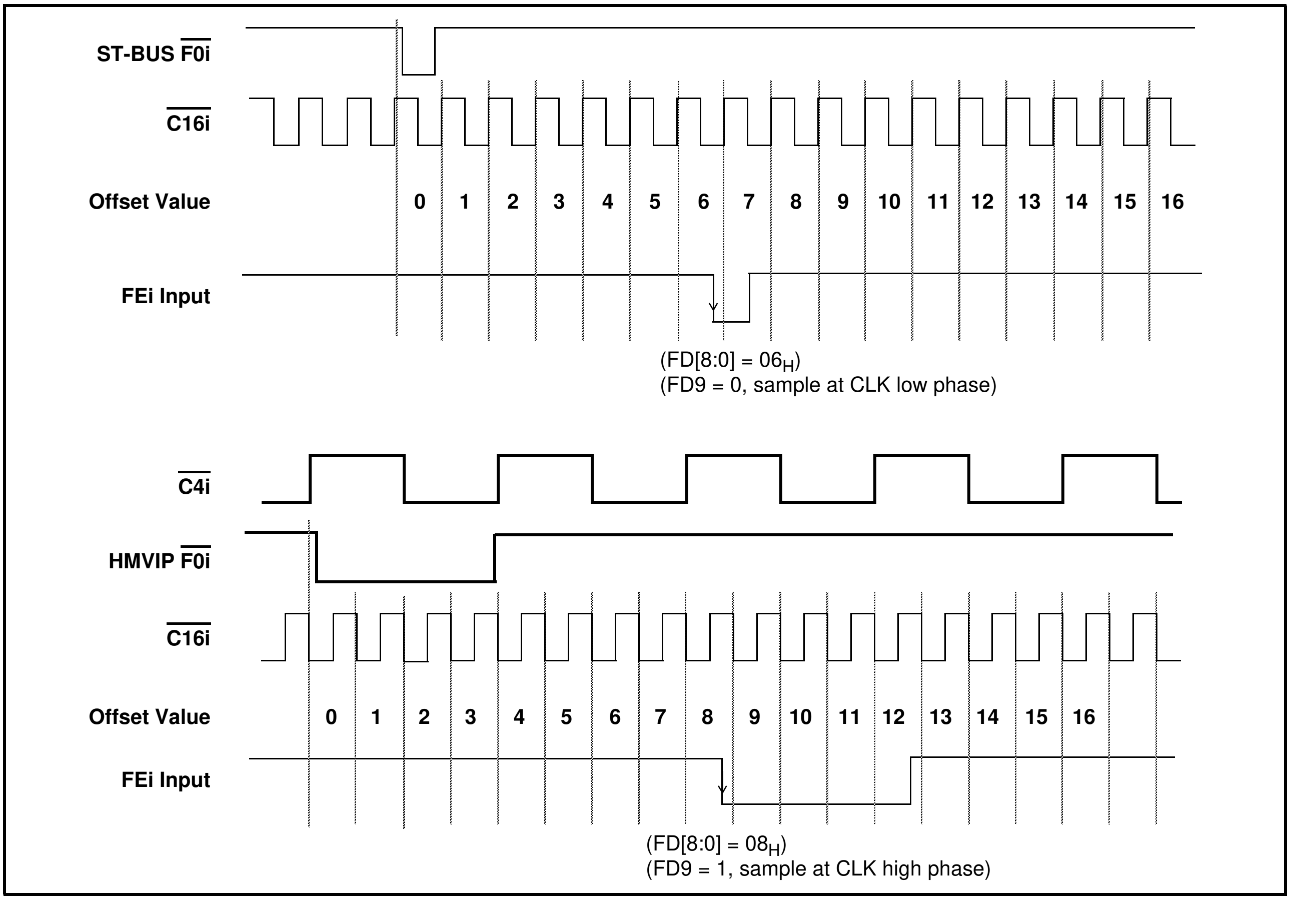

Figure 8 - Example for Frame Alignment Measurement

Read/Write Address: 04_H for DOS0 register,
05_H for DOS1 register,
06_H for DOS2 register,
07_H for DOS3 register,
08_H for DOS4 register,
09_H for DOS5 register,

Reset value: 0000_H for all DOS registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF32	IF31	IF30	**DLE3**	IF22	IF21	IF20	**DLE2**	IF12	IF11	IF10	**DLE1**	IF02	IF01	IF00	**DLE0**

DOS0 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF72	IF71	IF70	**DLE7**	IF62	IF61	IF60	**DLE6**	IF52	IF51	IF50	**DLE5**	IF42	IF41	IF40	**DLE4**

DOS1 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF112	IF111	IF110	**DLE11**	IF102	IF101	IF100	**DLE10**	IF92	IF91	IF90	**DLE9**	IF82	IF81	IF80	**DLE8**

DOS2 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF152	IF151	IF150	**DLE15**	IF142	IF141	IF140	**DLE14**	IF132	IF131	IF130	**DLE13**	IF122	IF121	IF120	**DLE12**

DOS3 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF192	IF191	IF190	**DLE19**	IF182	IF181	IF180	**DLE18**	IF172	IF171	IF170	**DLE17**	IF162	IF161	IF160	**DLE16**

DOS4 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF232	IF231	IF230	**DLE23**	IF222	IF221	IF220	**DLE22**	IF212	IF211	IF210	**DLE21**	IF202	IF201	IF200	**DLE20**

DOS5 register

Name (Note 1)	**Description**
IFn2, IFn1, IFn0	**Input Offset Bits 2,1 & 0.** These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the STio pin: i.e., to start a new frame. The input frame offset can be selected to +4 clock periods from the point where the external frame pulse input signal is applied to the $\overline{\text{F0i}}$ inputs of the device.Figure 9 -
DLEn	**Data Latch Edge.** ST-BUS mode: DLEn =0, if clock rising edge is at the 3/4 point of the bit cell. DLEn =1, if clock falling edge is at the 3/4 point of the bit cell.

Table 10 - Frame Delay Offset (DOS) Register Bits