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MT90866

Flexible 4 K x 2.4 K Channel Digital Switch with H.110 Interface and 2.4 K x 2.4 K Local Switch

Data Sheet

January 2006

Features

- 2,432 x 2,432 non-blocking switching among local streams
- 4,096 x 2,432 blocking switching between backplane and local streams
- 2,048 x 2,048 non-blocking switching among backplane streams
- Rate conversion between backplane and local streams
- Rate conversion among local streams
- Backplane interface accepts data rates of 8.192 Mb/s or 16.384 Mb/s
- Local interface accepts data rates of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s
- Sub-rate switching (2 or 4 bits) configuration for local streams at a data rate of 2.048 Mb/s
- Meets all the key H.110 mandatory signal requirements including timing
- Per-channel variable or constant throughput delay
- Per-stream input delay, programmable for local streams on a per bit basis
- Per-stream output advancement, programmable for backplane and local streams
- Per-channel direction control for backplane streams
- Per-channel message mode for backplane and local streams
- Per-channel high impedance output control for backplane and local streams
- Compatible to Stratum 4 Enhanced clock switching standard
  - Integrated PLL conforms to Telcordia GR-1244-CORE Stratum 4 Enhanced switching standard -Holdover Mode with holdover frequency stability of 0.07 ppm
    - Jitter attenuation from 1.52 Hz.
    - Time interval error (TIE) correction
    - Master and Slave mode operation
- Non-multiplexed microprocessor interface

Ordering Information

MT90866AG	344 Ball PBGA	Trays
MT90866AG2	344 Ball PBGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Connection memory block-programming for fast device initialization
- Tristate-control outputs for external drivers
- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for backplane and local streams
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- 3.3 V operation with 5 V tolerant inputs and I/O's
- 5 V tolerant PCI driver on CT-Bus I/O's

Applications

- Carrier-grade VoIP Gateways
- IP-PBX and PABX
- Integrated Access Devices
- Access Servers
- CTI Applications/CompactPCI® Platforms
- H.110, H.100, ST-BUS and proprietary Backplane Applications

Description

The MT90866 Digital Switch provides switching capacities of 4,096 x 2,432 channels between backplane and local streams, 2,432 x 2,432 channels among local streams and 2,048 x 2,048 channels among backplane streams. The local connected serial inputs and outputs have 32, 64 and 128 64 kb/s channels per frame with data rates of 2.048, 4.096 and 8.192 Mb/s respectively. The backplane connected serial inputs and outputs have 128 and 256 64 kb/s channels per frame with data rates of 8.192 and 16.384 Mb/s respectively.

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

The MT90866 also offers a sub-rate switching configuration which allows 2-bit wide 16 kb/s or 4-bit wide 32 kb/s data channels to be switched within the device.

The device has features that are programmable on a per-stream or a per-channel basis including message mode, input delay offset, output advancement offset, direction control, and high impedance output control.

The MT90866 supports all three of the H.110 specification required clocking modes: Primary Master, Secondary Master and Slave.

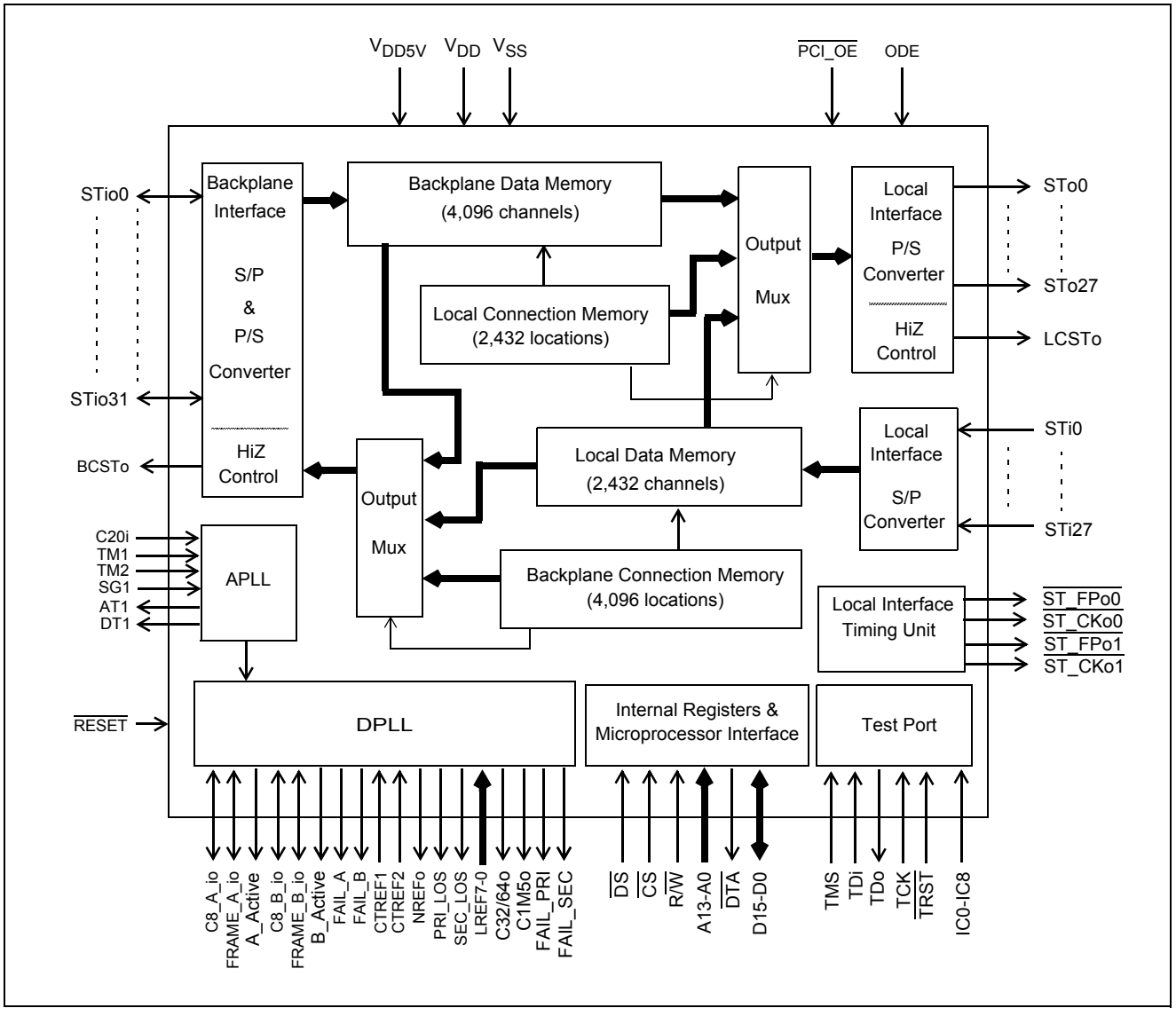

Figure 1 - Functional Block Diagram

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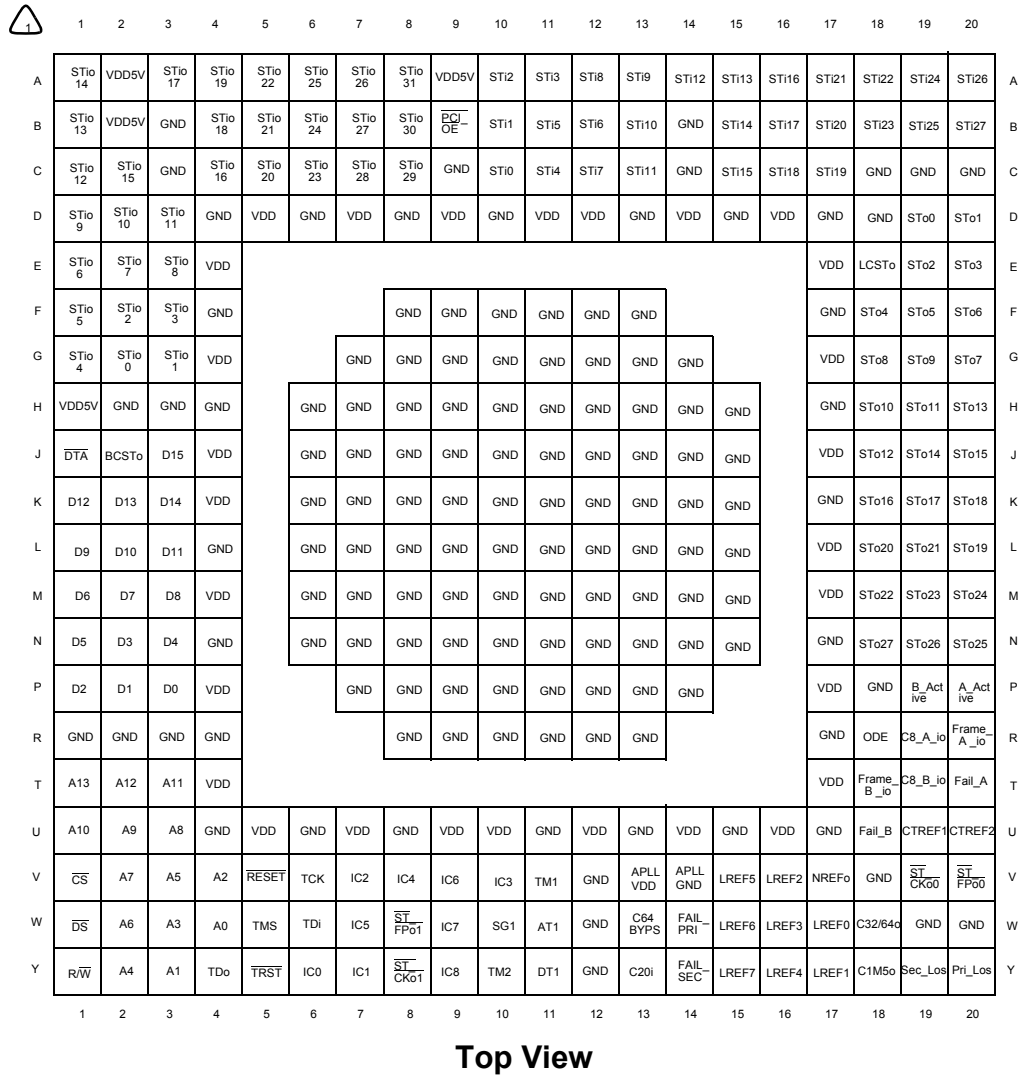
Changes Summary

The following table captures the changes from the September 2005 issue.

Page	Item	Change
9	Ball Signal Assignment	Added missing Ball signals.
11	Pin name: $\overline{\text{RESET}}$	Worst case 600 μs instead of 100 μs is specified for the delay that must be applied before performing the first microprocessor access after the release of $\overline{\text{RESET}}$ pin.
44	Section 20.0	The 600 μs delay requirement before performing the first microprocessor access after the release of $\overline{\text{RESET}}$ pin is added in this section for completeness.
80	Figure 40	Corrected 8 Mb/s stream channel to ch127

The following table captures the changes from the October 2003 issue.

Page	Item	Change
37, 58	Section 18.2 and Table 21	Added description clarifying that the MTIE reset must be set when the device is in the slave mode.
60	Table 22	Added MRST (bit 10) in MT90866 Mode Selection table
39, 41	Section 18.7 and Section 19.1	Deleted the intrinsic jitter descriptions in Section 18.7 and Section 19.1 and replaced them with “AC Electrical Characteristics†- Output Clock Jitter Generation (Unfiltered)” on page 76.
77, 78, 80	“AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 8 Mb/s” , “AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 16 Mb/s” and “AC Electrical Characteristics† - Local Serial Stream Input Timing” .	Input data sampling timings were updated for clarity purposes.



Top View

1 - A1 corner is identified by metallized markings.

Figure 2 - 27 mm x 27 mm PBGA (JEDEC MO-151) Pinout

Ball Signal Assignment

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	STIO14	C5	STIO20	F1	STIO5	H17	GND	L6	GND	N14	GND
A2	VDD5V	C6	STIO23	F2	STIO2	H18	STO10	L7	GND	N15	GND
A3	STIO17	C7	STIO28	F3	STIO3	H19	STO11	L8	GND	N17	GND
A4	STIO19	C8	STIO29	F4	GND	H20	STO13	L9	GND	N18	STO27
A5	STIO22	C9	GND	F8	GND	J1	$\overline{\text{DTA}}$	L10	GND	N19	STO26
A6	STIO25	C10	STI0	F9	GND	J2	BCSTO	L11	GND	N20	STO25
A7	STIO26	C11	STI4	F10	GND	J3	D15	L12	GND	P1	D2
A8	STIO31	C12	STI7	F11	GND	J4	VDD	L13	GND	P2	D1
A9	VDD5V	C13	STI11	F12	GND	J6	GND	L14	GND	P3	D0
A10	STI2	C14	GND	F13	GND	J7	GND	L15	GND	P4	VDD
A11	STI3	C15	STI15	F17	GND	J8	GND	L17	VDD	P7	GND
A12	STI8	C16	STI18	F18	STO4	J9	GND	L18	STO20	P8	GND
A13	STI9	C17	STI19	F19	STO5	J10	GND	L19	STO21	P9	GND
A14	STI12	C18	GND	F20	STO6	J11	GND	L20	STO19	P10	GND
A15	STI13	C19	GND	G1	STIO4	J12	GND	M1	D6	P11	GND
A16	STI16	C20	GND	G2	STIO0	J13	GND	M2	D7	P12	GND
A17	STI21	D1	STIO9	G3	STIO1	J14	GND	M3	D8	P13	GND
A18	STI22	D2	STIO10	G4	VDD	J15	GND	M4	VDD	P14	GND
A19	STI24	D3	STIO11	G7	GND	J17	VDD	M6	GND	P17	VDD
A20	STI26	D4	GND	G8	GND	J18	STO12	M7	GND	P18	GND
B1	STIO13	D5	VDD	G9	GND	J19	STO14	M8	GND	P19	B_ACTIVE
B2	VDD5V	D6	GND	G10	GND	J20	STO15	M9	GND	P20	A_ACTIVE
B3	GND	D7	VDD	G11	GND	K1	D12	M10	GND	R1	GND
B4	STIO18	D8	GND	G12	GND	K2	D13	M11	GND	R2	GND
B5	STIO21	D9	VDD	G13	GND	K3	D14	M12	GND	R3	GND
B6	STIO24	D10	GND	G14	GND	K4	VDD	M13	GND	R4	GND
B7	STIO27	D11	VDD	G17	VDD	K6	GND	M14	GND	R8	GND
B8	STIO30	D12	VDD	G18	STO8	K7	GND	M15	GND	R9	GND
B9	$\overline{\text{PCI\_OE}}$	D13	GND	G19	STO9	K8	GND	M17	VDD	R10	GND
B10	STI1	D14	VDD	G20	STO7	K9	GND	M18	STO22	R11	GND
B11	STI5	D15	GND	H1	VDD5V	K10	GND	M19	STO23	R12	GND
B12	STI6	D16	VDD	H2	GND	K11	GND	M20	STO24	R13	GND
B13	STI10	D17	GND	H3	GND	K12	GND	N1	D5	R17	GND
B14	GND	D18	GND	H4	GND	K13	GND	N2	D3	R18	ODE
B15	STI14	D19	STO0	H6	GND	K14	GND	N3	D4	R19	C8_A_IO
B16	STI17	D20	STO1	H7	GND	K15	GND	N4	GND	R20	FRAME_A_IO
B17	STI20	E1	STIO6	H8	GND	K17	GND	N6	GND	T1	A13
B18	STI23	E2	STIO7	H9	GND	K18	STO16	N7	GND	T2	A12
B19	STI25	E3	STIO8	H10	GND	K19	STO17	N8	GND	T3	A11
B20	STI27	E4	VDD	H11	GND	K20	STO18	N9	GND	T4	VDD
C1	STIO12	E17	VDD	H12	GND	L1	D9	N10	GND	T17	VDD
C2	STIO15	E18	LCSTO	H13	GND	L2	D10	N11	GND	T18	FRAME_B_IO
C3	GND	E19	STO2	H14	GND	L3	D11	N12	GND	T19	C8_B_IO
C4	STIO16	E20	STO3	H15	GND	L4	GND	N13	GND	T20	FAIL_A

Ball	Signal	Ball	Signal
U1	A10	W6	TDi
U2	A9	W7	IC5
U3	A8	W8	$\overline{\text{ST\_FPo1}}$
U4	GND	W9	IC7
U5	VDD	W10	SG1
U6	GND	W11	AT1
U7	VDD	W12	GND
U8	GND	W13	C64BYPS
U9	VDD	W14	FAIL_PRI
U10	VDD	W15	LREF6
U11	GND	W16	LREF3
U12	VDD	W17	LREF0
U13	GND	W18	C32/64o
U14	VDD	W19	GND
U15	GND	W20	GND
U16	VDD	Y1	R/$\overline{\text{W}}$
U17	GND	Y2	A4
U18	FAIL_B	Y3	A1
U19	CTREF1	Y4	TDo
U20	CTREF2	Y5	$\overline{\text{TRST}}$
V1	$\overline{\text{CS}}$	Y6	IC0
V2	A7	Y7	IC1
V3	A5	Y8	$\overline{\text{ST\_CKo1}}$
V4	A2	Y9	IC8
V5	$\overline{\text{RESET}}$	Y10	TM2
V6	TCK	Y11	DT1
V7	IC2	Y12	GND
V8	IC4	Y13	C20I
V9	IC6	Y14	FAIL_SEC
V10	IC3	Y15	LREF7
V11	TM1	Y16	LREF4
V12	GND	Y17	LREF1
V13	APLLVDD	Y18	C1M5O
V14	APLLGND	Y19	SEC_LOS
V15	LREF5	Y20	PRI_LOS
V16	LREF2		
V17	NREFo		
V18	GND		
V19	$\overline{\text{ST\_CKo0}}$		
V20	$\overline{\text{ST\_FPo0}}$		
W1	$\overline{\text{DS}}$		
W2	A6		
W3	A3		
W4	A0		
W5	TMS		

Pin Description

PBGA Ball Number	Name	Description
D5, D7, D9, D11, D12, D14, D16, E4, E17, G4, G17, J4, J17, K4, L17, M4, M17, P4, P17, T4, T17,U5, U7, U9, U10, U12, U14, U16	V_{DD}	**+3.3 Volt Power Supply**.
A2,A9,B2,H1	V_{DD5V}	**+5.0 V/+3.3 V Power Supply**. If 5 V power supply is tied to these pins, STio0-31 pins will meet 5 V PCI requirements. If 3.3 V power supply is tied to these pins, STio0-31 pins will meet 3.3 V PCI requirements.
B3, B14,C3, C9, C14, C18, C19, C20, D4, D6, D8, D10, D13, D15, D17, D18, F4, F8-F13, F17, G7-G14, H2, H3, H4, H6-H15, H17, J6-J15, K6-K15, K17, L4, L6-L15, M6-M15, N4, N6-15, N17, P7-P14, P18, R1, R2, R3, R4, R8-R13, R17, U4, U6, U8, U11, U13, U15, U17, V12, V18, W12, W19, W20, Y12	V_{SS}	**Ground**.
V13	$APLLV_{DD}$	**+3.3 Volt Analog PLL Power Supply**. No special filtering is required for this pin.
V14	$APLLV_{ss}$	**Analog PLL Ground**
V5	$\overline{RESET}$	**Device Reset (5 V Tolerant Input).** This input (active low) puts the device in its reset state; this state clears the device's internal counters and registers. To ensure proper reset action, the reset pin must be low for longer than 400 ns. To ensure proper operation, a delay of 600 µs must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high. The device reset also tristates STo0-27 and STio0-31, and sets the LCSTo and BCSTo pins. When in a $\overline{RESET}$ condition, the C8_A_io, FRAME_A_io, C8_B_io, and FRAME_B_io signals are tri-stated.
G2, G3, F2, F3, G1, F1, E1, E2, E3, D1, D2, D3, C1, B1, A1, C2	STio0-3, STio4-7, STio8-11, STio12-15	**Serial Input/Output Streams 0 - 15 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept serial TDM data streams at 8.192 Mb/s with 128 channels per stream. In the 16 Mb/s mode, these pins accept serial TDM data streams at 16.384 Mb/s with 256 channels per stream respectively.

Pin Description (continued)

PBGA Ball Number	Name	Description
C4, A3, B4, A4, C5, B5, A5, C6, B6, A6, A7, B7, C7, C8, B8, A8	STio16 - 19, STio20 - 23, STio24 - 27, STio28 - 31	**Serial Input/Output Streams 16 - 31 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept serial TDM data streams at 8.192 Mb/s with 128 channels per stream. In the 16 Mb/s mode, these pins are tristated internally and should be connected to ground.
C10, B10, A10, A11	STi0-3	**Serial Input Streams 0 - 3 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8Mb/s mode, these inputs accept data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
C11, B11, B12, C12	STi4 - 7	**Serial Input Streams 4 - 7 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these inputs accept data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
A12, A13, B13, C13	STi8 - 11	**Serial Input Streams 8 - 11 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these inputs accepts data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
A14, A15, B15, C15	STi12 - 15	**Serial Input Streams 12 - 15 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these inputs accept data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
A16, B16, C16, C17, B17, A17, A18, B18, A19, B19, A20, B20	STi16 - 27	**Serial Input Streams 16 - 27 (5 V Tolerant Inputs)**. In 2 Mb/s mode, these inputs accept data rates of 2.048 Mb/s with 32 channels per stream respectively. In 4 Mb/s or 8 Mb/s mode, the STi16 - 18 inputs accept data rates of 4.096 or 8.192 Mb/s with 64 or 128 channels per stream respectively. In 4 Mb/s or 8 Mb/s mode the STi19 - 27 inputs should be driven low. No sub-rate switching mode is offered for STi16-27.
D19, D20, E19, E20	STo0 - 3	**Serial Output Streams 0 - 3 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.
F18, F19, F20, G20	STo4 - 7	**Serial Output Streams 4 - 7 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.
G18, G19, H18, H19	STo8 - 11	**Serial Output Streams 8 - 11 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.
J18, H20, J19, J20	STo12 - 15	**Serial Output Streams 12 - 15 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.

Pin Description (continued)

PBGA Ball Number	Name	Description
K18, K19, K20, L20, L18, L19, M18, M19, M20, N20, N19, N18	STo16 - 27	**Serial Output Streams 16 to 27 (5 V Tolerant Tri-state Outputs).** In 2 Mb/s mode, these outputs have data rate of 2.048 Mb/s with 32 channels per stream. In 4 Mb/s or 8 Mb/s mode, the STo16 - 18 outputs have data rates of 4.096 Mb/s or 8.192 Mb/s with 64 or 128 channels per stream respectively; STo19 - 27 are driven low. No sub-rate switching mode is offered for STo16-27.
R18	ODE	**Output Drive Enable (5 V Tolerant Input).** When this pin is low, STo0 to STo27, STio0 to STio31, C1M5o, C32/64o, ST_CKo0, ST_CKo1, ST_FPo0 and ST_FPo1 outputs are all in high-impedance state. When ODE is high all of the aforementioned pins are active.
J2	BCSTo	**Backplane Control Signal (Output)**. This pin is used for backplane external tristate controllers. When this signal is high, the corresponding output channels are in a high impedance state. BCSTo's bit rate is 32.768 MHz.
E18	LCSTo	**Local Control Signal (Output).** This pin is used for local external tristate control. When this signal is high, the corresponding ouput channels are in a high impedance state. The bit rate is 32.768 MHz.
Y13	C20i	**Master Clock (5 V Tolerant Input).** This pin accepts a 20.000 MHz clock.
R19	C8_A_io	**Clock A (5 V Tolerant I/O).** This is a 8.192 MHz clock with 50% duty cycle.
R20	FRAME_A_io	**Frame Reference A (5 V Tolerant I/O).** This is a 122 ns wide, negative pulse, with 125 us period.
P20	A_Active	**A Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_A_io and the FRAME_A_io pins are inputs or outputs. When Bit 13 of the DOM1 register is low, this pin drives low and the C8_A_io and FRAME_A_io output drivers are disabled. When Bit 13 of the DOM1 register is high, this pin drives high and the C8_A_io and FRAME_A_io output drivers are enabled.
T19	C8_B_io	**Clock B (5 V Tolerant I/O).** This is a 8.192 MHz clock with 50% duty cycle.
T18	FRAME_B_io	**Frame Reference B (5 V Tolerant I/O).** This is a 122 ns wide, negative pulse, with 125 us period.
P19	B_Active	**B Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_B_io and the FRAME_B_io pins are inputs or outputs. When Bit 14 of the DOM1 register is low, this pin drives low and the C8_B_io and FRAME_B_io output drivers are disabled. When Bit 14 of the DOM1 register is high, this pins drives high and the C8_B_io and FRAME_B_io output drivers are enabled.
T20	FAIL_A	**A Failure (Output).** When the C8_A_io or the FRAME_A_io signal fails, this signal goes to high.
U18	FAIL_B	**B Failure (Output).** When the C8_B_io or the FRAME_B_io signal fails, this signal goes to high.

Pin Description (continued)

PBGA Ball Number	Name	Description
U19	CTREF1	**CT-Bus Reference 1 (5 V Tolerant Input).** This pin accepts 8 KHz, 1.544 MHz or 2.048 MHz network timing reference.
U20	CTREF2	**CT-Bus Reference 2 (5 V Tolerant Input).** This pin accepts 8 KHz, 1.544 MHz or 2.048 MHz network timing reference.
W17, Y17, V16, W16, Y16, V15, W15, Y15	LREF0- 7	**Local Reference (5 V Tolerant Inputs).** These pins accept 8 KHz, 1.544 MHz or 2.048 MHz local timing reference.
V17	NREFo	**Network Reference Output (Output).** Any local reference can be switched to this output. The output data rate can be either the same as the selected reference input data rate or divided to be 8 KHz.
Y20	PRI_LOS	**Primary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that PRIMARY REFERENCE is not valid. Combined with SEC_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
Y19	SEC_LOS	**Secondary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that SECONDARY REFERENCE is not valid. Combined with the PRI_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
W14	FAIL_PRI	**Primary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the PLS bit of the DPLL House Keeping Register (DHKR). When the primary reference fails, this signal goes to 1.
Y14	FAIL_SEC	**Secondary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the SLS bit of the DPLL House Keeping Register (DHKR). When the secondary reference fails, this signal goes to 1.
W18	C32/64o	**C32/64o Clock (5 V Tolerant Output).** A 32.768 MHz output clock when the DPLL Clock Monitor register bit (CKM) is low. A 65.536 MHz clock when the DPLL Clock Monitor register bit (CKM) is high.
Y18	C1M5o	**C1.5o Clock (5 V Tolerant Output).** A 1.544 MHz output clock.
V20	$\overline{\text{ST\_FPo0}}$	**ST-Bus Frame Pulse Output (5 V Tolerant Output).** The width of this output ST-Bus frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 KHz.
V19	$\overline{\text{ST\_CKo0}}$	**ST-Bus Clock Output (5 V Tolerant Output).** The frequency of this output ST-Bus clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
W8	$\overline{\text{ST\_FPo1}}$	**ST-Bus Frame Pulse Output (5 V Tolerant Output)**. The width of this output ST-Bus frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 KHz.
Y8	$\overline{\text{ST\_CKo1}}$	**ST-Bus Clock Output (5 V Tolerant Output)**. The frequency of this output ST-Bus clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
V1	$\overline{\text{CS}}$	**Chip Select (5 V Tolerant Input).** This active low input is used by the microprocessor to access the microport.

Pin Description (continued)

PBGA Ball Number	Name	Description
W1	$\overline{DS}$	**Data Strobe (5 V Tolerant Input).** This active low input works in conjunction with $\overline{CS}$ to initiate the read and write cycles.
Y1	R/$\overline{W}$	**Read/Write (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0 - D15) during the microprocessor access.
W4, Y3, V4, W3, Y2, V3, W2, V2, U3, U2, U1, T3, T2, T1	A0 - A13	**Address 0 - 13 (5 V Tolerant Inputs).** These are the address lines to the internal memories and registers.
P3, P2, P1, N2, N3, N1, M1, M2, M3, L1, L2, L3, K1, K2, K3, J3	D0 - D15	**Data Bus 0 - 15 (5 V Tolerant I/Os)**. These pins form the 16-bit data bus of the microport.
J1	$\overline{DTA}$	**Data Transfer Acknowledge (5 V Tolerant Output)**. This active low output indicates that a data bus transfer is completed. A pull-up resistor is required to hold a high level.
B9	$\overline{PCI\_OE}$	**PCI Output Enable (3.3 V Tolerant Input)**. This active low input is the control signal used to tristate the STio0 - 31 pins during hot-swapping. During normal operation this signal should be low.
W13	C64BYPS	**PLL Bypass Clock Input (5 V Tolerant Input).** Used for device testing. In functional mode, this input MUST be low.
V11	TM1	**APLL Test Pin 1 (3.3 V Input).** Use for APLL testing only. In normal operation, this input should be connected to ground.
Y10	TM2	**APLL Test Pin 2 (3.3 V Input).** Use for APLL testing only. In normal operation, this input should be connected to ground.
W10	SG1	**APLL Test Control (3.3 V Input).** Use for APLL testing only. In normal operation, this input should be connected to ground.
W11	AT1	**Analog Test Access (5 V Tolerant I/O).** Use for APLL testing only. No connection for normal operation.
Y11	DT1	**Digital Test Access Output (5 V Tolerant Output).** Use for APLL testing only. No connection for normal operation.
W5	TMS	**Test Mode Select (3.3 V Input with Internal pull-up).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
W6	TDi	**Test Serial Data In (3.3 V Input with Internal pull-up)**. JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
Y4	TDo	**Test Serial Data Out (3.3 V Tolerant Tri-state Output)**. JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.

Pin Description (continued)

PBGA Ball Number	Name	Description
V6	TCK	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic. This pin should be low when JTAG is not enabled.
Y5	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with Internal pull-up).** Asynchronously initializes the JTAG TAP Controller by putting it in the Test-Logic-Reset state. This pin should be pulled low to ensure that the MT90866 is in normal functional mode.
Y6	IC0	Leave unconnected for normal operation.
Y7	IC1	Leave unconnected for normal operation.
V7	IC2	In normal operation this pin MUST be connected to ground.
V10	IC3	Leave unconnected for normal operation.
V8	IC4	Leave unconnected for normal operation.
W7	IC5	Leave unconnected for normal operation.
V9	IC6	Leave unconnected for normal operation.
W9	IC7	Leave unconnected for normal operation.
Y9	IC8	Leave unconnected for normal operation.

1.0 Device Overview

The MT90866 can switch up to 4,096 × 2,432 channels while providing a rate conversion capability. It is designed to switch 64 kb/s PCM or N X 64 kb/s data between the backplane and local switching applications. The device maintains frame integrity in data applications and minimum throughput delay for voice application on a per channel basis.

The backplane interface can operate at 8.192 Mb/s in CT-Bus mode or 16.384 Mb/s in ST-BUS mode and is arranged in 125 µs wide frames that contain 128 or 256 channels respectively. A built-in rate conversion circuit allows users to interface between backplane and local interfaces which operates at 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s. When the device is in the local sub-rate switching mode, 2-bit 16 kb/s or 4-bit 32 kb/s data channels can be switched within the device. The local sub-rate switching mode is available in 2 Mb/s mode only.

By using Zarlink's message mode capability, the microprocessor can access input and output time slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices.

2.0 Functional Description

A Functional Block Diagram of the MT90866 is shown in Figure 1, "Functional Block Diagram" on page 2. It is designed to interface CT-Bus and ST-BUS serial streams from a backplane source and ST-BUS serial streams from a local source.

3.0 Frame Alignment Timing

In the ST-BUS or the CT-Bus mode, the C8_A_io or C8_B_io pin accepts an 8.192 MHz clock for the frame pulse alignment. The FRAME_A_io or FRAME_B_io is the frame pulse signal which goes low at the frame boundary for 122 ns. The frame boundary is defined by the rising edge of the C8_A_io or C8_B_io clock during the low cycle of the frame pulse. Figure 3, "CT-Bus Timing for 8 Mb/s Backplane Data Streams" on page 17 is the CT-Bus timing for the backplane 8.192 Mb/s data streams and Figure 4, "ST-BUS Timing for 16 Mb/s Backplane Data Streams" on page 18 is the ST-BUS timing for the 16.384 Mb/s backplane data stream.

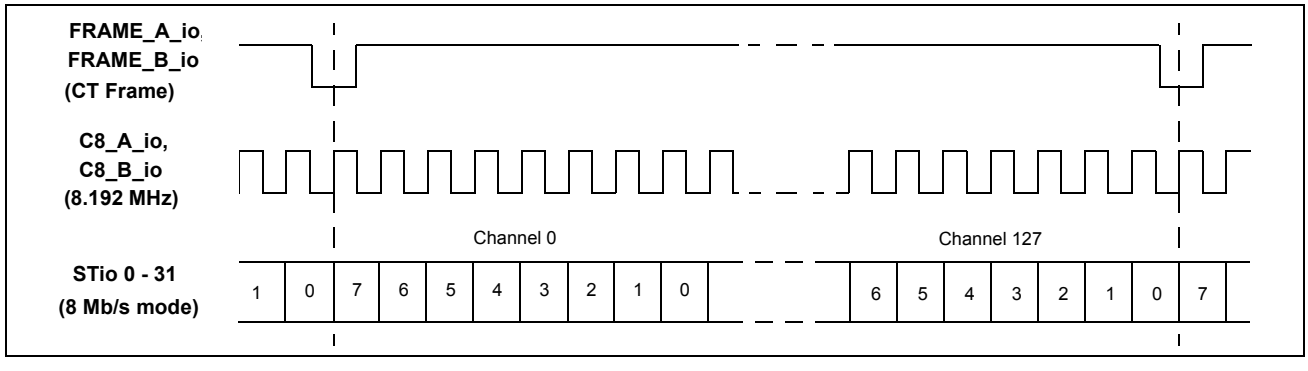


Figure 3 - CT-Bus Timing for 8 Mb/s Backplane Data Streams

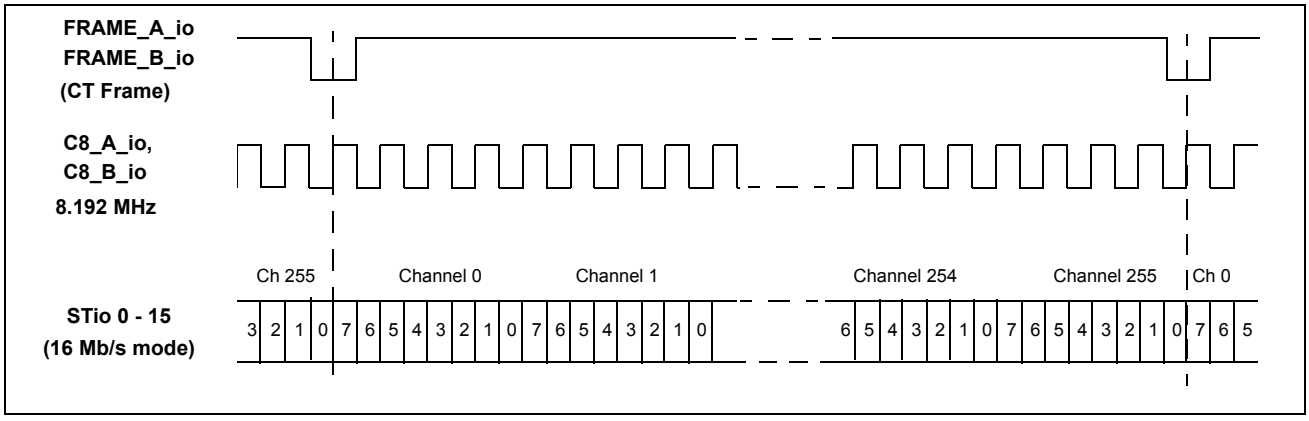


Figure 4 - ST-BUS Timing for 16 Mb/s Backplane Data Streams

4.0 Switching Configuration

The device has two operation modes at different data rates for the backplane interface and five operation modes for the local interface. These modes can be programmed via the Device Mode Selection (DMS) register. Mode selections between the backplane and local interfaces are independent.

4.1 Backplane Interface

The backplane interface can be programmed to accept data streams of 8 Mb/s or 16 Mb/s. When H.110 mode is enabled, STio0 to STio31 have a data rate of 8.192 Mb/s. When ST-BUS mode is enabled, STio0 to STio15 have a data rate of 16.384 Mb/s. Table 1 on page 18 describes the data rates and mode selections for the backplane interface.

4.2 Local Interface

Five operation modes, 2 Mb/s, 4 Mb/s, 8 Mb/s, 2-bit sub-rate and 4-bit sub-rate switching, can be selected for the local ST-BUS interface. The local interface is divided into five groups. Group 0 contains STi/STo0-3, Group 1 contains STi/STo4-7, Group 2 contains STi/STo8-11, Group 3 contains STi/STo12-15 and Group 4 contains STi/STo16-27. Each group can be selected individually through the Device Mode Selection (DMS) register. Streams belonging to the same group have the same operation mode. For Groups 0 to 3, any one of the five operation modes can be selected. Input data streams STi0-15 and output data streams, STo0 -15 can be selected according to the group to which they belong. STi16-27 and output data streams STo16-27 belong to Group 4 and can operate in 2 Mb/s mode. In Group 4, only input data streams Sti16-18 and output data streams Sto16-18 can operate in 4 Mb/s and 8 Mb/s mode. When operating Group 4 at 4 Mb/s or 8 Mb/s the unused output streams, STo19-27 are driven low. No sub-rate modes are available for Group 4 data streams. See Table 2 on page 19 to Table 6 on page 20 for a description of the data rates and mode selection for the local ST-BUS interface.

BMS bit of the DMS Register	Modes	Backplane Interface
0	8.192 Mb/s	STio0 - 31
1	16.384 Mb/s	STio0 - 15

Table 1 - Mode Selection for Backplane Streams

DMS Register Bits			Modes	Usable Streams
LG02	LG01	LG00		
0	0	0	8.192 Mb/s	STi0 - 3, STo0 - 3
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 2 - Mode Selection for Local STi0 - 3 and STo0 - 3 Streams, Group 0

DMS Register Bits			Modes	Usable Streams
LG12	LG11	LG10		
0	0	0	8.192 Mb/s	STi4 - 7, STo4 -7
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 3 - Mode Selection for Local STi4 - 7 and STo4 - 7 Streams, Group 1

DMS Register Bits			Modes	Usable Streams
LG22	LG21	LG20		
0	0	0	8.192 Mb/s	STi8 - 11, STo8 - 11
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 4 - Mode Selection for Local STi8 - 11 and STo8 - 11 Streams, Group 2

DMS Register Bits			Modes	Usable Streams
LG32	LG31	LG30		
0	0	0	8.192 Mb/s	STi12-15, STo12-15
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 5 - Mode Selection for Local STi12 - 15 and ST012 - 15 Streams, Group 3

DMS Register Bits		Modes	Usable Streams
LG41	LG40		
0	0	8.192 Mb/s	STi16 - 18, STo16 - 18
0	1	4.096 Mb/s	
1	0	2.048 Mb/s	STi16 - 27, STo16 - 27

Table 6 - Mode Selection for Local STi16 - 27 and STo16 - 27 Streams, Group 4

5.0 Local Input Delay Selection

The local input delay selection allows individual local input streams to be aligned and shifted against the input frame pulse (FRAME_A_io or FRAME_B_io). This feature compensates for the variable path delays in the local interface. Such delays can occur in large centralized and distributed switching system.

Each local input stream can have its own bit delay offset value by programming the local input bit delay selection registers (LIDR0 to LIDR9). See Table 12, "Local Input Bit Delay Registers (LIDR0 to LIDR9) Bits" on page 50, for the contents of these registers. Possible bit adjustment can range up to +7 3/4 bit periods forward with resolution of 1/4 bit period. See Table 13 on page 51 and Figure 19 on page 51 for local input delay programming.

6.0 Output Advancement Selection

The MT90866 allows users to advance individual backplane or local output streams with respect to the frame boundary. This feature is useful in compensating variable output delays caused by various output loading conditions. Each output stream can have its own advancement value programmed by the output advancement registers. The backplane output advancement registers (BOAR0 to BOAR3) are used to program the backplane output advancement. The local output advancement registers (LOAR0 to LOAR3) are used to program the local output advancement. Possible adjustment for local and backplane output data streams is 22.5 ns with a resolution of 7.5 ns. The advancement is independent of the output data rate. Table 14 on page 52 and Figure 20, "Example of Backplane Output Advancement Timing" on page 52, and Table 15 on page 53 and Figure 21, "Local Output Advancement Timing" on page 53 describe the details of the output advancement programming for the backplane and local interfaces respectively.

7.0 Local Output Timing Considerations

The output data of the MT90866's local side is slightly advanced with respect to the frame and bit boundary as defined by the local output clocks and frame pulses (ST_FPo0, ST_CKo0, ST_FPo1, ST_CKo1). The advancement is in the range of 5 ns to 17 ns. Despite this advancement, the MT90866 will operate within the parameters specified in the datasheet because input data are usually sampled at the 3/4 or 1/2 point of the bit cell. However, the user should be cautious when introducing additional delay to the clock signals only (e.g., by passing them through glue logic, FPGA, or CPLD), which will introduce a few nanoseconds of delay relative to the data. If the clock signal is delayed, data will be advanced from the receiver device's point of view. This may cause errors in sampling the data. Using an example where a 3/4 sampling point is used, there is about 30 ns from the sampling point to the end of the bit cell. With a worst-case of 17 ns advancement, the timing margin will be approximately 13 ns. Any additional delays applied to the local output clocks (ST_CKo0 and ST_CKo1) must not exceed 13 ns minus the hold time of the receiving device. Delays applied to both clocks and data equally will not impact the device operation.

8.0 Memory Block Programming

The MT90866 block programming mode (BPM) register provides users with the capability of initializing the local and backplane connection memories in two frames. The local connection memory is partitioned into high and low parts. Bit 13 - bit 15 of every backplane connection memory location will be programmed with the pattern stored in bit 6 - bit 8 of the BPM register. Bit 13 - bit 15 of every local connection memory low location will be programmed with the pattern stored in bits 3 to 5 of the BPM register. The other bit positions of the backplane connection memory, the local low connection memory and all bits of the local high connection memory are loaded with zeros. See Figure 5, "Block Programming Data in the Connection Memories" on page 22 for the connection memory contents when the device is in block programming mode.

The block programming mode is enabled by setting the memory block program (MBP) bit of the Control register to high. After the block programming enable (BPE) bit of the BPM register is set to high, the block programming data will be loaded into bits 13 to 15 of every backplane connection memory location and bits 13 to 15 of every local connection memory low location. The other connection memory bits are loaded with zeros. When the memory block programming is completed, the device resets the BPE bit to low. See Table 11 on page 49 for the bit assignment of the BPM register.

9.0 Delay Through the MT90866

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications it is recommended to select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications it is recommended to select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the BTM2 - BTM0 bits of the backplane connection memory or LTM0 - LTM2 bits of the local connection memory as described in Table 25 on page 63 and Table 29 on page 65, respectively.

9.1 Variable Delay Mode

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams. The minimum delays achievable in the MT90866 device are 3-channel delay, 5-channel delay, and 10-channel delay for the 2 MB/s, 4 MB/s, and 8 MB/s respectively. The maximum delay is one frame plus three channels, one frame plus five channels, and one frame plus ten channels for the 2 Mb/s, 4 Mb/s and 8 Mb/s modes respectively.

For the backplane interface, the variable delay mode can be programmed through the backplane connection memory bits, BTM2 - BTM0. When BTM2 - BTM0 are programmed to "000", it is a per-channel variable delay from

local input to the backplane output. When BTM2 - BTM0 are set to “010”, it is a per-channel variable delay from backplane input to backplane output.

For the local interface, the variable delay mode can be programmed through the local connection memory low bits, LTM2 - LTM0. When LTM2 - LTM0 is programmed to “000”, it is a per-channel variable delay from local input to local output. When LTM2 - LTM0 is set to “010”, it is a per-channel variable delay from backplane input to local output.

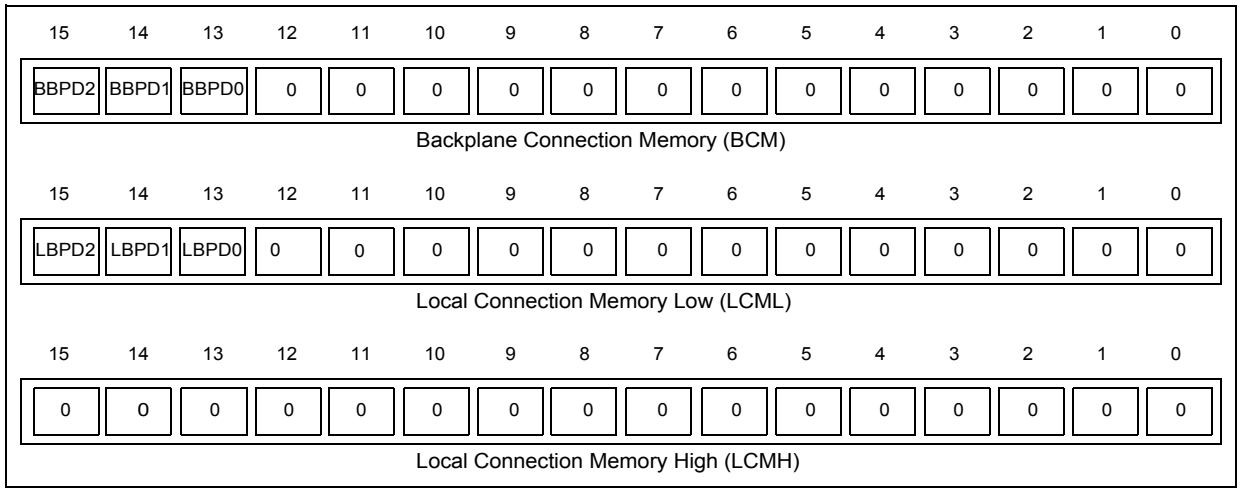


Figure 5 - Block Programming Data in the Connection Memories

9.2 Constant Delay Mode

In this mode, a multiple data memory buffer is used to maintain frame integrity in all switching configurations by using three pages of Data Memory where a channel written in any of the buffers during frame N is always read out during frame N+2.

For the backplane interface, when BTM2 - BTM0 is programmed to “001”, it is a per-channel constant delay mode from local input to backplane output. When BTM2 - BTM0 is programmed to “011”, it is a per-channel constant delay from backplane input to backplane output.

For the local interface, when LTM2 - LTM0 is programmed to “001”, it is a per-channel constant delay mode from local input to local output. When LTM2 - LTM0 is set to “011”, it is a per-channel constant delay mode from backplane input to local output.

10.0 Microprocessor Interface

The MT90866 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed bus structure. The required microprocessor signals are the 16-bit data bus (D15-D0), 14-bit address bus (A13-A0) and 4 control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 44, "Motorola Non-Multiplexed Bus Timing" on page 83 for the Motorola non-multiplexed bus timing.

The MT90866 microprocessor port provides access to the internal registers, the connection and data memories. All locations provide read/write access except for the Local and Backplane Bit Error Rate registers (LBERR and BBERR) and Data Memory which can only be read by the users.

10.1 $\overline{DTA}$ Data Transfer Acknowledgment Pin

The $\overline{DTA}$ pin of the microprocessor is driven LOW by internal logic to indicate that a data bus transfer is completed. When the bus cycle ends, this pin switches to the high impedance state. An external pull-up of between 1 KΩ and 10 KΩ is required at this output.

11.0 Address Mapping of Memories and Registers

The address bus on the microprocessor interface selects the internal registers and memories of the MT90866. If the address bit A13 is low, then the registers are addressed by A12 to A0 as shown in Table 7 on page 23.

A13 - A0	Location
0000_H	Control Register, CR
0001_H	Device Mode Selection Register, DMS
0002_H	Block Programming Mode Register, BPM
0003_H	Reserved
0004_H	Local Input Bit Delay Register 0, LIDR0
0005_H	Local Input Bit Delay Register 0, LIDR1
0006_H	Local Input Bit Delay Register 2, LIDR2
0007_H	Local Input Bit Delay Register 3, LIDR3
0008_H	Local Input Bit Delay Register 4, LIDR4
0009_H	Local Input Bit Delay Register 5, LIDR5
$000A_H$	Local Input Bit Delay Register 6, LIDR6
$000B_H$	Local Input Bit Delay Register 7, LIDR7
$000C_H$	Local Input Bit Delay Register 8, LIDR8
$000D_H$	Local Input Bit Delay Register 9, LIDR9
$000E_H$ to $001B_H$	Reserved
$001C_H$	Backplane Output Advancement Register 0, BOAR0
$001D_H$	Backplane Output Advancement Register 1, BOAR1
$001E_H$	Backplane Output Advancement Register 2, BOAR2
$001F_H$	Backplane Output Advancement Register 3, BOAR3
0020_H	Local Output Advancement Register 0, LOAR0
0021_H	Local Output Advancement Register 1, LOAR1
0022_H	Local Output Advancement Register 2, LOAR2
0023_H	Local Output Advancement Register 3, LOAR3
0024_H to 0026_H	Reserved
0027_H	Local BER Input Selection Register, LBIS
0028_H	Local BER Register, LBERR
0029_H	Backplane BER Input Selection Register, BBIS
$002A_H$	Backplane BER Register, BBERR
$002B_H$	DPLL Operation Mode Register 1, DOM1

Table 7 - Address Map For Internal Registers (A13 = 0)

A13 - A0	Location
$002C_H$	DPLL Operation Mode Register 2, DOM2
$002D_H$	DPLL Output Adjustment Register, DPOA
$002E_H$	DPLL House Keeping Register, DHKR

Table 7 - Address Map For Internal Registers (A13 = 0) (continued)

If A13 is high, the remaining address input lines are used to select the data and connection memory positions corresponding to the serial input or output data streams as shown in Table 8 on page 25.

The Control register (CR), the Device Mode Selection register (DMS) and the Block Programming Mode register (BPM) control all the major functions of the device. The DMS and BPM should be programmed immediately after system power up to establish the desired switching configuration as explained in the Frame Alignment Timing and Switching Configurations sections. The Control register is used to select Data or Connection Memory for microport operations, ST-BUS output frame and clock modes, and to set Memory Block Programing and Bit Error Rate Testing.

The Control register (CR) consists of the memory block programming bit (MBP) and the memory select bits (MS2-0). The memory block programming bit allows users to program the entire connection memory in two frames (see Memory Block Programming section). The memory select bits control the selection of the connection memories or the data memories. See Table 9 on page 46 for content of the Control register.

The DMS register consists of the backplane and the local mode selection bits (BMS, LG41 - LG40, LG32 - LG30, LG22 - LG20, LG12 - LG10 and LG02 - LG00) that are used to enable various switching modes for the backplane and the local interfaces respectively. See Table 10 on page 47 for the content of the DMS register.

The BPM register consists of the block programming data bits (LBPD2-0 and BBPD2-0) and the block programming enable bit (BPE). The block programming enable bit allows users to program the entire backplane and local connection memories in two frames (see Memory Block Programming section). If the ODE pin is low, the backplane CT-Bus is in input mode and the local output drivers are in high impedance state. If the ODE pin is high, all the backplane CT-Bus and local ST-BUS output drivers are controlled on a per channel basis by backplane and local connection memories, respectively. By programming BTM2 through BTM0 bits to “110” in the backplane connection memory, the user can control the per-channel input on the backplane interface. For the local interface, users can program LTM2 -0 bits to “110” in the local connection memory to control the per-channel high impedance output on the local ST-BUS. See Table 11 on page 49 for the content of the BPM register.

A13 (Note 1)	Stream Address (ST0-31)						Channel Address (Ch0-255)								
	A12	A11	A10	A9	A8	Stream #	A7	A6	A5	A4	A3	A2	A1	A0	Channel #
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	Ch 63 (Note 3 & 6)
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	1	1	1	1	1	1	0	Ch 126
1	1	1	0	1	1	Stream 27	0	1	1	1	1	1	1	1	Ch 127 (Note 4 & 7)
1	1	1	1	0	0	Stream 28	.	.	.	.	.	.	.	.	.
1	1	1	1	0	1	Stream 29	.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	Stream 30	1	1	1	1	1	1	1	0	Ch 254
1	1	1	1	1	1	Stream 31	1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Notes:
1. Bit A13 must be high for access to data and connection memory positions. Bit A13 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2 Mb/s.
3. Channels 0 to 63 are used when serial stream is at 4 Mb/s.
4. Channels 0 to 127 are used when serial stream is at 8 Mb/s.
5. Channels 0 to 255 are used when serial stream is at 16 Mb/s.
6. Channels 0 to 63 are used when local serial stream is in 4-bit wide sub-rate switching mode.
7. Channels 0 to 127 are used when local serial stream is in 2-bit wide sub-rate switching mode.

Table 8 - Address Map for Memory Locations (A13 = 1)

12.0 Backplane Connection Memory

The backplane connection memory controls the switching configuration of the backplane interface. Locations in the backplane connection memory are associated with particular STio streams.

The BTM2 - 0 bits of each backplane connection memory allows the per-channel selection for the message or the connection mode, the constant or the variable delay mode, the high impedance control of the STio driver or the bit error test enable. See Table 25 on page 63 for the content per-channel control function.

In the switching mode, the contents of the backplane connection memory stream address bits (BSAB4-0) and channel address bits (BCAB7-0) define the source information (stream and channel) of the time slot that will be switched to the backplane STio streams. During the message mode, only the lower 8 bits (8 least significant bits) of the backplane connection memory will be transferred to the STio pins.

13.0 Local Connection Memory

The local connection memory controls the local interface switching configuration. Local connection memory is split into a high and a low part. Locations in the local connection memory are associated with particular STo output streams.

The LTM2 - 0 bits of each local connection memory low allows the per-channel selection for the message or the connection mode, the constant or the variable delay mode, the high impedance control of the STo driver or the bit error test enable. See Table 29 on page 65 for the content per-channel control function.

In the switching mode, the contents of the local connection memory low stream address bits (LSAB4-0) and the channel address bits (LCAB7-0) of the local connection memory defines the source information (stream and