Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MT90870

Flexible 12 k Digital Switch (F12kDX)

Data Sheet

December 2010

Features

- 12,288-channel x 12,288-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 48 stream inputs and 48 stream outputs
- 8,192-channel x 4,096-channel blocking Backplane to Local stream switch
- 4,096-channel x 8,192-channel non-blocking Local to Backplane stream switch
- 8,192-channel x 8,192-channel non-blocking Backplane input to Backplane output switch
- 4,096-channel x 4,096-channel non-blocking Local input to Local output stream switch
- Rate conversion on all data paths, Backplane to Local, Local to Backplane, Backplane to Backplane and Local to Local streams
- Backplane port accepts 32 ST-BUS streams with data rates of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s in any combination, or a fixed allocation of 16 streams at 32.768 Mb/s
- Local port accepts 16 ST-BUS streams with data rates of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination
- Per-stream channel and bit delay for Local input streams
- Per-stream channel and bit delay for Backplane input streams
- Per-stream advancement for Local output streams
- Per-stream advancement for Backplane output streams

Ordering Information

MT90870AG	272 Ball PBGA	Trays
MT90870AG2	272 Ball PBGA*	Trays

*Pb Free Tin/Silver/Copper

-40 to +85°C

***Note**: the package thickness is different than the MT90870AG (see drawing at the end of the data sheet).

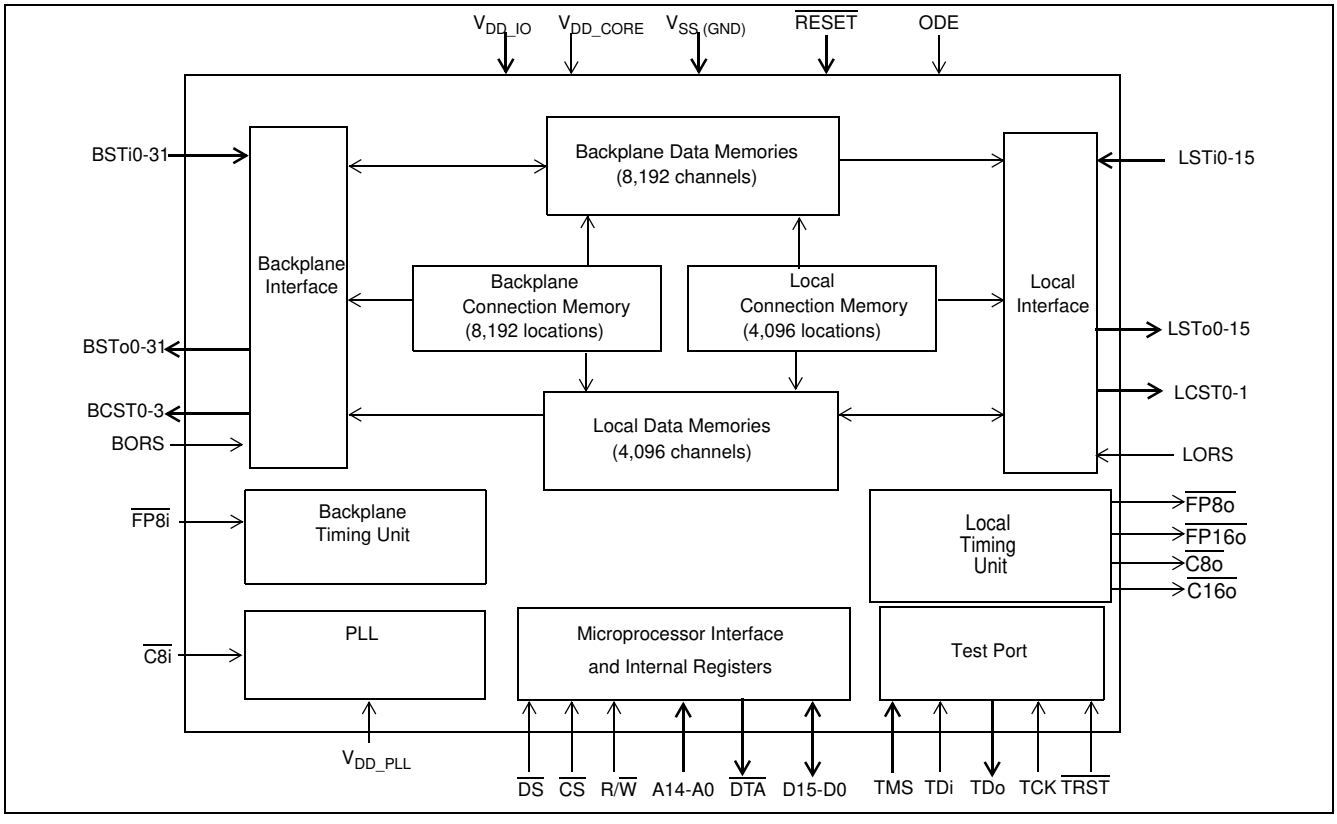

Figure 1 - MT90870 Functional Block Diagram

- Constant throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for Local and Backplane streams
- High impedance-control outputs for external drivers on Backplane and Local port
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- Automatic selection between ST-BUS and GCI-BUS operation
- Non-multiplexed Motorola microprocessor interface
- BER testing for Local and Backplane ports
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor registers
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os
- Per streams subrate switching at 4 bit, 2 bit and 1 bit depending on stream data rate

Applications

- Central Office Switches (Class 5)
- Mediation Switches
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The MT90870 has two data ports, the Backplane and the Local port. The Backplane port has two modes of operation, either 32 input and 32 output streams operated at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination, or 16 input and 16 output streams operated at 32.768 Mb/s. The Local port has 16 input and 16 output streams operated at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination.

The MT90870 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Backplane-to-Local, supporting 8 K x 4 K data switching,
- Local-to-Backplane, supporting 4 K x 8 K data switching,
- Backplane-to-Backplane, supporting 8 K x 8 K data switching.
- Local-to-Local, supporting 4 K x 4 K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode the contents of the connection memory defines, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{FP8i}$) and master clock ($\overline{C8i}$) to define the frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-BUS style frame pulse is being used. There is a two frame delay from the time $\overline{RESET}$ is de-asserted to the establishment of full switch functionality. During this period the frame format is determined before switching begins. The device provides $\overline{FP8o}$, $\overline{FP16o}$, $\overline{C8o}$ and $\overline{C16o}$ outputs to support external devices connected to the Local port.

Subrate switching is accomplished by oversampling (i.e., 1 bit switching can be accomplished by sampling a 2 Mb/s stream at 16 Mbps). Refer to MSAN-175.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The MT90870 is manufactured in a 27 mm x 27 mm body, 1.27 mm ball-pitch, 272-PBGA to JEDEC standard MS-034 BAL-2 Iss. A.

Table of Contents

Table of Contents

List of Figures

List of Tables

List of Tables

Changes Summary

The following table captures the changes from the November 2005 issue.

Page	Item	Change
85	Package Drawing	Changed package Bill of Material with a thinner substrate thickness.

The following table captures the changes from the December 2002 issue.

Page	Item	Change
14	**Pin Description**, $\overline{C8i}$	The internal frame boundary alignment description is changed from the clock rising or falling edge to rising edge only. Also added description to specify setting the C8IPOL bit in the Control Register to one for clock rising edge alignment operation.
21	Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates	Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge.
23	Figure 7, Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates	Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge.
23	Section 2.3. Backplane Frame Pulse Input and Master Input Clock Timing	Removed the falling clock edge frame boundary alignment option.
24	Figure 8, Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s	Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge.
25	Figure 9, Backplane and Local Input Channel Delay Timing Diagram (8 Mb/s)	Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively and showing rising C8i frame boundary active edge.
26	Figure 10, Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16 Mb/s	Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively and showing rising C8i frame boundary active edge.
27	Figure 11, Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 8 Mb/s	Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively.
52	Section 13.1. Control Register (CR) Bit 6, C8IPOL	Changed description to specify Bit 6, C8IPOL must be set high for rising clock edge frame boundary alignment operation.
53	Figure 18, Frame Boundary Conditions, ST- BUS Operation	Removed waveforms showing $\overline{C8i}$ falling edge frame boundary option.
54	Figure 19, Frame Boundary Conditions, GCI - BUS Operation	Removed waveforms showing $\overline{C8i}$ falling edge frame boundary option.

Page	Item	Change
73	**Backplane and Local Clock Timing**: Item 2, Backplane Frame Pulse Setup Time before C8i clock falling edge Item 3, Backplane Frame Pulse Hold Time from C8i clock falling edge	Item 2, Backplane Frame Pulse Setup Time before C8i clock falling edge changed to Backplane Frame Pulse Setup Time before C8i clock rising edge. Item 3, Backplane Frame Pulse Hold Time from C8i clock falling edge changed to Backplane Frame Pulse Hold Time from C8i clock rising edge.
75	Figure 20, Backplane and Local Clock Timing Diagram for ST-BUS	Changed C8i frame boundary active edge from falling to rising edge.
78	Figure 22, ST-BUS Backplane Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)	Changed C8i frame boundary active edge from falling to rising edge.
79	Figure 23, ST-BUS Backplane Data Timing Diagram (32 Mb/s, 16 Mb/s)	Changed C8i frame boundary active edge from falling to rising edge.
82	Figure 26, ST-BUS Local Timing Diagram (16 Mb/s)	Changed C8i frame boundary active edge from falling to rising edge.
82	Figure 27, ST-BUS Local Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)	Changed FPo and C8o to FPi and C8i respectively and shows rising C8i frame boundary active edge.

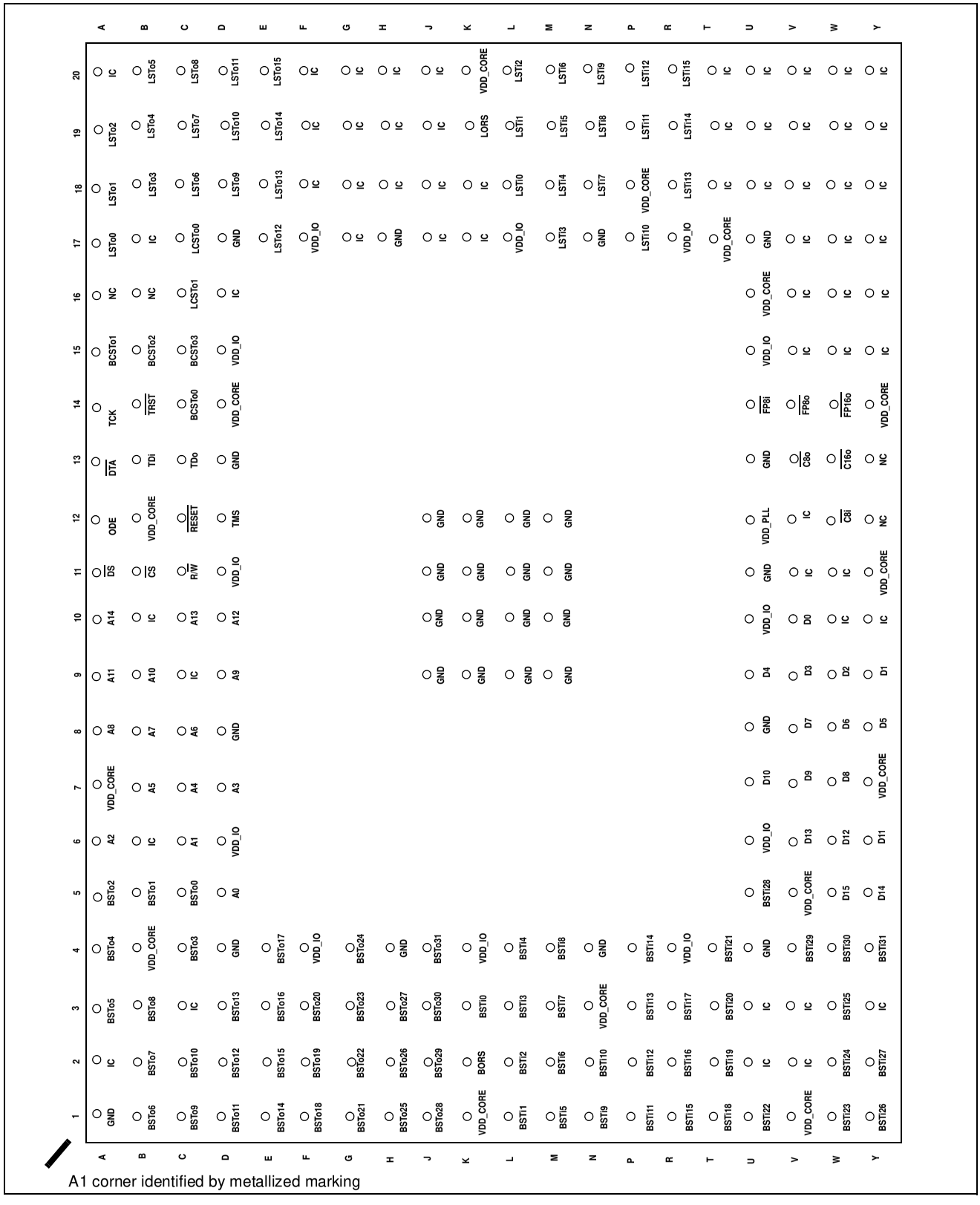

Figure 2 - MT90870 PBGA Connections (272 PBGA) Pin Diagram

(as viewed through top of package)

Pin Description

Name	Package Coordinates	Description
V_{DD_IO}	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	**Power Supply for Periphery Circuits: +3.3 V**
V_{DD_CORE}	A7, B4, B12, D14, K1, K20, N3, P18, T17, U16, V1, V5, Y7, Y11, Y14	**Power Supply for Core Logic Circuits: +1.8 V**
V_{DD_PLL}	U12	**Power Supply for Analog PLL: +1.8 V**
$V_{SS\ (GND)}$	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U11, U13, U17	**Ground**
BSTi0 - 15	K3, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, P1, P2, P3, P4, R1	**Backplane Serial Input Streams 0 to 15 (5 V Tolerant, Internal pull-down).** In Non-32 Mb/s Mode, these pins accept serial TDM data streams at a data-rate of: 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each input stream. In 32 Mb/s Mode, these pins accept serial TDM data streams at a fixed data-rate of 32.768 Mb/s (with 512 channels per stream).
BSTi16 - 31	R2, R3, T1, T2, T3, T4, U1,W1, W2, W3, Y1, Y2, U5, V4, W4, Y4	**Backplane Serial Input Streams 16 to 31 (5 V Tolerant, Internal pull-down).** In Non-32 Mb/s Mode, these pins accept serial TDM data streams at a data-rate of: 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each input stream. In 32 Mb/s Mode, these pins are unused and should be externally connected to a defined logic level.

Pin Description (continued)

Name	Package Coordinates	Description
BSTo0 - 15	C5, B5, A5 C4, A4, A3, B1, B2, B3, C1, C2, D1, D2, D3, E1, E2	**Backplane Serial Output Streams 0 to 15 (5 V Tolerant, Three-state Outputs).** In Non-32 Mb/s Mode, these pins output serial TDM data streams at a data-rate of: 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each output stream. In 32 Mb/s Mode, these pins output serial TDM data streams at a fixed data-rate of 32.768 Mb/s (with 512 channels per stream). Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state.
BSTo16 - 31	E3, E4, F1, F2, F3, G1, G2, G3, G4, H1, H2, H3, J1, J2, J3, J4	**Backplane Serial Output Streams 16 to 31 (5 V Tolerant Three-state Outputs).** In Non-32 Mb/s Mode, these pins output serial TDM data streams at a data-rate of: 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each output stream. These pins are unused when the 32 Mb/s Mode is selected. Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state.

Pin Description (continued)

Name	Package Coordinates	Description
BCSTo0-3	C14, A15, B15, C15	**Backplane Output Channel High Impedance Control (5 V Tolerant Three-state Outputs).** Active high output enable which may be used to control external buffering individually for a set of Backplane output streams on a per channel basis. In non-32 Mb/s mode (stream rates 2 Mb/s to 16 Mb/s): BCSTo0 is the output enable for BSTo[0,4,8,12,16,20,24,28], BCSTo1 is the output enable for BSTo[1,5,9,13,17,21,25,29], BCSTo2 is the output enable for BSTo[2,6,10,14,18,22,26,30], BCSTo3 is the output enable for BSTo[3,7,11,15,19,23,27,31]. In 32 Mb/s mode (stream rate 32 Mb/s): BCSTo0 is the output enable for BSTo[0,4,8,12], BCSTo1 is the output enable for BSTo[1,5,9,13], BCSTo2 is the output enable for BSTo[2,6,10,14], BCSTo3 is the output enable for BSTo[3,7,11,15]. Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state.
$\overline{\text{FP8i}}$	U14	**Frame Pulse Input (5 V Tolerant).** This pin accepts the Frame Pulse signal. The pulse width may be active for 122 ns or 244 ns at the frame boundary and the Frame Pulse Width bit (FPW) of the Control Register must be set Low (default) for a 122 ns and set High for a the 244 ns pulse condition.The device will automatically detect whether an ST-BUS or GCI-BUS style frame pulse is applied.
$\overline{\text{C8i}}$	W12	**Master Clock Input (5 V Tolerant).** This pin accepts a 8.192 MHz clock. The internal Frame Boundary is aligned with the rising edge of this clock. This rising edge frame boundary alignment is controlled by the C8IPOL bit in the Control Register as shown in Table 16 on page 52. The C8IPOL bit MUST be set to ONE for the rising edge frame boundary to be detected correctly. Falling $\overline{\text{C8i}}$ edge frame boundary alignment is not supported and should not be used.
$\overline{\text{CS}}$	B11	**Chip Select (5 V Tolerant).** Active low input used by the microprocessor to enable the microprocessor port access. This input is internally set low during a device $\overline{\text{RESET}}$.
$\overline{\text{DS}}$	A11	**Data Strobe (5 V Tolerant).** This active low input works in conjunction with $\overline{\text{CS}}$ to enable the microprocessor port read and write operations.
R/$\overline{\text{W}}$	C11	**Read/Write (5 V Tolerant).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
A0 - A14	D5, C6, A6, D7, C7, B7, C8, B8, A8, D9, B9, A9, D10, C10, A10	**Address 0 - 14 (5 V Tolerant).** These pins form the 15-bit address bus to the internal memories and registers. (Address A0 = LSB).

Pin Description (continued)

Name	Package Coordinates	Description
D0 - D15	V10, Y9, W9, V9, U9, Y8, W8, V8, W7, V7, U7, Y6, W6, V6, Y5, W5	**Data Bus 0 - 15 (5 V Tolerant).** These pins form the 16-bit data bus of the microprocessor port. (Data D0 = LSB).
$\overline{\text{DTA}}$	A13	**Data Transfer Acknowledgment (5 V Tolerant).** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. (Max. I_{OL} = 10mA).
TMS	D12	**Test Mode Select (5 V Tolerant with internal pull-up).** JTAG signal that controls the state transitions of the TAP controller.
TCK	A14	**Test Clock (5 V Tolerant).** Provides the clock to the JTAG test logic.
TDi	B13	**Test Serial Data In (5 V Tolerant with internal pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	C13	**Test Serial Data Out (5 V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
$\overline{\text{TRST}}$	B14	**Test Reset (5 V Tolerant with internal pull-up)** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. To be pulsed low during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
$\overline{\text{RESET}}$	C12	**Device Reset (5 V Tolerant with internal pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0 - 15 and BSTo0 - 31 are set to a high or high impedance depending on the state of the LORS and BORS external control pins, respectively. It clears the device registers and internal counters. This pin must stay low for more than 2 cycles of input clock $\overline{\text{C8i}}$ for the reset to be invoked.
LSTi0-15	L18, L19, L20, M17, M18, M19, M20, N18, N19, N20, P17, P19, P20, R18, R19, R20,	**Local Serial Input Streams 0 to 15 (5 V Tolerant with internal pull-down).** These pins accept serial TDM data streams at a data-rate of: 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each input stream.
$\overline{\text{C16o}}$	W13	**$\overline{\text{C16o}}$ Output Clock (Three-state Output).** A 16.384 MHz clock output. The clock falling edge or rising edge is aligned with the Local frame boundary, this is controlled by the COPOL bit of the Control Register.
$\overline{\text{C8o}}$	V13	**$\overline{\text{C8o}}$ Output Clock (Three-state Output).** A 8.192 MHz clock output. The clock falling edge or rising edge is aligned with the Local frame boundary, this is controlled by the COPOL bit of the Control Register.

Pin Description (continued)

Name	Package Coordinates	Description
$\overline{\text{FP16o}}$	W14	**Frame Pulse Output (Three-state Output).** Frame pulse output is active for 61 ns at the frame boundary. The frame pulse, running at a 8 KHz rate, will be the same format (ST-BUS or GCI-BUS) as the input frame pulse ($\overline{\text{FP8i}}$).
$\overline{\text{FP8o}}$	V14	**Frame Pulse Output (Three-state Output).** Frame pulse output is active for 122 ns at the frame boundary. The frame pulse, running at 8 KHz rate, will be the same style (ST-BUS or GCI-BUS) as the input frame pulse ($\overline{\text{FP8i}}$).
LSTo0 - 15	A17, A18, A19, B18, B19, B20, C18, C19, C20, D18, D19, D20, E17, E18, E19, E20,	**Local Serial Output Streams 0 to 15 (5 V Tolerant Three-state Outputs).** These pins output serial TDM data streams at a data-rate of: 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each output stream. Refer to descriptions of the **LORS** and **ODE** pins for control of the output High or High-Impedance state.
LCSTo0-1	C17, C16	**Local Output Channel High Impedance Control (5 V Tolerant Three-state Outputs).** Active high output enable: used to control, on a per-channel basis, the external buffering of Local output streams. LCSTo0 is the output enable for streams: LSTo[0,2,4,6,8,10,12, and 14]. LCSTo1 is the output enable for streams: LSTo[1,3,5,7,9,11,13, and 15]. Refer to descriptions of the **LORS** and **ODE** pins for control of the output High or High-Impedance state.
ODE	A12	**Output Drive Enable (5 V Tolerant, Internal pull-up).** An asynchronous input providing Output Enable control to the BSTo0- 31, LSTo0-15, BCSTo0-3 and LCSTo0-1 outputs. When LOW, the BSTo0-31 and LSTo0- 31 outputs are driven high or high impedance (dependent on the **BORS** and **LORS** pin settings respectively) and the outputs BCSTo0-3 and LCSTo0-1 are driven low. When HIGH, the outputs BSTo0- 31, LSTo0-15, BCSTo0-3 and LCSTo0-1 are enabled.

Pin Description (continued)

Name	Package Coordinates	Description
BORS	K2	**Backplane Output Reset State (5 V Tolerant, Internal pull-down).** When this input is LOW the device will initialize with the BSTo0-31 outputs driven high, and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs BCSTo0-3. When this input is HIGH, the device will initialize with the BSTo0-31 outputs at high impedance and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin, or on a per-channel basis with the **BE** bit of the Backplane Connection Memory.
LORS	K19	**Local Output Reset State (5 V Tolerant, Internal pull-down).** When this input is LOW, the device will initialize with the LSTo0-15 outputs driven high and the LCSTo0-1 outputs driven low. Following initialization, the Local stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by the LCSTo0-1 outputs. When this input is HIGH, the device will initialize with the LSTo0-15 outputs at high impedance and the LCSTo0-1 outputs driven low. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin, or on a per-channel basis with the **LE** bit of the Local Connection Memory.
NC	A16, B16, Y12, Y13	No Connect. No connection to be made.
IC	A2, A20, B6, B10, B17, C3, C9, D16, U2, U3, V2, V3, V11, V12, V15, V16, W10, W11, W15, W16, W17, W20, Y3, Y10, Y15, Y16, T18, T19, T20, U18, U19, U20, V17, V18, V19, V20, W18, W19, Y20, Y17, Y18, Y19, F18, F19, F20, G17, G18, G19, G20, H18, H19, H20, J17, J18, J19, J20, K17, K18	Internal Connects These inputs MUST be held LOW.

1.0 Bidirectional and Unidirectional Applications

The MT90870 has a maximum capacity of 12,288 input channels and 12,288 output channels. This is calculated from the maximum number of streams and channels: 48 input streams (32 Backplane, 16 Local) at 16.384 Mb/s and 48 output streams (32 Backplane, 16 Local) at 16.384 Mb/s.

One typical mode of operation is to separate the Backplane and Local sides, as shown in Figure 3 below.

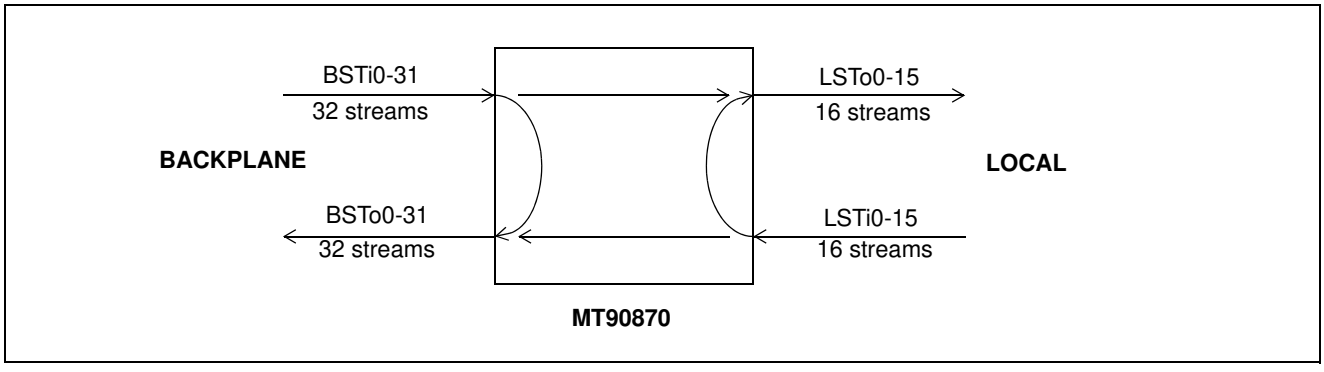

Figure 3 - 8,192 x 4,096 Channels (16 Mb/s), Bidirectional Switching

In this system setup, the chip has a capacity of 8,192 input channels and 8,192 output channels on the Backplane side as well as 4,096 input channels and 4,096 output channels on the Local side. Note that some of the output channels on one side can come from the other side, i.e., Backplane input to Local output switching.

Often a system design does not need to differentiate between Backplane and Local side, and merely needs maximum switching capacity. In this case, the MT90870 can be used as shown in Figure 4 to give the full 12,288 x 12,288 channel capacity.

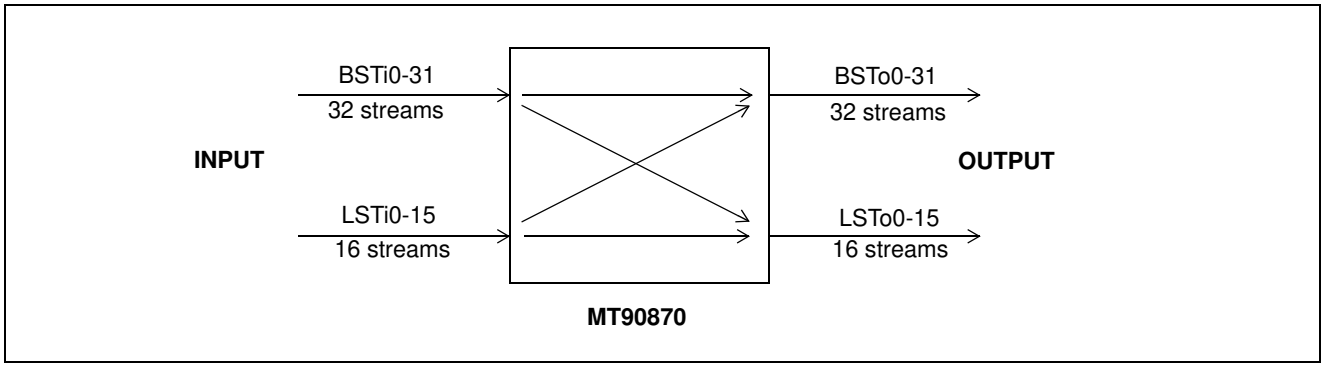

Figure 4 - 12,288 x 12,288 Channels (16 Mb/s), Unidirectional Switching

In this system, the Backplane and Local inputs and outputs are combined and the switch appears as a 48 stream input by 48 stream output switch. This style of operation is similar to older switch designs, such as the MT90826.

Note, in either configuration the Backplane may be operated in the 32 Mb/s Mode, providing 512 channels on each of the 16 available input and output streams (BSTi0-15 and BSTo0-15) operating at a data-rate of 32.768 Mb/s, in conjunction with the Local streams (LSTi0-15 and LSTo0-15) operated at 16.384 Mb/s. This allows data-rate conversion between 32.768 Mb/s and 16.384 Mb/s without loss to the switching capacity.

1.1 Flexible Configuration

The F12KDX can be configured as an 8 K by 4 K blocking bi-directional digital switch, a 12 K by 12 K unidirectional non-blocking digital switch, and as a non-blocking switch with various switching capacities.

A. Blocking Bi-directional Configuration (Typical System Configuration)

- 8,192-channel x 4,096-channel blocking switching from backplane to local streams
- 4,096-channel x 8,192-channel blocking switching from local to backplane streams
- 8,192-channel x 8,192-channel non-blocking switching from backplane input to backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from local input to local output streams

B. Unidirectional Configuration

Because the input and output drivers are synchronous, the user can combine input backplane streams and input local streams or output backplane streams and output local streams to increase the total number of input and output streams of the switch in a unidirectional configuration.

- 12,288-channel x 12,288-channel non-blocking switching from input to output streams

C. Non-Blocking Configuration

The F12KDX can be configured as a non-blocking switch if it is an application requirement. For example, it can be configured as a 6 K by 6 K non-blocking switch:

- 6,144-channel x 6,144-channel non-blocking switching from "backplane" to "local" streams
- 6,144-channel x 6,144-channel non-blocking switching from "local" to "backplane" streams
- 6,144-channel x 6,144-channel non-blocking switching from "backplane" input to "backplane" output streams
- 6,144-channel x 6,144-channel non-blocking switching from local input to local output streams

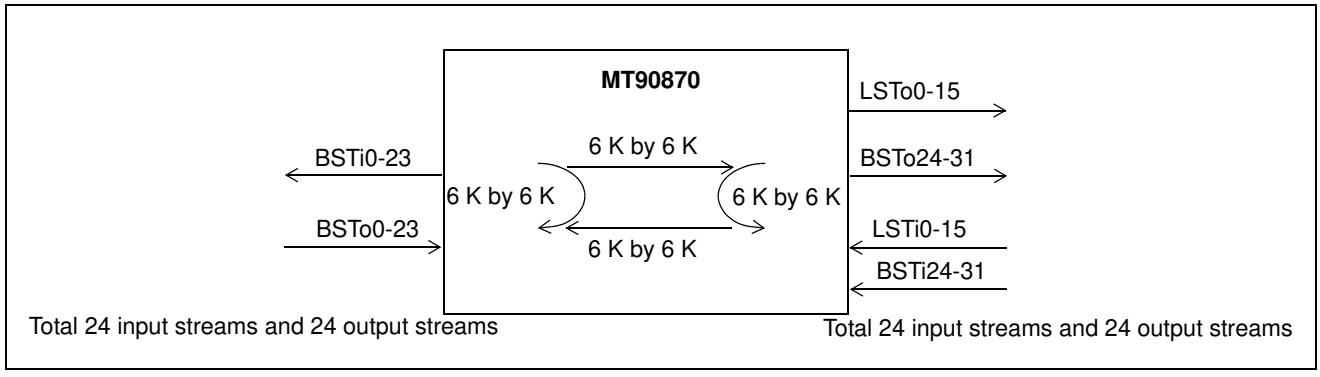

Figure 5 - 6 K x 6 K Non-Blocking Configuration

2.0 Functional Description

2.1 Switching Configurations

The device supports five switching configurations. (1) Backplane-to-Local, (2) Local-to-Backplane, (3) Backplane-to-Backplane, (4) Local-to-Local, and (5) Uni-directional switch. The following sections describe the switching paths. The switch paths of Configurations (1) to (4) may be operated simultaneously and in all 5 cases the Backplane streams may be operated at a fixed data-rate of 32.768 Mb/s on 16 input and 16 output streams, or optionally, at 16.384 Mb/s or lower data-rates on 32 input and 32 output streams. The Local streams (16 input and 16 output) may be operated at 16.384 Mb/s or lower data-rates. When the lower data-rates of 8.192, 4.096, and

2.048 Mb/s are included, there will be a corresponding reduction in switch capacity although conversion between differing rates will be maintained.

2.1.1 Backplane-to-Local Path

The device can provide data switching between the Backplane input port (8192 channels) and the Local output port (4096 channels). The Local Connection Memory determines the switching configurations.

2.1.2 Local-to-Backplane Path

The device can provide data switching between the Local input port (4096 channels) and the Backplane output port (8192 channels). The Backplane Connection Memory determines the switching configurations.

2.1.3 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input (8192 channels) and output (8192 channels) ports. The Backplane Connection Memory determines the switching configurations.

2.1.4 Local-to-Local Path

The device can provide data switching between the Local input (4096 channels) and output (4096 channels) ports. The Local Connection Memory determines the switching configurations.

2.1.5 Uni-directional Switch

The device may be optionally configured to provide a 12,288 x 12,288 uni-directional switch by grouping together Backplane and Local input and output streams.

2.2 Port Data Rate Modes and Selection

The selection of individual stream data-rates is summarized in Table 1.

2.2.1 Local Port Rate Selection

The Local port has 16 input (LSTi0-15) and 16 output (LSTo0-15) data streams. All input and output streams may be individually selected for operation at a data rate of either 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. The timing of the input and output clocks and frame pulses are shown in Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates.

2.2.1.1 Local Input Port

The bit rate for each input stream is selected by writing to a dedicated Local Input Bit Rate Register (LIBRR0-15). Refer to Table 41, Local Input Bit Rate Register (LIBRRn) Bits.

Stream Number	Rate Selection Capability (for each individual stream)
Input stream - Backplane 0-15 (BSTi0-15)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode 32.768 Mb/s - 32 Mb/s Mode
Input stream - Backplane 16-31 (BSTi16-31)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode Unused - 32 Mb/s Mode
Output stream - Backplane 0-15 (BSTo0-15)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode 32.768 Mb/s - 32 Mb/s Mode

Stream Number	Rate Selection Capability (for each individual stream)
Output stream - Backplane 16-31 (BSTo16-31)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode Unused - 32 Mb/s Mode
Input stream - Local 0-15 (LSTi0-15)	2.048, 4.096, 8.192 or 16.384 Mb/s
Output stream - Local 0-15 (LSTo0-15)	2.048, 4.096, 8.192 or 16.384 Mb/s

Table 1 - Per-stream Data-Rate Selection: Backplane and Local, Non-32 Mb/s Mode and 32 Mb/s Mode

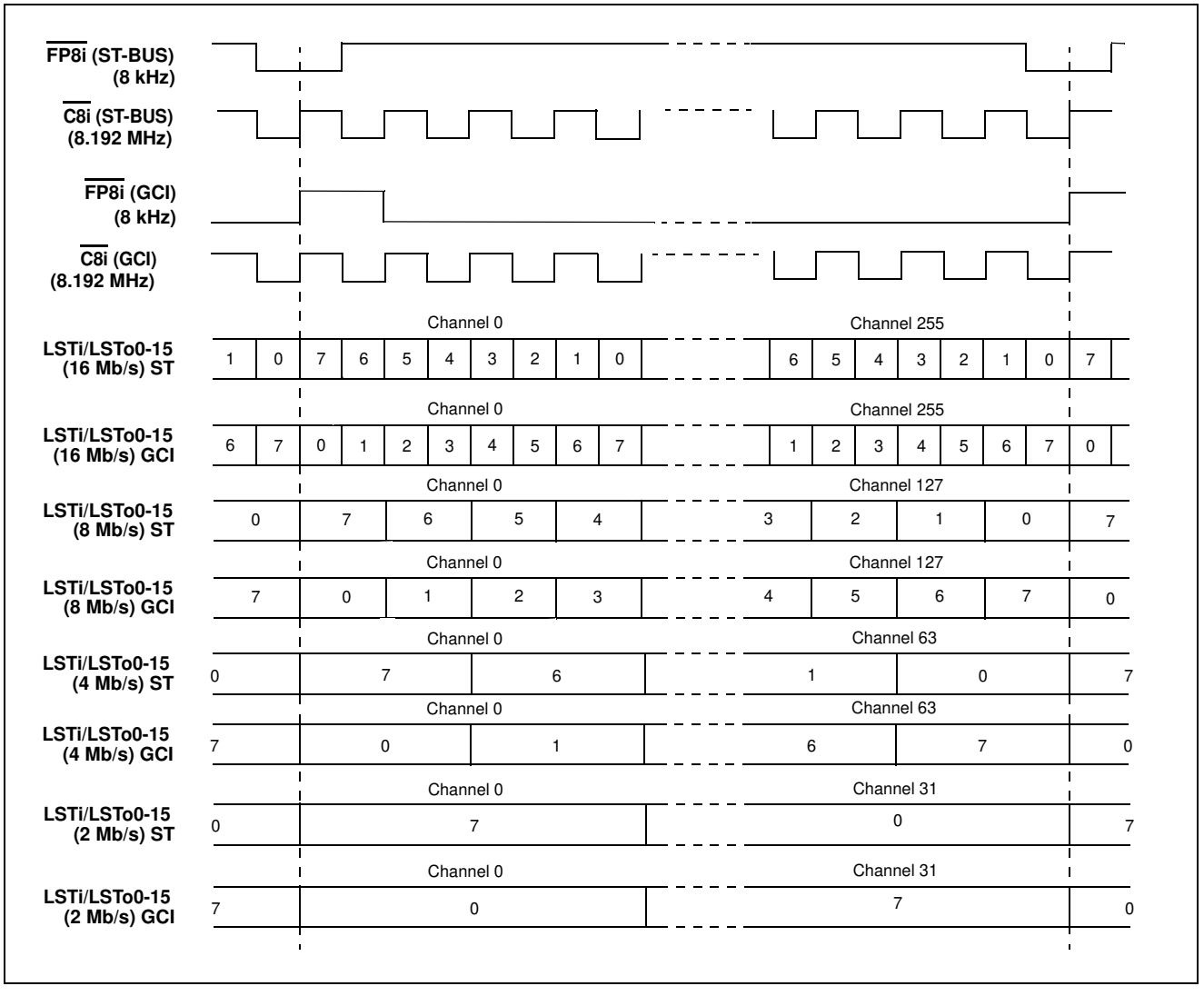

Figure 6 - Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates

2.2.1.2 Local Output Port

The bit rate for each output stream is selected by writing to a dedicated Local Output Bit Rate Register (LOBRR0-15). Refer to Table 43, Local Output Bit Rate Register (LOBRRn) Bits.

Operation of stream data in the Connection Mode or the Message Mode is determined by the state of the LMM bit, and the channel High-impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 6.1, Local Connection Memory, and Section 12.3, Local Connection Memory Bit Definition.

2.2.2 Backplane Port Rate Selection

The Backplane streams may be operated in one of two modes, namely Non-32 Mb/s Mode and 32 Mb/s Mode. The Local stream data-rates are not affected by the operating mode of the Backplane. The operating mode of the Backplane is determined by setting the Control Register bit, MODE32. Setting the bit HIGH will invoke the 32 Mb/s Mode. Setting the bit LOW will invoke the Non-32 Mb/s mode. The default bit value on device Reset is LOW. The timing of the input and output clocks and frame pulses are shown in Figure 7, Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates.

Non-32 Mb/s Mode: Each of the 32 Backplane streams (BSTi0-31 and BSTo0-31) and Local streams (LSTi0-15 and LSTo0-15) can be independently programmed for a data-rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s.

32 Mb/s Mode: 16 of the Backplane input streams (BSTi0-15) and 16 Backplane output (BSTo0-15) streams operate at a fixed rate of 32.768 Mb/s. In this mode, the upper 16 input (BSTi16-31) and 16 output (BSTi16-31) streams are unused. All 32 Local streams can be independently programmed for a data-rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s.

2.2.2.1 Backplane Input Port

The bit rate for each input stream is selected by writing to a dedicated Backplane Input Bit Rate Register (BOBRR0-31). Refer to Table 45, Backplane Input Bit Rate Register (BIBRRn) Bits. If the 32 Mb/s mode is selected by writing to the Control Register bit (MODE32), the settings in BIBRRn are ignored.

2.2.2.2 Backplane Output Port

The bit rate for each output stream is selected by writing to a dedicated Backplane Output Bit Rate Register (BOBRR0-31). Refer to Table 47, Backplane Output Bit Rate Register (BOBRRn) Bits. If the 32 Mb/s mode is selected by writing to the Control Register bit (MODE32), the settings in BOBRRn are ignored.

Operation of stream data in the Connection Mode or the Message Mode is determined by the state of the BMM bit, and the channel High-impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e., from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 6.2, Backplane Connection Memory and Section 12.4, Backplane Connection Memory Bit Definition.

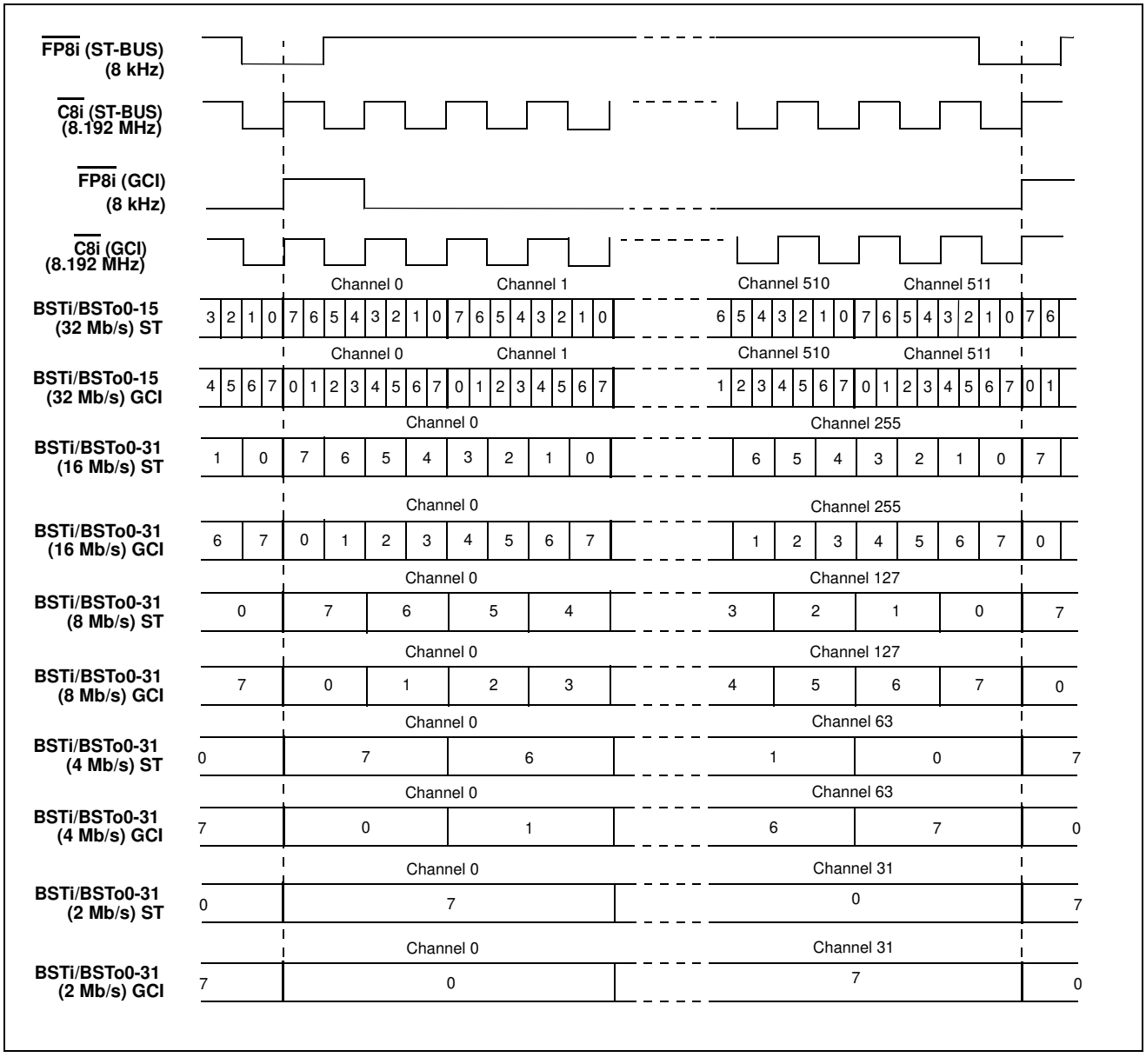

Figure 7 - Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates

2.3 Backplane Frame Pulse Input and Master Input Clock Timing

The Backplane frame pulse ($\overline{\text{FP8i}}$) is an 8 kHz input signal active for 122 ns or 244 ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Table 16, Control Register Bits, for details.

The active state and timing of $\overline{\text{FP8i}}$ may conform either to the ST-BUS or to the GCI-BUS as shown in Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates, and Figure 7, Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates. The MT90869 will automatically detect whether an ST-BUS or a GCI-BUS style frame pulse is being used for the master frame pulse ($\overline{\text{FP8i}}$). The device will detect the frame boundary alignment using the rising edge of the input clock ($\overline{\text{C8i}}$), provided the C8IPOL bit in Table 16, “Control Register Bits,” on page 52 is set to one. Before the C8IPOL bit is set to one, the frame boundary will not be detected correctly. For the

purposes of describing the device operation, the remaining part of this document assumes the ST-BUS style frame pulse with a single width frame pulse of 122 ns and the C8IPOL bit is set to one unless explicitly stated otherwise.

In addition, the device provides FP8o, FP16o, C8o and C16o outputs to support external devices which connect to the Local port. The Local frame pulses (FP8o, FP16o) will be provided in the same style as the master frame pulse (FP8i). The polarity of C8o and C16o, at the Frame Boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the external clock frequency to generate an internal clock signal operated at 131.072 MHz.

2.4 Backplane Frame Pulse Input and Local Frame Pulse Output Alignment

The MT90870 accepts a Backplane Frame Pulse (FP8i) and generates the Local Frame Pulse outputs, FP8o and FP16o, which are aligned to the master frame pulse. There is a constant three frame delay for data being switched. Figure 8, Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s, shows the backplane and local frame pulse alignment for different data rates.

For further details of Frame Pulse conditions and options see Section 13.1, Control Register (CR), Figure 18, Frame Boundary Conditions, ST- BUS Operation, and Figure 19, Frame Boundary Conditions, GCI - BUS Operation.

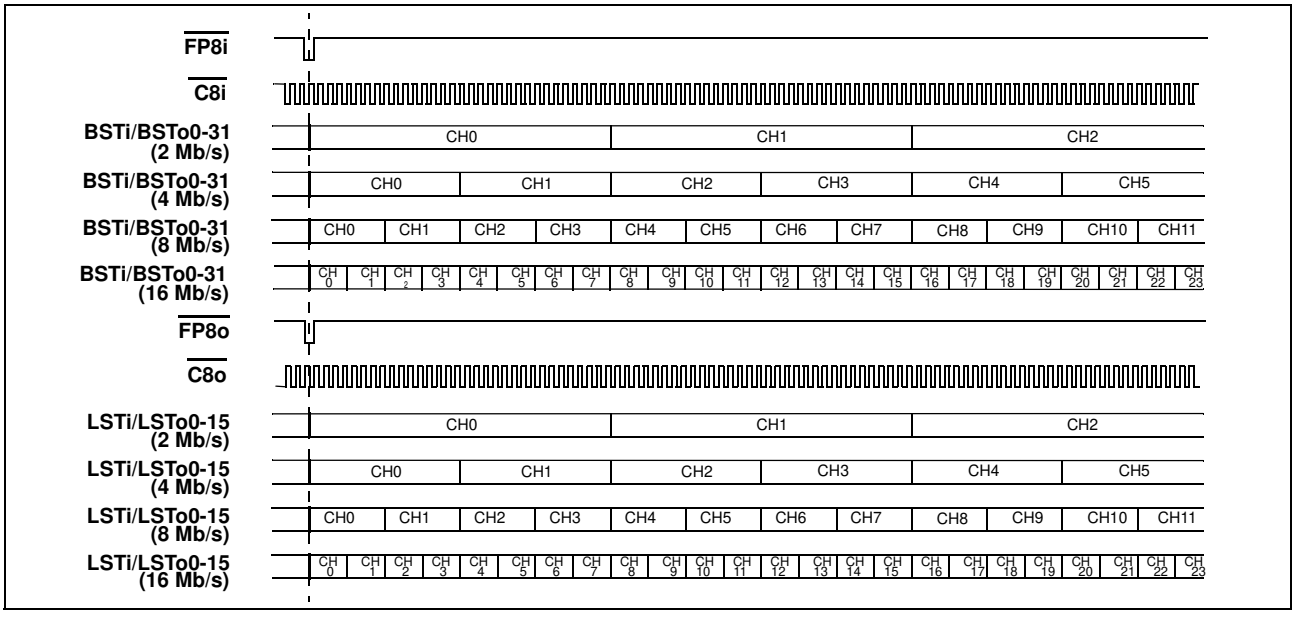

Figure 8 - Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s

3.0 Input and Output Offset Programming

3.1 Input Channel Delay Programming (Backplane and Local Input Streams)

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

The control of the Input Channel Delay and the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, FP8i. By default, all input streams have channel delay of zero such that Ch0 is the first channel that appears after the frame boundary.

By programming the Backplane or Local input channel delay registers, BCDR0-31 and LCDR0-15, users can assign the Ch0 position to be located at any one of the channel boundaries in a frame. See Figure 9.

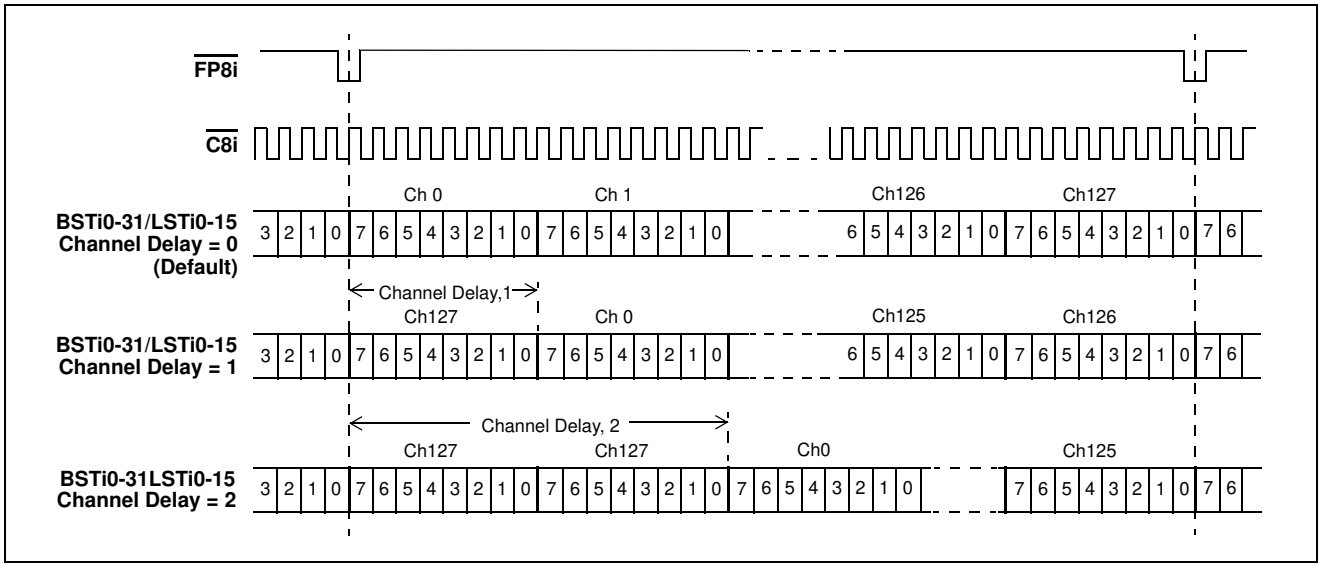

Figure 9 - Backplane and Local Input Channel Delay Timing Diagram (8 Mb/s)

For delays within channel boundaries, the input bit delay programming can be used. The use of Input Channel Delay in combination with Input Bit Delay enables the Ch0 position to be placed anywhere within a frame to a resolution of 1/4 of the bit period.

3.2 Input Bit Delay Programming (Backplane and Local Input Streams)

In addition to the Input Channel Delay programming, the Input Bit Delay programming feature provides users with greater flexibility when designing switch matrices for high speed operation. The input bit delay may be programmed on a per-stream basis to accommodate delays created on PCM highways. For all streams the delay is up to 7 3/4 bits with a resolution of 1/4 bit, for the selected data-rate.

See Figure 10 and Figure 11 for Input Bit Delay Timing at 16 Mb/s and 8 Mb/s data rates, respectively.

The Local input delay is defined by the Local Input Delay registers, LIDR0 to LIDR15, corresponding to the Local data streams, LSTi0 to LSTi15, and the Backplane input delay is defined by the Backplane Input Delay registers, BIDR0 to BIDR31, which correspond to the Backplane data streams, BSTi0 to BSTi31.