Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

## Features

March 2005

- 8,192-channel x 8,192-channel non-blocking unidirectional switching. The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 32 stream inputs and 32 stream outputs.
- 4,096-channel x 4,096 channel non-blocking Backplane to Local stream switch
- 4,096-channel x 4,096 channel non-blocking Local to Backplane stream switch
- 4,096-channel x 4,096 channel non-blocking Backplane input to Backplane output switch
- 4,096-channel x 4,096 channel non-blocking Local input to Local output stream switch
- Rate conversion on all data paths, Backplane to Local, Local to Backplane, Backplane to Backplane and Local to Local streams
- Backplane port accepts 16 ST-BUS streams with data rates of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s in any combination

**Ordering Information**

MT90871AV 196 Ball LBGA

**-40C to +85C**

- Local port accepts 16 ST-BUS streams with data rates of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination
- Per-stream channel and bit delay for Local input streams
- Per-stream channel and bit delay for Backplane input streams
- Per-stream advancement for Local output streams
- Per-stream advancement for Backplane output streams
- Constant throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for Local and Backplane streams

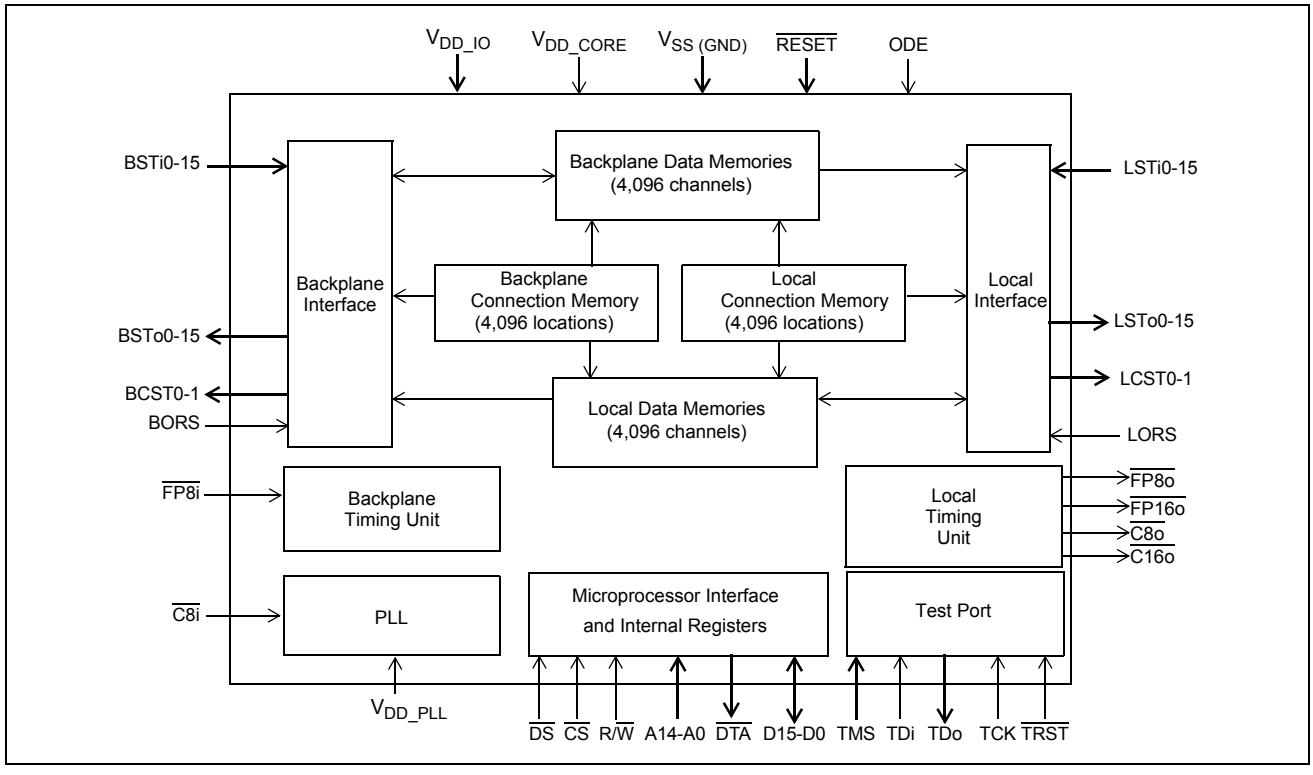


**Figure 1 - MT90871 Functional Block Diagram**

- High impedance-control outputs for external drivers on Backplane and Local port
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- Automatic selection between ST-BUS and GCI-BUS operation
- Non-multiplexed Motorola microprocessor interface
- BER testing for Local and Backplane ports
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor registers
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os
- Per stream subrate switching at 4-bit, 2-bit, 1-bit depending on stream data rate

## Applications

- Central Office Switches (Class 5)
- Mediation Switches
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

## Device Overview

The MT90871 has two data ports, the Backplane and the Local port. The Backplane port has 16 input and 16 output streams operated at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination and the Local port has 16 input and 16 output streams operated at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination.

The MT90871 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Backplane-to-Local, supporting 4 K x 4 K data switching,
- Local-to-Backplane, supporting 4 K x 4 K data switching,
- Backplane-to-Backplane, supporting 4 K x 4 K data switching.
- Local-to-Local, supporting 4 K x 4 K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode the contents of the connection memory defines, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{FP8i}$) and master clock ($\overline{C8i}$) to define the frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-BUS style frame pulse is being used. There is a two frame delay from the time $\overline{RESET}$ is de-asserted to the establishment of full switch functionality. During this period the frame format is determined before switching begins. The device provides $\overline{FP8o}$, $\overline{FP16o}$, $\overline{C8o}$ and $\overline{C16o}$ outputs to support external devices connected to the Local port.

Subrate switching can be accomplished by over-sampling (i.e. 1-bit switching can be achieved by sampling a 2 Mbps stream at 16 Mbps). Refer to MSAN-175.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The MT90871 is manufactured in a 15mm x 15mm body, 1.0mm ball-pitch, 196-LBGA to JEDEC standard MS-034 BAL-2 Iss. A.

# Table of Contents

# Table of Contents

# List of Figures

# List of Tables

**Changes Summary**

The following table captures the changes from the December 2002 issue.

| Page | Item | Change |
|---|---|---|
| 5 | Pin Description Table, $\overline{C8i}$ | The internal frame boundary alignment description is changed from the clock rising or falling edge to rising edge only. Also added description to specify setting the C8IPOL bit in the Control Register to one for clock rising edge alignment operation. |
| 11 | Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s Stream Rates | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 12 | Figure 7, Backplane Port Timing Diagram for 2, 4, 8, and 16 Mb/s stream rates | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 13 | Section 2.3. Backplane Frame Pulse Input and Master Input Clock Timing | Removed the falling clock edge frame boundary alignment option. |
| 13 | Figure 8, Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 14 | Figure 9, Backplane and Local Input Channel Delay Timing Diagram (8 Mb/s) | Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively and showing rising C8i frame boundary active edge. |
| 15 | Figure 10, Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16 Mb/s | Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively and showing rising C8i frame boundary active edge. |
| 35 | Section 13.1. Control Register (CR) Bit 6, C8IPOL | Changed description to specify Bit 6, C8IPOL must be set high for rising clock edge frame boundary alignment operation. |
| 16 | Figure 11, Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 8 Mb/s | Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively. |
| 37 | Figure 17, Frame Boundary Conditions, ST- BUS Operation | Removed waveforms showing $\overline{C8i}$ falling edge frame boundary option. |
| 37 | Figure 18, Frame Boundary Conditions, GCI - BUS Operation | Removed waveforms showing $\overline{C8i}$ falling edge frame boundary option. |
| 56 | Backplane and Local Clock Timing:<br>Item 2, Backplane Frame Pulse Setup Time before C8i clock falling edge<br>Item 3, Backplane Frame Pulse Hold Time from $\overline{C8i}$ clock falling edge | Item 2, Backplane Frame Pulse Setup Time before C8i clock falling edge changed to Backplane Frame Pulse Setup Time before $\overline{C8i}$ clock rising edge.<br>Item 3, Backplane Frame Pulse Hold Time from C8i clock falling edge changed to Backplane Frame Pulse Hold Time from C8i clock rising edge. |

| Page | Item | Change |
|---|---|---|
| 57 | Figure 19, Backplane and Local Clock Timing Diagram for ST-BUS | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 59 | Figure 21, ST-BUS Backplane Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s) | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 60 | Figure 22, ST-BUS Backplane Data Timing Diagram (16 Mb/s) | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 63 | Figure 25, ST-BUS Local Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s) | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |
| 63 | Figure 26, ST-BUS Local Data Timing Diagram (16 Mb/s) | Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge. |

A1 corner identified by metallized marking, mold indent, ink dot or right-angled corner

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | BSTo1 | BSTo2 | A4 | A5 | A8 | A9 | A12 | A13 | R/W | CS | TMS | TDo | BCSTo0 | TRST |
| B | A0 | BSTo5 | BSTo0 | A1 | A2 | A7 | A11 | A14 | ODE | TDi | TCK | LCSTo1 | LSTo0 | LSTo1 |
| C | IC | BSTo7 | BSTo8 | BSTo3 | BSTo4 | A6 | A10 | DS | RESET | BCSTo1 | IC | LCSTo0 | IC | LSTo3 |
| D | IC | BSTo6 | BSTo10 | GND | A3 | VDD_IO | VDD_IO | VDD_IO | DTA | VDD_IO | GND | LSTo4 | LSTo6 | LSTo2 |
| E | BSTo12 | BSTo11 | BSTo13 | VDD_IO | GND | VDD_CORE | VDD_CORE | VDD_CORE | VDD_CORE | GND | VDD_IO | LSTo8 | LSTo7 | LSTo5 |
| F | BSTo9 | BSTo14 | BSTo15 | VDD_IO | VDD_CORE | GND | GND | GND | GND | VDD_CORE | VDD_IO | LSTo12 | LSTo13 | LSTo9 |
| G | BSTi0 | BORS | VDD_CORE | VDD_IO | VDD_CORE | GND | GND | GND | GND | VDD_CORE | VDD_IO | LSTo11 | LSTo15 | LSTo10 |
| H | BSTi1 | BSTi2 | BSTi3 | VDD_IO | VDD_CORE | GND | GND | GND | GND | VDD_CORE | VDD_IO | VDD_CORE | LORS | LSTo14 |
| J | BSTi4 | BSTi5 | BSTi7 | VDD_IO | VDD_CORE | GND | GND | GND | GND | VDD_CORE | VDD_IO | LSTi5 | LSTi1 | LSTi2 |
| K | BSTi6 | BSTi9 | BSTi13 | VDD_IO | GND | VDD_CORE | VDD_CORE | VDD_CORE | VDD_CORE | GND | VDD_IO | LSTi15 | LSTi3 | LSTi0 |
| L | BSTi8 | BSTi11 | BSTi14 | GND | VDD_IO | VDD_IO | VDD_IO | VDD_IO | VDD_IO | VDD_IO | GND | LSTi14 | LSTi8 | LSTi6 |
| M | BSTi10 | BSTi15 | D15 | D14 | D12 | D5 | IC | IC | C16o | FP8i | LSTi13 | LSTi10 | LSTi7 | LSTi4 |
| N | BSTi12 | D13 | D10 | D11 | D7 | D3 | D0 | IC | VDD_PLL | C8o | FP8o | LSTi11 | LSTi12 | LSTi9 |
| P | GND | D9 | D8 | D6 | D4 | D2 | D1 | IC | NC | C8i | NC | FP16o | GND | GND |

**Figure 2 - MT90871 LBGA Connections (196 LBGA) Pin Diagram (as viewed through top of package)**

**Pin Description Table**

| Name | Package Coordinates | Description |
|---|---|---|
| $V_{DD\_IO}$ | D6, D7, D8, D10, E4, E11,F4, F11, G4, G11, H4, H11, J4, J11, K4, K11, L5, L6, L7, L8, L9, L10 | **Power Supply for Periphery Circuits:** +3.3 V |
| $V_{DD\_CORE}$ | E6, E7, E8, E9, F5, F10, G3, G5, G10, H5, H10, H12, J5, J10, K6, K7, K8, K9 | **Power Supply for Core Logic Circuits: +1.8 V** |
| $V_{DD\_PLL}$ | N9 | **Power Supply for Analog PLL: +1.8 V** |
| $V_{SS\ (GND)}$ | D4, D11, E5, E10, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9 K5, K10, L4, L11, P1, P13, P14 | **Ground** |
| BSTi0 - 15 | G1, H1, H2, H3, J1, J2, K1, J3, L1, K2, M1, L2, N1, K3, L3, M2 | **Backplane Serial Input Streams 0 to 7 (5 V Tolerant, Internal pull-down).** These pins accept serial TDM data streams at a data-rate of:<br>• 16.384 Mb/s (with 256 channels per stream),<br>• 8.192 Mb/s (with 128 channels per stream),<br>• 4.096 Mb/s (with 64 channels per stream), or<br>• 2.048 Mb/s (with 32 channels per stream).<br>The data-rate is independently programmable for each input stream. |
| BSTo0 - 15 | B3, A1, A2, C4, C5, B2, D2, C2, C3, F1, D3, E2, E1, E3, F2, F3 | **Backplane Serial Output Streams 0 to 7 (5 V Tolerant, Three-state Outputs).** These pins output serial TDM data streams at a data-rate of:<br>• 16.384 Mb/s (with 256 channels per stream),<br>• 8.192 Mb/s (with 128 channels per stream),<br>• 4.096 Mb/s (with 64 channels per stream), or<br>• 2.048 Mb/s (with 32 channels per stream).<br>The data-rate is independently programmable for each output stream.<br>Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state. |
| BCSTo0-1 | A13, C10 | **Backplane Output Channel High Impedance Control (5 V Tolerant Three-state Outputs).** Active high output enable which may be used to control external buffering of Backplane output streams on a per channel basis.<br>BCSTo0 is the output enable for BSTo[0, 2, 4, 6, 8, 10, 12, 14], BCSTo1 is the output enable for BSTo[1, 3, 5, 7, 9, 11, 13, 15].<br>Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state. |

**Pin Description Table (continued)**

| Name | Package Coordinates | Description |
|---|---|---|
| $\overline{FP8i}$ | M10 | **Frame Pulse Input (5 V Tolerant).** This pin accepts the Frame Pulse signal. The pulse width may be active for 122 ns or 244 ns at the frame boundary and the Frame Pulse Width bit (FPW) of the Control Register must be set Low (default) for a 122 ns and set High for a the 244 ns pulse condition.<br>The device will automatically detect whether an **ST-BUS** or **GCI-BUS** style frame pulse is applied. |
| $\overline{C8i}$ | P10 | **Master Clock Input (5 V Tolerant).** This pin accepts a 8.192 MHz clock. The internal Frame Boundary is aligned with the rising edge of this clock. This rising edge frame boundary alignment is controlled by the C8IPOL bit in the Control Register as shown in Table 13 on page 35. The C8IPOL bit MUST be set to ONE for the rising edge frame boundary to be detected correctly. Falling C8i edge frame boundary alignment is not supported and should not be used. |
| $\overline{CS}$ | A10 | **Chip Select (5 V Tolerant).** Active low input used by the microprocessor to enable the microprocessor port access. This input is internally set LOW during a device $\overline{RESET}$. |
| $\overline{DS}$ | C8 | **Data Strobe (5 V Tolerant).** This active low input is used in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. |
| R/$\overline{W}$ | A9 | **Read/Write (5 V Tolerant).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access. |
| A0 - A14 | B1, B4, B5, D5, A3, A4, C6, B6, A5, A6, C7, B7, A7, A8, B8 | **Address 0 - 14 (5 V Tolerant).** These pins form the 15-bit address bus to the internal memories and registers. (Address A0 = LSB). |
| D0 - D15 | N7, P7, P6, N6, P5, M6, P4, N5, P3, P2, N3, N4, M5, N2, M4, M3 | **Data Bus 0 - 15 (5 V Tolerant).** These pins form the 16-bit data bus of the microprocessor port. (Data D0 = LSB). |
| $\overline{DTA}$ | D9 | **Data Transfer Acknowledgment (5 V Tolerant).** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. (Max. $I_{OL}$ = 10 mA). |
| TMS | A11 | **Test Mode Select (5 V Tolerant with internal pull-up).** JTAG signal that controls the state transitions of the TAP controller. |
| TCK | B11 | **Test Clock (5 V Tolerant).** Provides the clock to the JTAG test logic. |
| TDi | B10 | **Test Serial Data In (5 V Tolerant with internal pull-up).** JTAG serial test instructions and data are shifted in on this pin. |
| TDo | A12 | **Test Serial Data Out (5 V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled. |
| $\overline{TRST}$ | A14 | **Test Reset (5 V Tolerant with internal pull-up)** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. To be pulsed low during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device. |
| $\overline{RESET}$ | C9 | **Device Reset (5 V Tolerant with internal pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0 - 15 and BSTo0 - 15 are set to a high or high impedance depending on the state of the LORS and BORS external control pins, respectively. It clears the device registers and internal counters. This pin must stay low for more than 2 cycles of input clock $\overline{C8i}$ for the reset to be invoked. |

**Pin Description Table (continued)**

| Name | Package Coordinates | Description |
|---|---|---|
| LSTi0-15 | K14, J13, J14, K13, M14, J12, L14, M13, L13, N14, M12, N12, N13, M11, L12, K12 | **Local Serial Input Streams 0 to 15 (5 V Tolerant with internal pull-down).** These pins accept serial TDM data streams at a data-rate of:<br>• 16.384 Mb/s (with 256 channels per stream),<br>• 8.192 Mb/s (with 128 channels per stream),<br>• 4.096 Mb/s (with 64 channels per stream), or<br>• 2.048 Mb/s (with 32 channels per stream).<br>The data-rate is independently programmable for each input stream. |
| $\overline{C16o}$ | M9 | **$\overline{C16o}$ Output Clock (Three-state Output).** A 16.384 MHz clock output. The clock falling edge or rising edge is aligned with the Local frame boundary, and is determined by the COPOL bit of the Control Register. |
| $\overline{C8o}$ | N10 | **$\overline{C8o}$ Output Clock (Three-state Output).** A 8.192 MHz clock output. The clock falling edge or rising edge is aligned with the Local frame boundary, and is determined by the COPOL bit of the Control Register. |
| $\overline{FP16o}$ | P12 | **Frame Pulse Output (Three-state Output).** Frame pulse output is active for 61ns at the frame boundary. The frame pulse, running at a 8 KHz rate, will be the same format (ST-BUS or GCI-BUS) as the input frame pulse (FP8i). |
| $\overline{FP8o}$ | N11 | **Frame Pulse Output (Three-state Output).** Frame pulse output is active for 122 ns at the frame boundary. The frame pulse, running at 8 KHz rate, will be the same style (ST-BUS or GCI-BUS) as the input frame pulse (FP8i). |
| LSTo0 - 15 | B13, B14, D14, C14, D12, E14, D13, E13, E12, F14, G14, G12, F12, F13, H14, G13 | **Local Serial Output Streams 0 to 15 (5 V Tolerant Three-state Outputs).** These pins output serial TDM data streams at a data-rate of:<br>• 16.384 Mb/s (with 256 channels per stream),<br>• 8.192 Mb/s (with 128 channels per stream),<br>• 4.096 Mb/s (with 64 channels per stream), or<br>• 2.048 Mb/s (with 32 channels per stream).<br>The data-rate is independently programmable for each output stream.<br>Refer to descriptions of the **LORS** and **ODE** pins for control of the output High or High-Impedance state. |
| LCSTo0-1 | C12, B12 | **Local Output Channel High Impedance Control (5 V Tolerant Three-state Outputs).**<br>Active high output enable which may be used to control external buffering individually for a set of Local output streams on a per channel basis.<br>LCSTo0 is the output enable for LSTo[0, 2, 4, 6, 8, 10, 12, 14],<br>LCSTo1 is the output enable for LSTo[1, 3, 5, 7, 9, 11, 13, 15].<br>Refer to descriptions of the **LORS** and **ODE** pins for control of the output High or High-Impedance state. |

**Pin Description Table (continued)**

| Name | Package Coordinates | Description |
|---|---|---|
| ODE | B9 | **Output Drive Enable (5 V Tolerant, Internal pull-up).** An asynchronous input providing Output Enable control to the BSTo0-15, LSTo0-15, BCSTo0-1 and LCSTo0-1 outputs.<br>When LOW, the BSTo0-15 and LSTo0-15 outputs are driven high or high impedance (dependent on the **BORS** and **LORS** pin settings respectively) and the outputs BCSTo0-1 and LCSTo0-1 are driven low.<br>When HIGH, the outputs BSTo0-15, LSTo0-15, BCSTo0-1 and LCSTo0-1 are enabled. |
| BORS | G2 | **Backplane Output Reset State (5 V Tolerant, Internal pull-down).** Asynchronous input. When LOW, the device will initialize with the BSTo0-15 outputs driven high, and the BCSTo0-1 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs BCSTo0-1.<br>When the input is HIGH, the device will initialize with the BSTo0-15 outputs at high impedance and the BCSTo0-1 outputs are driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or, on a per-channel basis, with the **BE** bit in Backplane Connection Memory. |
| LORS | H13 | **Backplane Output Reset State (5 V Tolerant, Internal pull-down).** Asynchronous input. When LOW, the device will initialize with the LSTo0-15 outputs driven high, and the LCSTo0-1 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs LCSTo0-1.<br>When the input is HIGH, the device will initialize with the LSTo0-15 outputs at high impedance and the LCSTo0-1 outputs are driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or, on a per-channel basis, with the **LE** bit in Backplane Connection Memory. |
| NC | P9, P11 | **No Connect.** These ball-pads MUST remain unconnected. |
| IC | C1, D1, C11, C13, M7, M8, N8, P8 | **Internal Connects**<br>These inputs MUST be held at logic ‘LOW’. |

## 1.0 Bidirectional and Unidirectional Applications

The MT90871 has a maximum capacity of 8,192 input channels and 8,192 output channels. This is calculated from the maximum number of streams and channels: 32 input streams (16 Backplane, 16 Local) at 16.384 Mb/s and 32 output streams (16 Backplane, 16 Local) at 16.384 Mb/s.

One typical mode of operation is to separate the Backplane and Local sides, as shown in Figure 3 below.

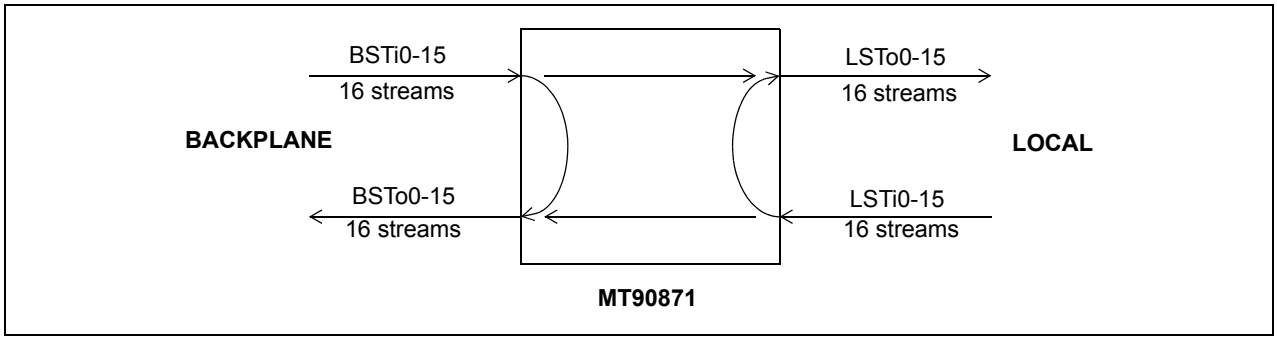


**Figure 3 - 4,096 x 4,096 Channels (16 Mb/s), Bidirectional Switching**

In this system setup, the chip has a capacity of 4,096 input channels and 4,096 output channels on the Backplane side as well as 4,096 input channels and 4,096 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, i.e. Backplane input to Local output switching.

Often a system design does not need to differentiate between Backplane and Local side, and merely needs maximum switching capacity. In this case, the MT90871 can be used as shown in Figure 4 to give the full 8,192 x 8,192 channel capacity.

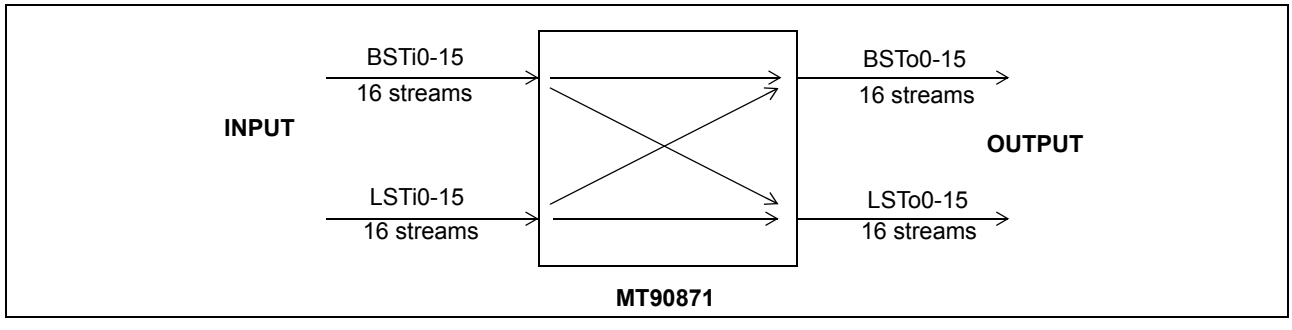


**Figure 4 - 8,192 x 8,192 Channels (16 Mb/s), Unidirectional Switching**

In this system, the Backplane and Local inputs and outputs are combined and the switch appears as a 32 stream input by 32 stream output switch. This style of operation is similar to older switch designs, such as the MT90826.

### 1.1 Flexible Configuration

The F8KDX can be configured as a 4 K by 4 K non-blocking bi-directional digital switch, an 8 K by 8 K unidirectional non-blocking switch, and as a blocking switch with various switching capacities.

#### 1.1.1 A. Blocking Bi-directional Configuration (Typical System Configuration)

- 4,096-channel x 4,096-channel non-blocking switching from backplane to local streams
- 4,096-channel x 4,096-channel non-blocking switching from local to backplane streams
- 4,096-channel x 4,096-channel non-blocking switching from backplane input to backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from local input to local output streams

### 1.1.2 Unidirectional Configuration

Because the input and output drivers are synchronous, the user can combine input backplane streams and input local streams or output backplane streams and output local streams to increase the total number of input and output streams of the switch in a unidirectional configuration.

- 8,192-channel x 8,192-channel non-blocking switching from input to output streams

### 1.1.3 Blocking Configuration

The F8KDX can be configured as a blocking switch if it is an application requirement. For example, it can be configured as a 6 K by 2 K blocking switch.

- 6,144-channel x 2,048-channel blocking switching from ’backplane’ to ’local’ streams
- 2,048-channel x 6,144-channel blocking switching from ’local’ to ’backplane’ streams
- 6,144-channel x 6,144-channel non-blocking switching from ’backplane’ input to ’backplane’ output streams
- 2,048-channel x 2,048-channel non-blocking switching from ’local’ input to ’local’ output streams

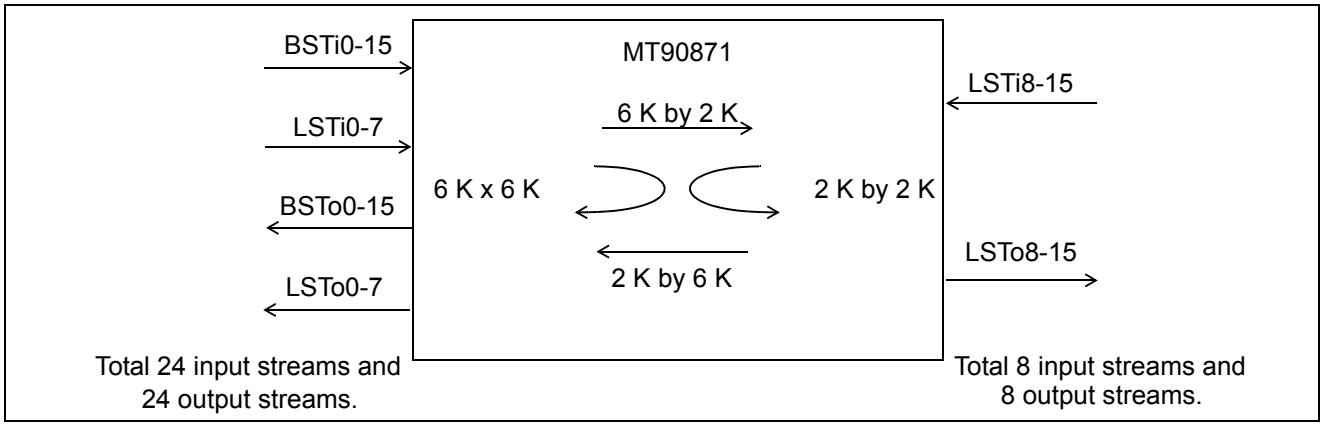


**Figure 5 - 6 K by 2 K Blocking Configuration**

## 2.0 Functional Description

### 2.1 Switching Configuration

The device supports five switching configurations. (1) Backplane-to-Local, (2) Local-to-Backplane, (3) Backplane-to-Backplane, (4) Local-to-Local, and (5) Uni-directional switch. The following sections describe the switching paths in detail. Configurations (1) - (4) enable a non-blocking switch with a maximum capacity of 4,096 input channels and 4,096 output channels at Backplane and Local stream data-rates of 16.384 Mb/s. The switch paths of Configurations (1) to (4) may be operated simultaneously. Configuration (5) provides a uni-directional switch with a maximum capacity of 8,192 x 8,192 channels at 16.384 Mb/s data rate.

### 2.1.1 Backplane-to-Local Path

The device can provide data switching between the Backplane input ports and the Local output ports. The Local Connection Memory determines the switching configurations.

### 2.1.2 Local-to-Backplane Path

The device can provide data switching between the Local input ports and the Backplane output ports. The Backplane Connection Memory determines the switching configurations.

### 2.1.3 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

### 2.1.4 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

### 2.1.5 Uni-directional Switch

The device may be optionally configured to provide an 8,192 x 8,192 uni-directional switch by grouping together all input and all output streams. All streams (LSTi/LSTo0-15 and BSTi/BSTo0-15) may be operated at a data-rate of 16.384 Mb/s. Lower data-rates may be employed with a corresponding reduction in switch capacity.

## 2.2 Port Data Rate Modes and Selection

The selection of individual stream data-rates is summarized in Table 1.

### 2.2.1 Local Port Rate Selection

The Local port has 16 input (LSTi0-15) and 16 output (LSTo0-15) data streams. All input and output streams may be individually selected for operation at a data rate of either 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. The timing of the input and output clocks and frame pulses are shown in Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s Stream Rates.

#### 2.2.1.1 Local Input Port

The bit rate for each input stream is selected by writing to a dedicated Local Input Bit Rate Register (LIBRR0-15). Refer to 38, Local Input Bit Rate Register (LIBRRn) Bits.

| Stream Number | Rate Selection Capability (for each individual stream) |
|---|---|
| Input stream - Local 0-15 (LSTi0-15) | 2.048, 4.096, 8.192 or 16.384 Mb/s |
| Output stream - Local 0-15 (LSTo0-15) | 2.048, 4.096, 8.192 or 16.384 Mb/s |
| Input stream - Backplane 0-15 (BSTi0-15) | 2.048, 4.096, 8.192 or 16.384 Mb/s |
| Output stream - Backplane 0-15 (BSTo0-15) | 2.048, 4.096, 8.192 or 16.384 Mb/s |

**Table 1 - Per-stream Data-Rate Selection: Backplane and Local streams**

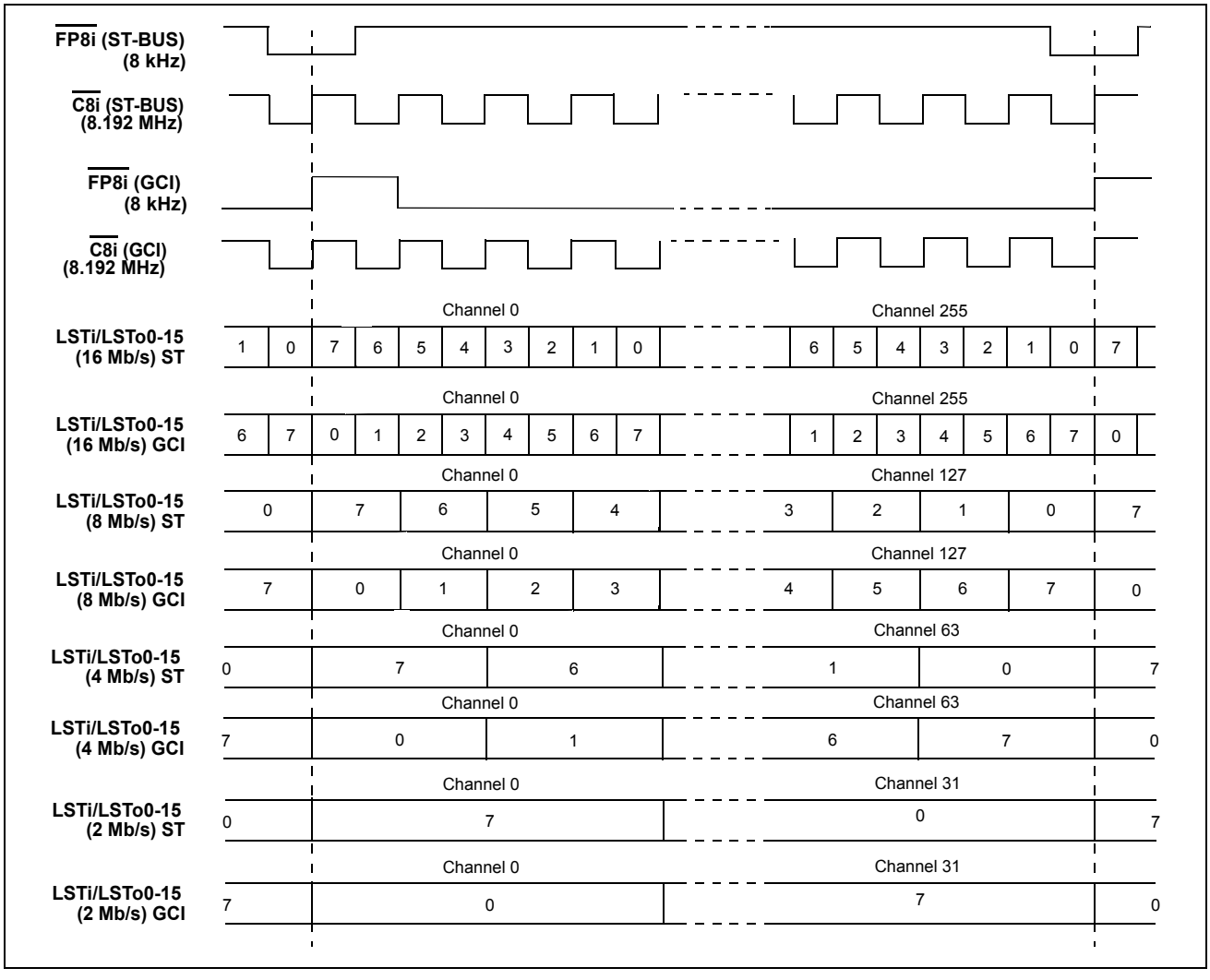


**Figure 6 - Local Port Timing Diagram for 2,4,8 and 16 Mb/s Stream Rates**

### 2.2.1.2 Local Output Port

The bit rate for each output stream is selected by writing to a dedicated Local Output Bit Rate Register (LOBRR0-15). Refer to 40, Local Output Bit Rate Register (LOBRRn) Bits.

Operation of stream data in the Connection Mode or the Message Mode is determined by the state of the LMM bit, and the channel High-impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 6.1 and Section 12.3.

## 2.2.2 Backplane Port Rate Selection

The Backplane port has 16 input (BSTi0-15) and 16 output (BSTo0-15) data streams. All input and output streams may be individually selected for operation at a data rate of either 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. The timing of the input and output clocks and frame pulses are shown in Figure 7, Backplane Port Timing Diagram for 2, 4, 8, and 16 Mb/s stream rates.

### 2.2.3 Backplane Input Port

The bit rate for each input stream is selected by writing to a dedicated Backplane Input Bit Rate Register (BOBRR0-15). Refer to 42, Backplane Input Bit Rate Register (BIBRRn) Bits.

#### 2.2.3.1 Backplane Output Port

The bit rate for each output stream is selected by writing to a dedicated Backplane Output Bit Rate Register (BOBRR0-15). Refer to 44, Backplane Output Bit Rate Register (BOBRRn) Bits.

Operation of stream data in the Connection Mode or the Message Mode is determined by the state of the BMM bit, and the channel High-impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e., from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to section 6.2 "Backplane Connection Memory" and section 12.4 "Backplane Connection Memory Bit Definition".

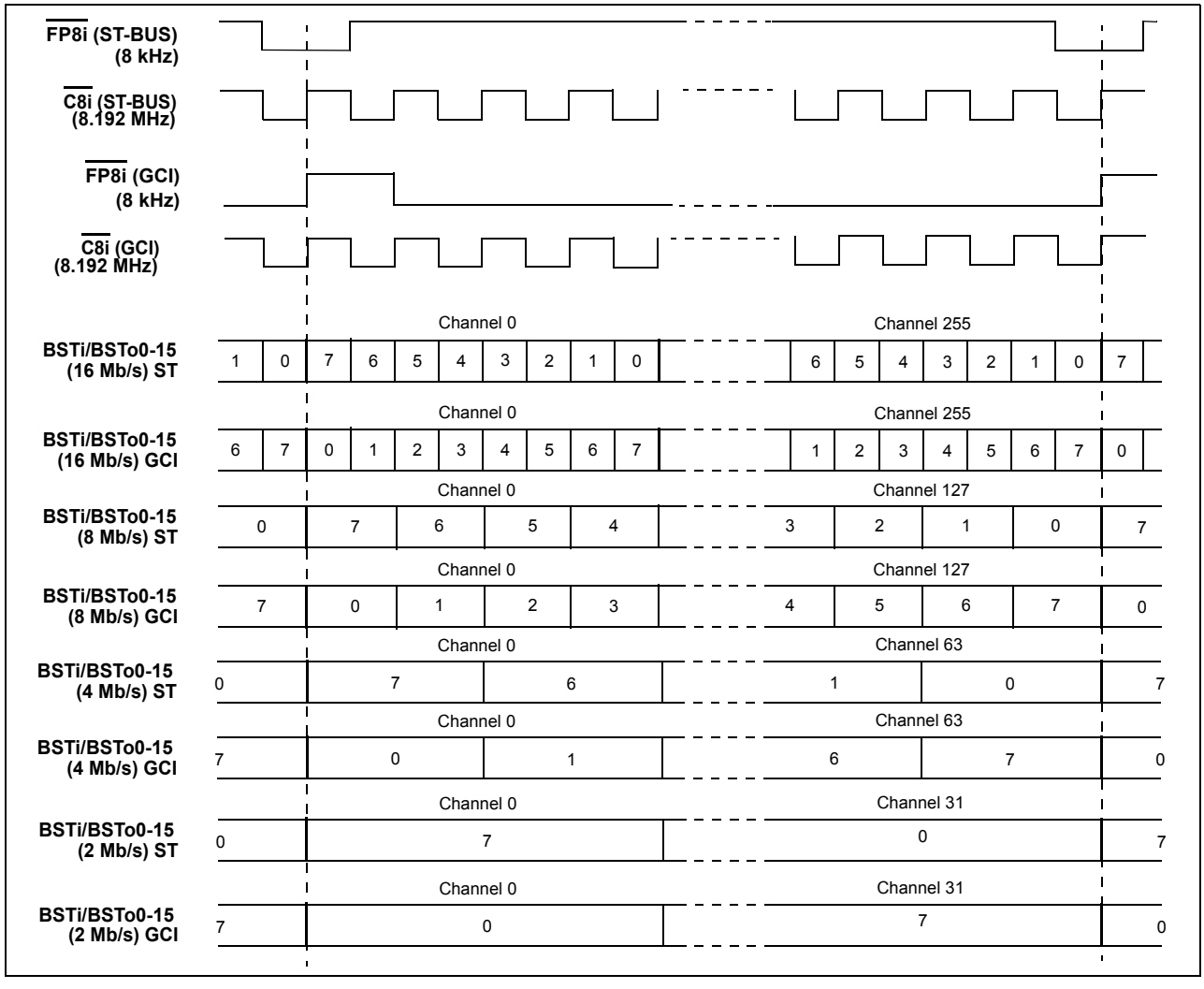


**Figure 7 - Backplane Port Timing Diagram for 2, 4, 8, and 16 Mb/s stream rates**

## 2.3 Backplane Frame Pulse Input and Master Input Clock Timing

The Backplane frame pulse (FP8i) is an 8 kHz input signal active for 122 ns or 244 ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description Table and 13, Control Register Bits, for details.

The active state and timing of FP8i may conform either to the ST-BUS or to the GCI-BUS as shown in Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s Stream Rates, and Figure 7, Backplane Port Timing Diagram for 2, 4, 8, and 16 Mb/s stream rates. The MT90869 will automatically detect whether an ST-BUS or a GCI-BUS style frame pulse is being used for the master frame pulse (FP8i). The device will detect the frame boundary alignment using the rising edge of the input clock (C8i), provided the C8IPOL bit in Table 13, “Control Register Bits,” on page 35 is set to one. Before the C8IPOL bit is set to one, the frame boundary will not be detected correctly. For the purposes of describing the device operation, the remaining part of this document assumes the ST-BUS style frame pulse with a single width frame pulse of 122 ns and the C8IPOL bit is set to one unless explicitly stated otherwise.

In addition, the device provides FP8o, FP16o, C8o and C16o outputs to support external devices which connect to the Local port. The Local frame pulses (FP8o, FP16o) will be provided in the same style as the master frame pulse (FP8i). The polarity of C8o and C16o, at the Frame Boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the external clock frequency to generate an internal clock signal operated at 131.072 MHz.

## 2.4 Backplane Frame Pulse Input and Local Frame Pulse Output Alignment

The MT90871 accepts a Backplane Frame Pulse (FP8i) and generates the Local Frame Pulse outputs, FP8o and FP16o, which are aligned to the master frame pulse. There is a constant three frame delay for data being switched. Figure 8, Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s, shows the backplane and local frame pulse alignment for different data rates.

For further details of Frame Pulse conditions and options see Section 13.1 "Control Register (CR)", Figure 17, Frame Boundary Conditions, ST- BUS Operation, and Figure 18, Frame Boundary Conditions, GCI - BUS Operation.

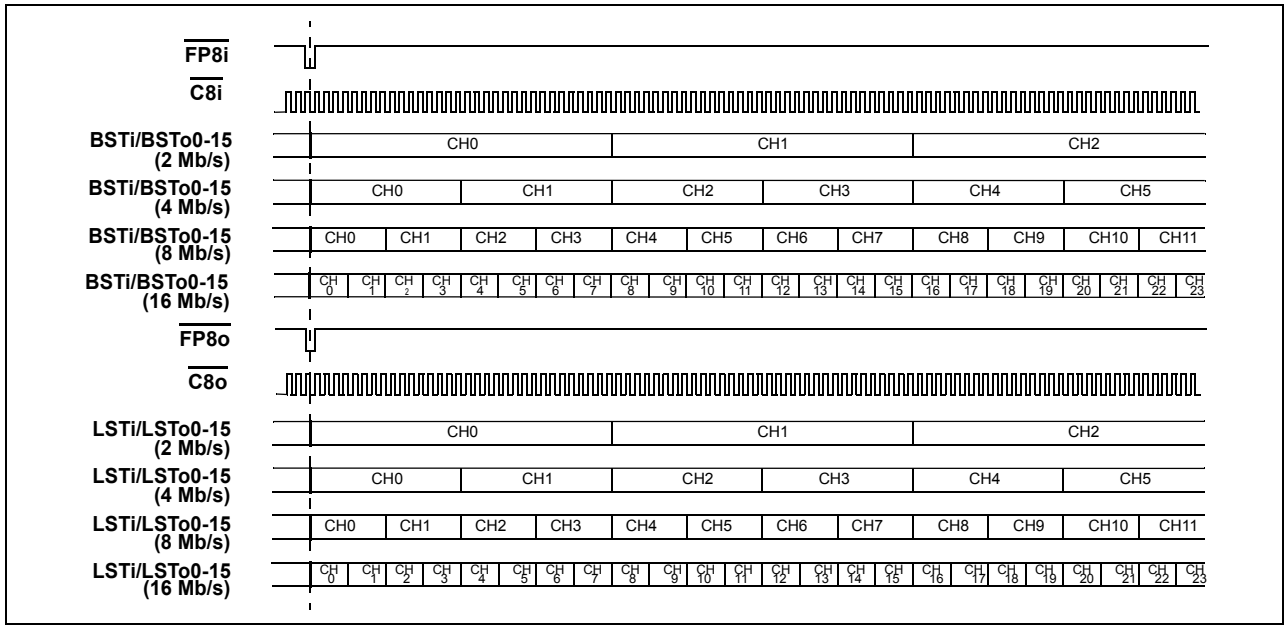


**Figure 8 - Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s**

## 3.0 Input and Output Offset Programming

### 3.1 Input Channel Delay Programming (Backplane and Local Input Streams)

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

The control of the Input Channel Delay and the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, $\overline{\text{FP8i}}$. By default, all input streams have channel delay of zero such that Ch0 is the first channel that appears after the frame boundary.

By programming the Backplane or Local input channel delay registers, BCDR0-15 and LCDR0-15, users can assign the Ch0 position to be located at any one of the channel boundaries in a frame. For delays within channel boundaries, the input bit delay programming can be used. The use of Input Channel Delay in combination with Input Bit Delay enables the Ch0 position to be placed anywhere within a frame to a resolution of 1/4 of the bit period.

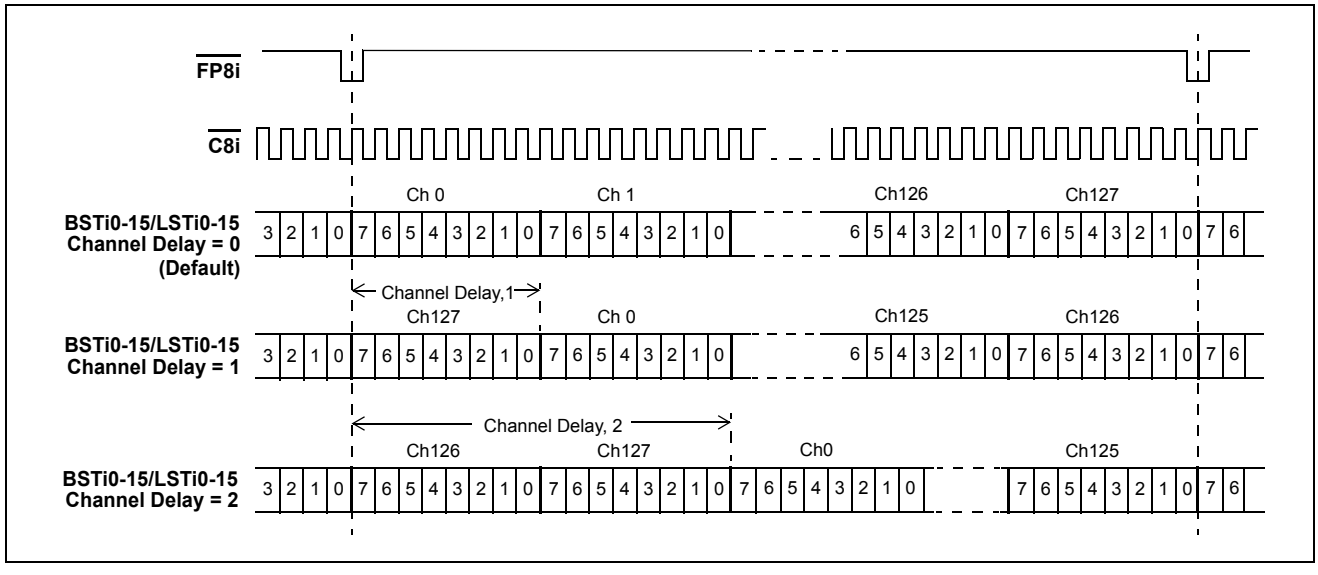


**Figure 9 - Backplane and Local Input Channel Delay Timing Diagram (8 Mb/s)**

### 3.2 Input Bit Delay Programming (Backplane and Local Input Streams)

In addition to the Input Channel Delay programming, the Input Bit Delay programming feature provides users with greater flexibility when designing switch matrices for high speed operation. The input bit delay may be programmed on a per-stream basis to accommodate delays created on PCM highways. For all streams the delay is up to 7 3/4 bits with a resolution of 1/4 bit, for the selected data-rate.

See Figure 10 and Figure 11 for Input Bit Delay Timing at 16 Mb/s and 8 Mb/s data rates, respectively.

The Local input delay is defined by the Local Input Delay registers, LIDR0 to LIDR15, corresponding to the Local data streams, LSTi0 to LSTi15, and the Backplane input delay is defined by the Backplane Input Delay registers, BIDR0 to BIDR15, which correspond to the Backplane data streams, BSTi0 to BSTi15.

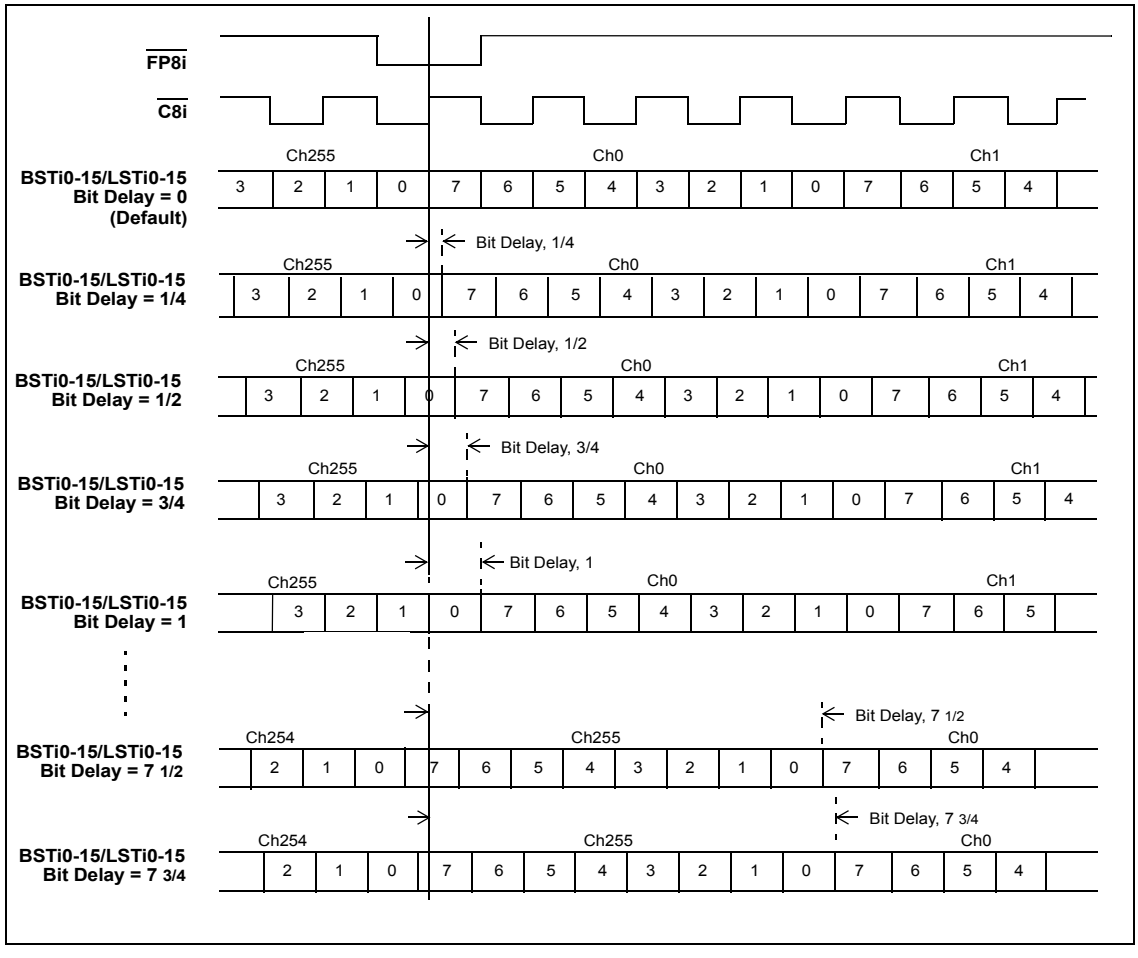


**Figure 10 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16 Mb/s**

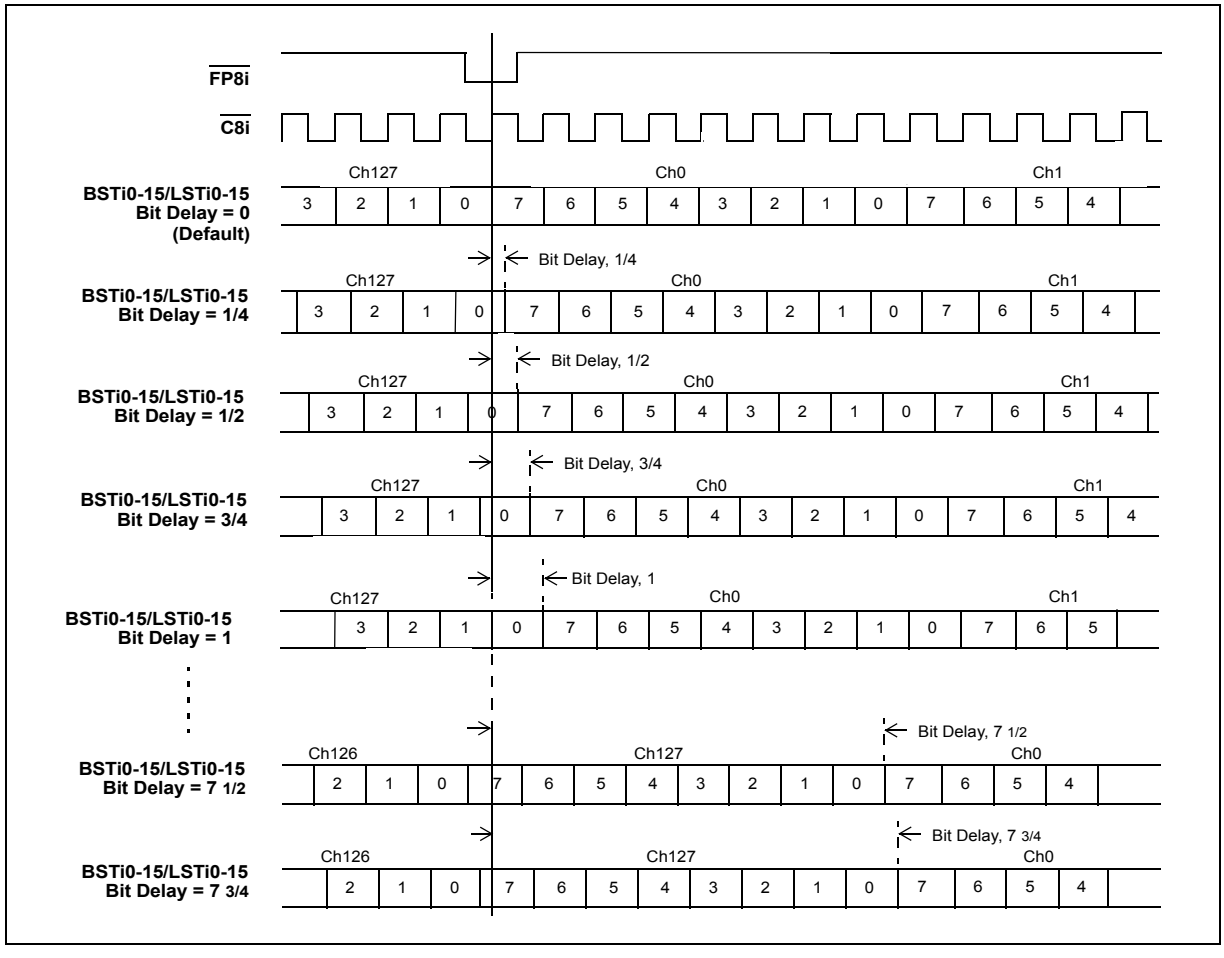


**Figure 11 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 8 Mb/s**

## 3.3 Output Advancement Programming (Backplane and Local Output Streams)

This feature is used to advance the output channel alignment of individual Local or Backplane output streams with respect to the frame boundary. Each output stream has its own advancement value which can be programmed by the output advancement registers. The output advancement selection is useful in compensating for various parasitic loading on the serial data output pins.

### 3.3.1 Local Output Advancement Programming

The Local output advancement registers, **LOAR0-15**, are used to control the Local output advancement. The advancement is determined with reference to the internal system clock rate (131.072 MHz). For 2 Mb/s, 4 Mb/s, 8 Mb/s or 16 Mb/s streams the advancement may be 0, -2 cycles, -4 cycles or -6 cycles, which converts to approximately 0 ns, -15 ns, -30 ns or -45 ns as shown in Figure 12.

### 3.3.2 Backplane Output Advancement Programming

The Backplane output advancement registers, **BOAR0-15** are used to control the Backplane output advancement. The advancement is determined with reference to the internal system clock rate (131.072 MHz). For 2 Mb/s, 4 Mb/s, 8 Mb/s or 16 Mb/s streams the advancement may be 0, -2 cycles, -4 cycles or -6 cycles, which converts to approximately 0ns, -15 ns, -30 ns or -45 ns as shown in Figure 12.

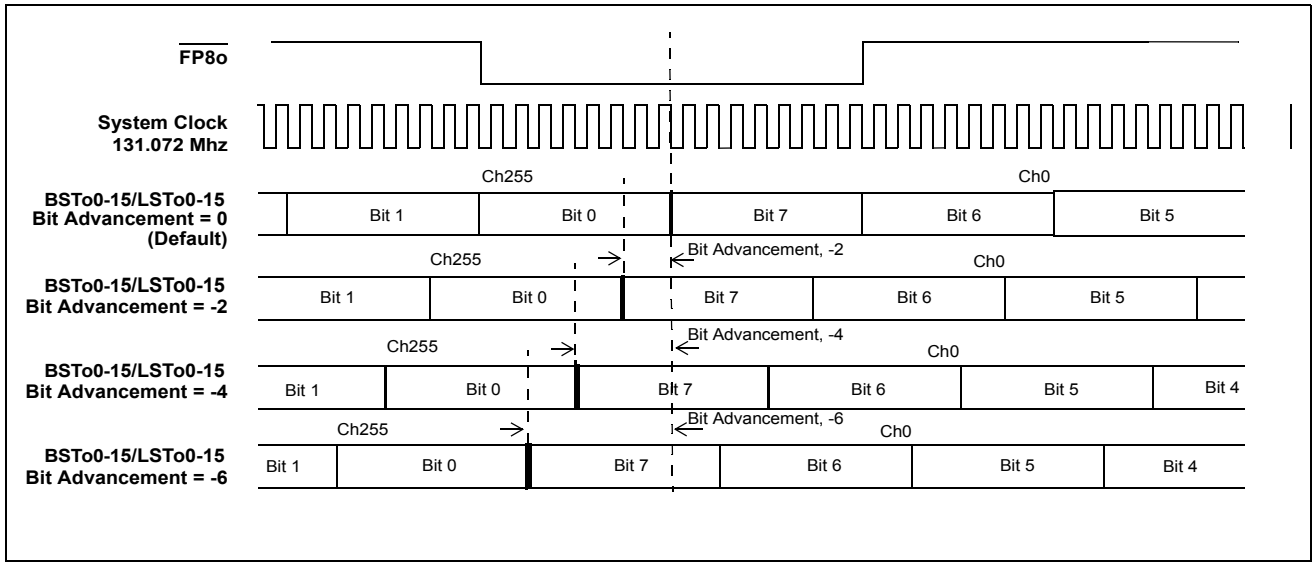


**Figure 12 - Backplane and Local Output Advancement Timing Diagram for Data Rate of 16 Mb/s**

## 4.0 Port High Impedance Control

### 4.1 Local Port High Impedance Control

The input pin **LORS** selects whether the Local output streams **LSTo0-15** are set to high impedance at the output of the MT90871 itself or are always driven (active HIGH or active LOW) and a high impedance state, if required on a per-channel basis, is invoked through an external interface circuit controlled by the **LCSTo0-1** signals. Setting **LORS** to a LOW state will configure the output streams **LSTo0-15** to transmit bi-state channel data with per-channel high-impedance determined by external circuits under the control of the **LCSTo0-1** outputs. Setting **LORS** to a HIGH state will configure the output streams **LSTo0-15** of the MT90871 to invoke a high-impedance output on a per-channel basis.

The **LORS** pin is an asynchronous input and is expected to be hard-wired for a particular system application, although it may be driven under logic control if preferred.

#### 4.1.1 LORS Set LOW

The data (channel control bit) transmitted by **LCSTo0-1** replicates the Local Output Enable Bit (**LE**) of the Local Connection Memory, with a LOW state indicating that the channel should be set to High Impedance by external drivers. Refer to section 12.3 "Local Connection Memory Bit Definition" for setting the Local Output Enable Bit (**LE**).

The **LCSTo0-1** outputs transmit serial data (channel control bits) at 16.384 Mb/s, with each bit representing the per-channel high impedance state for specific streams. Eight output streams are allocated to each control line as follows:

- LCSTo0 outputs the channel control bits for streams LSTo0, 2, 4, 6, 8, 10, 12 and 14.
- LCSTo1 outputs the channel control bits for streams LSTo1, 3, 5, 7, 9, 11, 13 and 15.

(See also “**Pin Description**”.)

The Channel Control Bit location, within a frame period, for each channel of the Local output streams is presented in Table 2 "LCSTo Allocation of Channel Control Bits to the Output Streams"**.**

As an aid to the description, the channel control bit for a single channel on specific streams is presented, with reference to Table 2.

1. The Channel Control Bit corresponding to Stream 0, Channel 0, **LSTo0_Ch0,** is transmitted on **LCSTo0** and is advanced, relative to the Frame Boundary, by 10 periods of **C16o**.
2. The Channel Control Bit corresponding to Stream 14, Channel 0, **LSTo14_Ch0,** is transmitted on **LCSTo0** in advance of the Frame Boundary by three periods of output clock, **C16o**. Similarly, the Channel Control Bit for **LSTo15_Ch0** is advanced relative to the Frame Boundary by three periods of **C16o**, on **LCSTo1**.

The **LCSTo0-1** outputs data at a constant data-rate of 16.384 Mb/s, independent of the data-rate selected for the individual output streams, **LSTo0-15**. Streams at data-rates lower than 16.384 Mb/s will have the value of the respective channel control bit repeated for the duration of the channel. The bit will be transmitted twice for 8.192 Mb/s streams, four times for 4.096 Mb/s streams and eight times for 2.048 Mb/s streams. The channel control bit is not repeated for 16.384 Mb/s streams.

Examples are presented, with reference to Table 2:

3. With stream **LSTo2** selected to operate at a data-rate of 2.048 Mb/s, the value of the Channel Control Bit for **Channel 0** will be transmitted during the **C16o** clock period nos. 2040, 2048, 8, 16, 24, 32, 40 and 48.
4. With stream **LSTo4** operated at a data-rate of 8.192 Mb/s, the value of the Channel Control Bit for **Channel 1** will be transmitted during the **C16o** clock period nos. 9 and 17.

Figure 13, Local Port External High Impedance Control Bit Timing (ST-Bus Mode) shows the channel control bits for **LCSTo0** and **LCSTo1** in one possible scenario which includes stream **LSTo0** at a data-rate of 16.384 Mb/s, **LSTo1** at 8.192 Mb/s, **LSTo6** at 4.096 Mb/s and **LSTo7** at 2.048 Mb/s. All remaining streams are operated at a data-rate of 16.384 Mb/s.

### 4.1.2 LORS Set HIGH

The Local Output Enable Bit (**LE**) of the Local Connection Memory has direct per-channel control on the high-impedance state of the Local Output streams, **LSTo0-15**. Programming a LOW state will set the stream output of the MT90871 to High Impedance for the duration of the channel period. See section 12.3 "Local Connection Memory Bit Definition", for programming details.

The **LCSTo0-1** outputs remain active.

| | **Allocated Stream No.** | | **Allocated Channel No. [2]** | | | |
|---|---|---|---|---|---|---|
| **$\overline{\text{C16o}}$ Period[1]** | **LCSTo0** | **LCSTo1** | **16 Mb/s** | **8 Mb/s** | **4 Mb/s** | **2 Mb/s** |
| 2039 | 0 [3-1] | 1 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |
| 2040 | 2 [3-3] | 3 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |
| 2041 | 4 | 5 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |
| 2042 | 6 | 7 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |
| 2043 | 8 | 9 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |
| 2044 | 10 | 11 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |
| 2045 | 12 | 13 | Ch 0 | Ch 0 | Ch 0 | Ch 0 |

**Table 2 - LCSTo Allocation of Channel Control Bits to the Output Streams**