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ISO^2-CMOS ST-BUS^{TM} Family MT9092
Digital Telephone with HDLC (HPhone-II)

Data Sheet

August 2005

Features

- Programmable μ-Law/A-Law codec and filters
- Programmable CCITT (G.711)/sign-magnitude coding
- Programmable transmit, receive and side-tone gains
- DSP-based:
  - i) Speakerphone switching algorithm
  - ii) DTMF and single tone generator
  - iii) Tone Ringer
- Differential interface to telephony transducers
- Differential audio paths
- Single 5 volt power supply
- X.25 Level 2 HDLC data formatting

Applications

- Fully featured digital telephone sets
- Cellular phone sets
- Local area communications stations

Ordering Information

MT9092APR	44 Pin PLCC	Tape & Reel
MT9092AP	44 Pin PLCC	Tubes
MT9092APR1	44 Pin PLCC*	Tape & Reel
MT9092AP1	44 Pin PLCC*	Tubes

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT9092 HPhone-II is a fully featured integrated digital telephone circuit which includes an HDLC data formatter. Voice band signals are converted to digital PCM and vice versa by a switched capacitor Filter/Codec. The Filter/Codec uses an ingenious differential architecture to achieve low noise operation over a wide dynamic range with a single 5V supply. A Digital Signal Processor provides handsfree speaker-phone operation. The DSP is also used to generate tones (DTMF, Ringer and Call Progress) and control audio gains. Internal registers are accessed through a serial microport conforming to INTEL MCS-51™ specifications. The device is fabricated in Zarlink's low power ISO^2-CMOS technology.

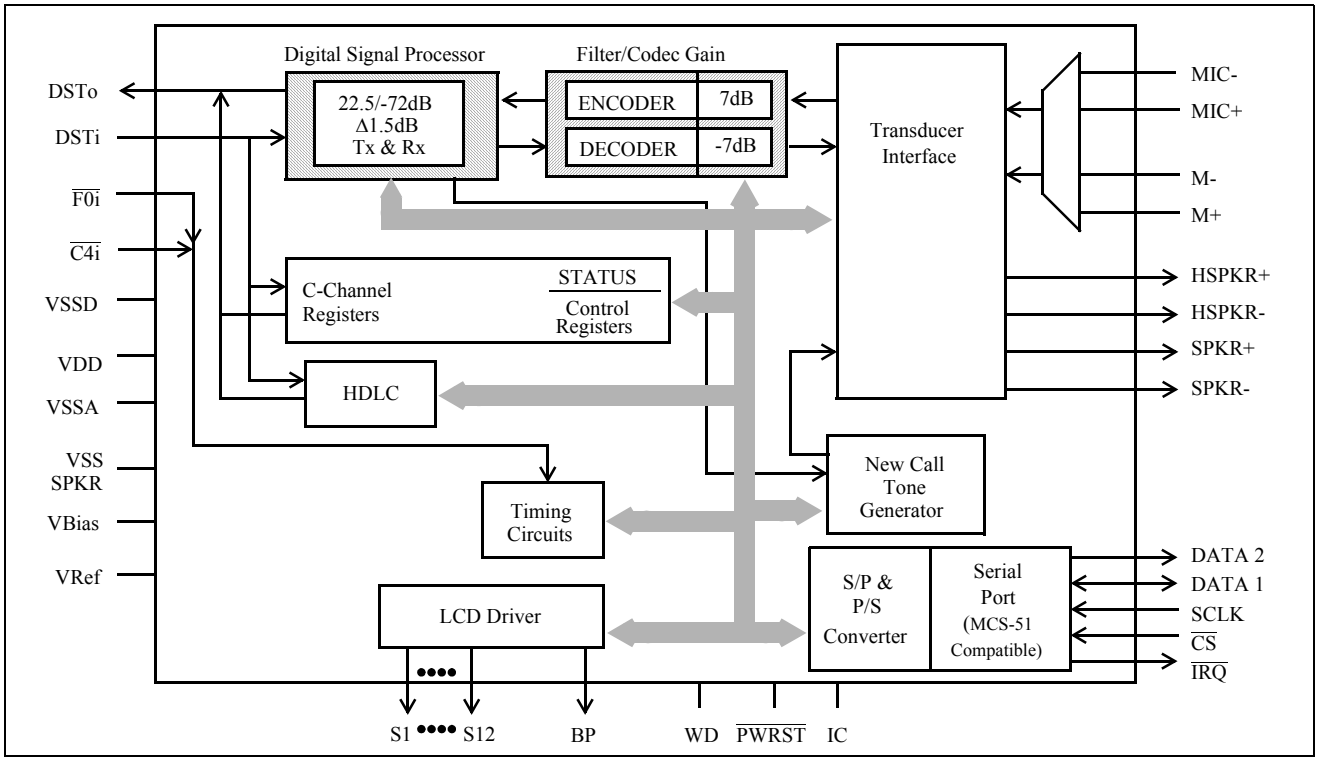

Figure 1 - Functional Block Diagram

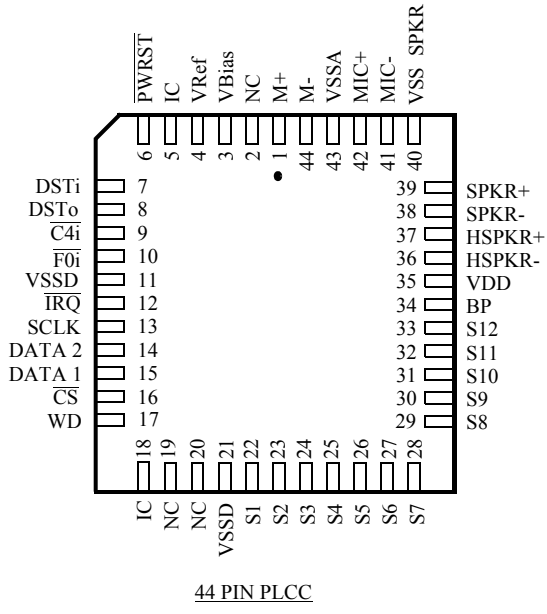

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	M+	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
2	NC	**No Connect.** No internal connection to this pin.
3	V_{Bias}	**Bias Voltage (Output).** (V_{DD}/2) volts is available at this pin for biasing external amplifiers. Connect 0.1 µF capacitor to V_{SSA}.
4	V_{Ref}	**Reference voltage for codec (Output).** Nominally [(V_{DD}/2)-1.5] volts. Used internally. Connect 0.1 µF capacitor to V_{SSA}.
5	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
6	$\overline{PWRST}$	**Power-up Reset (Input).** CMOS compatible input with Schmitt Trigger (active low).
7	DSTi	**ST-BUS Serial Stream (Input).** 2048 kbit/s input stream composed of 32 eight bit channels; the first four of which are used by the MT9092. Input level is TTL compatible.
8	DSTo	**ST-BUS Serial Stream (Output).** 2048 kbit/s output stream composed of 32 eight bit channels. The MT9092 sources digital signals during the appropriate channel, time coincident with the channels used for DSTi.
9	$\overline{C4i}$	**4096 kHz Clock (Input).** CMOS level compatible.
10	$\overline{F0i}$	**Frame Pulse (Input).** CMOS level compatible. This input is the frame synchronization pulse for the 2048 kbit/s ST-BUS stream.
11	V_{SSD}	**Digital Ground .** Nominally 0 volts.
12	$\overline{IRQ}$	**Interrupt Request (Open Drain Output).** An active low output indicating an unmasked HDLC interrupt event. Requires 1 kΩ pull-up to V_{DD}.

Pin Description (continued)

Pin #	Name	Description
13	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for MCS-51 compatible microport. TTL level compatible.
14	DATA 2	**Serial Data Transmit.** In an alternate mode of operation, this pin is used for data transmit from MT9092. In the default mode, serial data transmit and receive are performed on the DATA 1 pin and DATA 2 is tri-stated.
15	DATA 1	**Bidirectional Serial Data.** Port for microprocessor serial data transfer compatible with MCS-51 standard (default mode). In an alternate mode of operation , this pin becomes the data receive pin only and data transmit is performed on the DATA 2 pin. Input level TTL compatible.
16	$\overline{CS}$	**Chip Select (Input).** This input signal is used to select the device for microport data transfers. Active low. (TTL level compatible.)
17	WD	**Watchdog (Output).** Watchdog timer output. Active high.
18	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
19, 20	NC	**No Connection.** No internal connection to these pins.
21	V_{SSD}	**Digital Ground.** Nominally 0 volts.
22-33	S1-S12	**Segment Drivers (Output).** 12 independently controlled, two level, LCD segment drivers. An in-phase signal, with respect to the BP pin, produces a non-energized LCD segment. An out-of-phase signal, with respect to the BP pin, energizes its respective LCD segment.
34	BP	**Backplane Drive (Output).** A two-level output voltage for biasing an LCD backplane.
35	V_{DD}	**Positive Power Supply (Input).** Nominally 5 volts.
36	HSPKR-	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
37	HSPKR+	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
38	SPKR-	**Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
39	SPKR+	**Non-Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
40	V_{SS} SPKR	**Power Supply Rail for Analog Output Drivers.** Nominally 0 Volts.
41	MIC-	**Inverting Handsfree Microphone (Input).** Handsfree microphone amplifier inverting input pin.
42	MIC+	**Non-inverting Handsfree Microphone (Input).** Handsfree microphone amplifier non-inverting input pin.
43	V_{SSA}	**Analog Ground.** Nominally 0 V.
44	M-	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.

NOTES:
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Overview

The functional block diagram of Figure 1 depicts the main operations performed within the HPhone-II. Each of these functional blocks will be described in the sections to follow. This overview will describe some of the end-user features which may be implemented as a direct result of the level of integration found within the HPhone-II.

The main feature required of a digital telephone is to convert the digital Pulse Code Modulated (PCM) information, being received by the telephone set, into an analog electrical signal. This signal is then applied to an appropriate audio transducer such that the information is finally converted into intelligible acoustic energy. The same is true of the reverse direction where acoustic energy is converted first into an electrical analog and then digitized (into PCM) before being transmitted from the set. Along the way if the signals can be manipulated, either in the analog or the digital domains, other features such as gain control, signal generation and filtering may be added. More complex processing of the digital signal is also possible and is limited only be the processing power available. One example of this processing power may be the inclusion of a complex handsfree switching algorithm. Finally, most electro-acoustic transducers (loudspeakers) require a large amount of power to develop an effective acoustic signal. The inclusion of audio amplifiers to provide this power is required.

The HPhone-II features Digital Signal Processing (DSP) of the voice encoded PCM, complete Analog/Digital and Digital/Analog conversion of audio signals (Filter/CODEC) and an analog interface to the external world of electro-acoustic devices (Transducer Interface). These three functional blocks combine to provide a standard full-duplex telephone conversation utilizing a common handset. Selecting transducers for handsfree operation, as well as allowing the DSP to perform its handsfree switching algorithm, is all that is required to convert the full-duplex handset conversation into a half-duplex speakerphone conversation. In each of these modes, full programmability of the receive path and side-tone gains is available to set comfortable listening levels for the user as well as transmit path gain control for setting nominal transmit levels into the network.

The HPhone-II's HDLC block is easy to use in proprietary signalling protocols such as those within PABXs and Key Systems. A fully interrupt driven interface, buffered by 19 byte FIFOs in each direction, simplifies the microcontroller's asynchronous access to the D-Channel information.

The ability to generate tones locally provides the designer with a familiar method of feedback to the telephone user as they proceed to set-up, and ultimately, dismantle a telephone conversation. Also, as the network slowly evolves from the dial pulse/DTMF methods to the D-Channel protocols it is essential that the older methods be available for backward compatibility. As an example; once a call has been established, say from your office to your home, using the D-Channel signalling protocol it may be necessary to use in-band DTMF signalling to manipulate your personal answering machine in order to retrieve messages. Thus the locally generated tones must be of network quality and not just a reasonable facsimile. The HPhone-II DSP can generate the required tone pairs as well as single tones to accommodate any in-band signalling requirement.

Each of the programmable parameters within the functional blocks is accessed through a serial microcontroller port compatible with Intel MCS-51 specifications.

Functional Description

In this section, each functional block within the HPhone-II is described along with all of the associated control/status bits. Each time a control/ status bit(s) is described it is followed by the address register where it will be found. The reader is referred to the section titled 'Register Summary' for a complete listing of all address map registers, the control/status bits associated with each register and a definition of the function of each control/status bit. The Register Summary is useful for future reference of control/status bits without the need to locate them within the text of the functional descriptions.

Filter-CODEC

The Filter/CODEC block implements conversion of the analog 3.3kHz speech signals to/from the digital domain compatible with 64 kb/s PCM B-Channels. Selection of companding curves and digital code assignment are register programmable. These are CCITT G.711 A-law or μ-Law, with true-sign/ Alternate Digit Inversion or true-

sign/Inverted Magnitude coding, respectively. Optionally, sign- magnitude coding may also be selected for proprietary applications.

The Filter/CODEC block also implements transmit and receive audio path gains in the analog domain. These gains are in addition to the digital gain pad provided in the DSP section and provide an overall path gain resolution of 0.5dB. A programmable gain, voice side-tone path is also included to provide proportional transmit speech feedback to the handset receiver so that a dead sounding handset is not encountered. Figure 3 depicts the nominal half-channel and side-tone gains for the HPhone-II.

On $\overline{\text{PWRST}}$ (pin 6) the Filter/CODEC defaults such that the side-tone path, dial tone filter and 400 Hz transmit filter are off, all programmable gains are set to 0 dB and μ-Law companding is selected. Further, the Filter/CODEC is powered down due to the PuFC bit (Transducer Control Register, address 0Eh) being reset. This bit must be set high to enable the Filter/CODEC.

The internal architecture is fully differential to provide the best possible noise rejection as well as to allow a wide dynamic range from a single 5 volt supply design. This fully differential architecture is continued into the Transducer Interface section to provide full chip realization of these capabilites.

A reference voltage (V_{Ref}), for the conversion requirements of the CODER section, and a bias voltage (V_{Bias}), for biasing the internal analog sections, are both generated on-chip. V_{Bias} is also brought to an external pin so that it may be used for biasing any external gain plan setting amplifiers. A 0.1 μF capacitor must be connected from V_{Bias} to analog ground at all times. Likewise, although V_{Ref} may only be used internally, a 0.1 μF capacitor from the V_{Ref} pin to ground is required at all times. It is suggested that the analog ground reference point for these two capacitors be physically the same point.

To facilitate this the V_{Ref} and V_{Bias} pins are situated on adjacent pins.

The transmit filter is designed to meet CCITT G.714 specifications. The nominal gain for this filter path is 0 dB (gain control = 0 dB). An anti-aliasing filter is included. This is a second order lowpass implementation with a corner frequency at 25 kHz. Attenuation is better than 32 dB at 256 kHz and less than 0.01 dB within the passband.

An optional 400 Hz high-pass function may be included into the transmit path by enabling the Tfhp bit in the Transducer Control Register (address 0Eh). This option allows the reduction of transmitted background noise such as motor and fan noise.

The receive filter is designed to meet CCITT G.714 specifications. The nominal gain for this filter path is 0 dB (gain control = 0 dB). Filter response is peaked to compensate for the sinx/x attenuation caused by the 8 kHz sampling rate.

The Rx filter function can be altered by enabling the DIAL EN control bit in the Transducer Control Register (address 0Eh). This causes another lowpass function to be added, with a 3 dB point at 1000 Hz. This function is intended to improve the sound quality of digitally generated dial tone received as PCM.

Transmit sidetone is derived from the Tx filter and is subject to the gain control of the Tx filter section. Sidetone is summed into the receive path after the Rx filter gain control section so that Rx gain adjustment will not affect sidetone levels. The side-tone path may be enabled/disabled with the SIDE EN bit located in the Transducer Control Register (address 0Eh). See also STG_0-STG_2 (address 0Bh).

Transmit and receive filter gains are controlled by the $TxFG_0$-$TxFG_2$ and $RxFG_0$-$RxFG_2$ control bits respectively. These are located in the FCODEC Gain Control Register 1 (address 0Ah). Transmit filter gain is adjustable from 0 dB to +7 dB and receive filter gain from 0 dB to -7 dB, both in 1 dB increments.

Side-tone filter gain is controlled by the STG_0-STG_2 control bits located in the FCODEC Gain Control Register 2 (address 0Bh). Side-tone gain is adjustable from -9.96 dB to +9.96 dB in 3.32 dB increments.

Law selection for the Filter/$\overline{\text{CODEC}}$ is provided by the A/μ companding control bit while the coding scheme is controlled by the sign-mag/$\overline{\text{CCITT}}$ bit. Both of these reside in the General Control Register (address 0Fh).

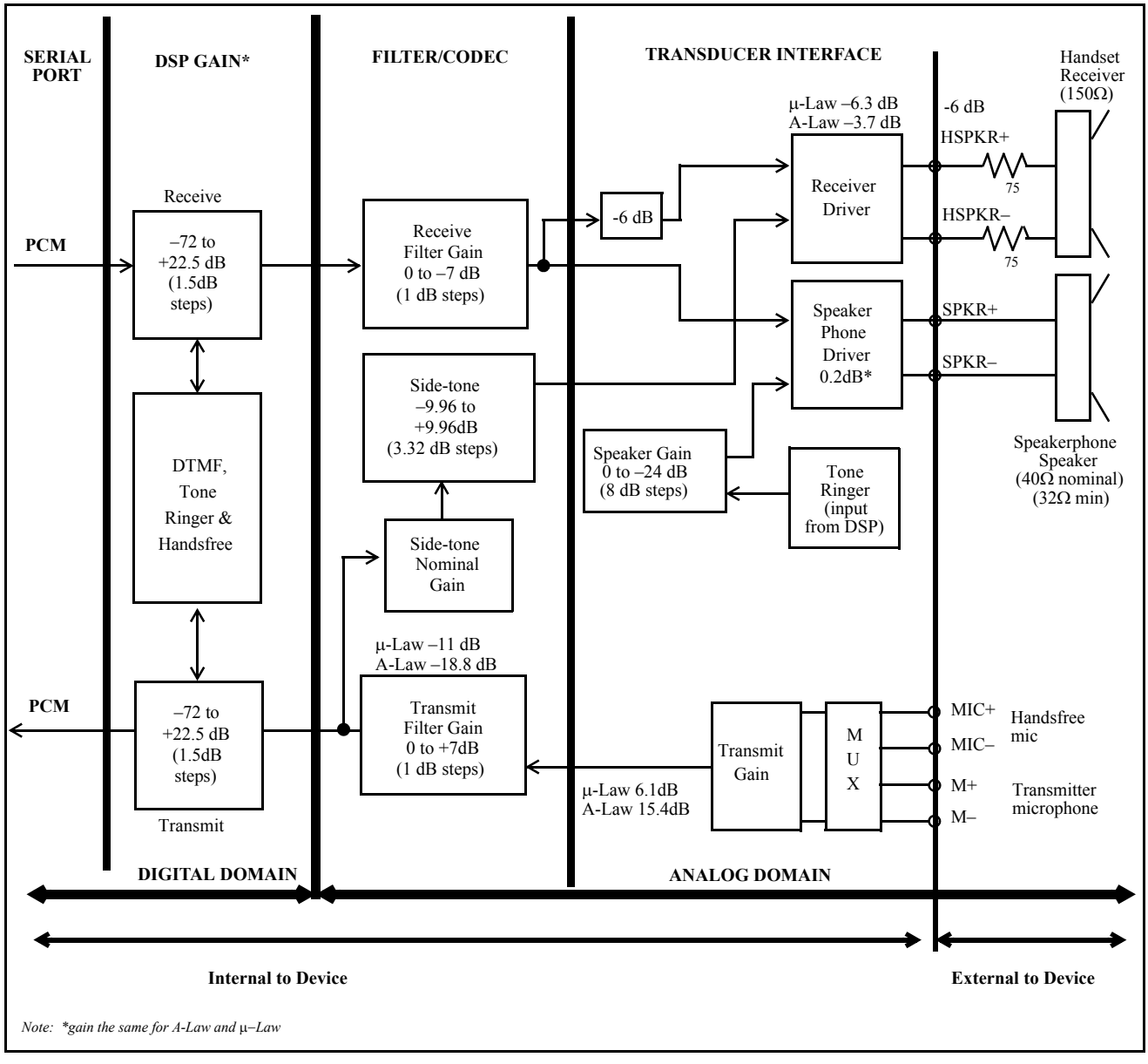

Figure 3 - Audio Gain Partitioning

Digital Signal Processor

The DSP block is located, functionally, between the serial ST-BUS port and the Filter/CODEC block. Its main purpose is to provide both a digital gain control and a half-duplex handsfree switching function. The DSP will also generate the digital patterns required to produce standard DTMF signalling tones as well as single tones and a tone ringer output. A programmable (ON/OFF) offset null routine may also be performed on the transmit PCM data stream. The DSP can generate a ringer tone to be applied to the speakerphone speaker during normal handset operation so that the existing call is not interrupted.

The main functional control of the DSP is through two hardware registers which are accessible at any time via the microport. These are the Receive Gain Control Register at address 1Dh and the DSP Control Register at address 1Eh. In addition, other functional control is accomplished via multiple RAM-based registers which are accessible only while the DSP is held in a reset state. This is accomplished with the DRESET bit of the DSP Control Register. Ram-based registers are used to store transmit gain levels (20h for transmit PCM and 21h for transmit DTMF

levels), the coefficients for tone and ringer generation (addresses 23h and 24h), and tone ringer warble rates (address 26h). All undefined addresses below 20h are reserved for the temporary storage of interim variables calculated during the execution of the DSP algorithms. These undefined addresses should not be written to via the microprocessor port. The DSP can be programmed to execute the following micro-programs which are stored in instruction ROM, (see PS0 to PS2, DSP Control Register, address 1Eh). All program execution begins at the frame pulse boundary.

PS2	PS1	PS0	Micro-program
0	0	0	Power up reset program
0	0	1	Transmit and receive gain control program; with autonulling of the transmit PCM, if the AUTO bit is set (see address 1Dh)
0	1	0	DTMF generation plus transmit and receive gain control program (autonull available via the AUTO control bit)
0	1	1	Tone ringer plus transmit and receive gain control program (autonull available via the AUTO control bit)
PS2	**PS1**	**PS0**	**Micro-program**
1	0	0	handsfree switching program
1	0	1	
1	1	0	Last three selections reserved
1	1	1	

Note: For the DSP to function it must be selected to operate, in conjunction with the Filter/Codec, in one of the B-Channels. Therefore, one of the B-Channel enable bits must be set (see Timing Control, address 15h : bits CH_2EN and CH_3EN).

Power Up reset Program

A hardware power-up reset (pin 6, $\overline{\text{PWRST}}$) will initialize the DSP hardware registers to the default values (all zeros) and will reset the DSP program counter. The DSP will then be disabled and the PCM streams will pass transparently through the DSP. The RAM-based registers are not reset by the $\overline{\text{PWRST}}$ pin but may be initialized to their default settings by programming the DSP to execute the power up reset program. None of the micro-programs actually require the execution of the power up reset program but it is useful for pre-setting the variables to a known condition. Note that the reset program requires one full frame (125 μSec) for execution.

Gain Control Program

Gain control is performed on converted linear code for both the receive and the transmit PCM. Receive gain control is set via the hardware register at address 1Dh (see bits B0 - B5) and may be changed at any time. Gain in 1.5 dB increments is available within a range of +22.5 dB to -72 dB. Normal operation usually requires no more than a +20 to -20 dB range of control. However, the handsfree switching algorithm requires a large attenuation depth to maintain stability in worst case environments, hence the large (-72 dB) negative limit. Transmit gain control is divided into two RAM registers, one for setting the network level of transmit speech (address 20h) and the other for setting the transmit level of DTMF tones into the network (address 21h). Both registers provide gain control in 1.5 dB increments and are encoded in the same manner as the receive gain control register (see address 1Dh, bits B0 - B5). The power up reset program sets the default values such that the receive gain is set to -72.0 dB, the transmit audio gain is set to 0.0 dB and the transmit DTMF gain is set to -3.0 dB (equivalent to a DTMF output level of -4 dBm0 into the network).

Optional Offset Nulling

Transmit PCM may contain residual offset in the form of a DC component. An offset of up to ±fifteen linear bits is acceptable with no degradation of the parameters defined in CCITT G.714. The HPhone-II filter/CODEC guarantees no more than ±ten linear bits of offset in the transmit PCM when the autonull routine is not enabled. By enabling autonulling (see AUTO in the Receive Gain Control Register, address 1Dh) offsets are reduced to within ±one bit of zero. Autonulling circuitry was essential in the first generations of Filter/Codecs to remove the large DC offsets found in the linear technology. Newer technology has made nulling circuitry optional as offered in the HPhone-II.

DTMF and Gain Control Program

The DTMF program generates a dual cosine wave pattern which may be routed into the receive path as comfort tones or into the transmit path as network signalling. In both cases, the digitally generated signal will undergo gain adjustment as programmed into the Receive Gain Control and the Transmit DTMF Gain Control registers. The composite signal output level in both directions is -4 dBm0 when the gain controls are set to 2Eh (-3.0 dB). Adjustments to these levels may be made by altering the settings of the gain control registers. Pre-twist of 2.0 dB is incorporated into the composite signal. The frequency of the low group tone is programmed by writing an 8-bit coefficient into Tone Coefficient Register 1 (address 23h), while the high group tone frequency uses the 8-bit coefficient programmed into Tone Coefficient Register 2 (address 24h). Both coefficients are determined by the following equation:

$$COEFF = 0.128 \times Frequency\ (in\ Hz)$$

where COEFF is a rounded off 8 bit binary integer

A single frequency tone may be generated instead of a dual tone by programming the coefficient at address 23h to a value of zero. In this case the frequency of the single output tone is governed by the coefficient stored at address 24h.

Table 1 gives the standard DTMF frequencies, the coefficient required to generate the closest frequency, the actual frequency generated and the percent deviation of the generated tone from the nominal.

Frequency (Hz)	COEF	Actual Frequency	% Deviation
697	59h	695.3	-.20%
770	63h	773.4	+.40%
852	6Dh	851.6	-.05%
941	79h	945.3	+.46%
1209	9Bh	1210.9	+.20%
1336	ABh	1335.9	.00%
1477	BDh	1476.6	-.03%
1633	D1h	1632.8	-.01%

Table 1 - DTMF Frequencies

DTMF Signal to distortion:

The sum of harmonic and noise power in the frequency band from 50 Hz to 3500 Hz is typically more than 30 dB below the power in the tone pair. All individual harmonics are typically more than 40 dB below the level of the low group tone.

Tone Ringer and Gain Control Program

A locally generated alerting (ringing) signal is used to prompt the user when an incoming call must be answered. The DSP uses the values programmed into Tone Coefficient Registers 1 and 2 (addresses 23h and 24h) to generate two different squarewave frequencies in PCM code. The amplitude of the squarewave frequencies is set to a mid level before being sent to the receive gain control block. From there the PCM passes through the decoder and receive filter, replacing the normal receive PCM data, on its way to the loudspeaker driver. Both coefficients are determined by the following equation:

$$COEFF = 8000/Frequency\ (Hz)$$

where COEFF is a rounded off 8 bit binary integer.

The ringer program switches between these two frequencies at a rate defined by the 8-bit coefficient programmed into the Tone Ringer Warble Rate Register (address 26h). The warble rate is defined by the equation:

$$Tone\ duration\ (warble\ frequency\ in\ Hz) = 500/COEFF$$

where $0 < COEFF < 256$, a warble rate of 5-20Hz is suggested.

An alternate method of generating ringer tones to the speakerphone speaker is available. With this method the normal receive speech path through the decoder and receive filter is uninterrupted to the handset, allowing an existing conversation to continue. The normal DSP and Filter/CODEC receive gain control is also retained by the speech path. When the OPT bit (DSP Control Register address 1Eh) is set high the DSP will generate the new call tone according to the coefficients programmed into registers 23h, 24h and 26h as before. In this mode the DSP output is no longer a PCM code but a toggling signal which is routed directly through the New Call Tone gain control section to the loudspeaker driver. Refer to the section titled ‘New Call Tone’.

Handsfree Program

A half-duplex speakerphone program, fully contained on chip, provides high quality gain switching of the transmit and receive speech PCM to maintain loop stability under most network and local acoustic environments. Gain switching is performed in continuous 1.5 dB increments and operates in a complimentary fashion. That is, with the transmit path at maximum gain the receive path is fully attenuated and vice versa. This implies that there is a mid position where both transmit and receive paths are attenuated equally during transition. This is known as the idle state.

Of the 64 possible attenuator states, the algorithm may rest in only one of three stable states; full receive, full transmit and idle. The maximum gain values for full transmit and full receive are programmable through the microport at addresses 20h and 1Dh respectively, as is done for normal handset operation. This allows the user to set the maximum volumes to which the algorithm will adhere. The algorithm determines which path should maintain control of the loop based upon the relative levels of the transmit and receive audio signals after the detection and removal of background noise energy. If the algorithm determines that neither the transmit or the receive path has valid speech energy then the idle state will be sought. The present state of the algorithm plus the result of the Tx vs. Rx decision will determine which transition the algorithm will take toward its next stable state. The time durations required to move from one stable state to the next are parameters defined in CCITT Recommendation P.34 and are used by default by this algorithm (i.e., build-up time, hang-over time and switching time).

Quiet Code

The DSP can be made to send quiet code to the decoder and receive filter path by setting the RxMUTE bit high. Likewise, the DSP will send quiet code in the transmit (DSTo) path when the TxMUTE bit is high. Both of these

control bits reside in the DSP Control Register at address 1Eh. When either of these bits are low, their respective paths function normally.

HDLC

The High-level Data Link Control (HDLC) block is located, functionally, between the serial ST-BUS port and the serial Microcontroller port. This functional block handles the bit oriented protocol requirements of layer 2 X.25 packet switching and Q.921 link access protocols defined by CCITT. The HDLC is dedicated to D-Channel operation at 16 kb/s and offers buffered access to the serial D-Channel data through separate 19 byte transmit and receive FIFOs.

The HDLC generates and detects the flags, various link channel states and abort sequences as well as performing a cyclic redundancy check on data packets according to the CCITT defined polynomial. Lastly, the protocol functions may be disabled to provide transparent access, of the serial port D-Channel, to the microport.

A power up reset ($\overline{\text{PWRST}}$, pin 6) or a software reset via RST (address 0Fh) will cause the HDLC transceiver to be initialized. This results in the transmitter and receiver being disabled and all HDLC registers defaulting to their power reset values.

HDLC Frame Structure

A valid HDLC frame begins with an opening flag, contains at least 16 bits of address, control or information, ends with a 16 bit FCS followed by a closing flag. Data formatted in this manner is also referred to as a "packet". Refer to Figure 4.

FLAG	DATA FIELD	FCS	FLAG
One Byte	n Bytes (nŠ2)	Two Bytes	One Byte

Figure 4 - Frame Format

Flag Sequence

All HDLC frames start and end with a unique sequence of 8 bits. This sequence is 0111 1110 (7Eh). The closing flag of one frame can be the opening flag of the next frame. The transmitter generates flags and appends them to the packet to be transmitted. The receiver searches the incoming data stream for flags on a bit-by-bit basis to establish frame synchronization. The receiver uses flags for synchronization only and does not transfer them to the Rx FIFO.

Address Field

The address field consists of one or two 8-bit bytes directly following the opening flag. Address, Control and Information fields are known collectively as the Data field.

Control Field

The control field consists of one 8-bit byte directly following the address field. The HDLC does not distinguish between the control field and the information field.

Information Field

The information field immediately follows the control field and consists of N bytes of data where one byte contains 8 bits. A packet does not need to contain an information field to be valid. The HDLC does not distinguish between the control field and the information field.

Frame Checking Sequence Field

The 16 bits preceding a closing flag are the FCS field. A cyclic redundancy check utilizing the CRC-CCITT standard generator polynomial $X^{16} + X^{12} + X^5 + 1$ produces the 16-bit FCS. In the transmitter the FCS is calculated on all bits of the address, control and information fields. The complement of the FCS is transmitted, most significant bit first, in the FCS field. The receiver calculates the FCS on the incoming packet's address, control, information and FCS fields and compares the result to 'F0B8'. This result verifies no transmission errors occurred. If the packet, between flags, is also at least 32 bits in length then the address, control and information field data are entered into the receive FIFO minus the FCS which is discarded.

Order of Bit Transmission

Address, control and information field data are entered into the transmit FIFO. This data is then transmitted and received on the serial bus least significant bit first. The FCS is sent most significant bit first on the serial bus. Note that it is the complement of the calculated FCS which is transmitted. The HDLC does not distinguish ADDRESS/CONTROL/INFORMATION bytes except to determine if the packet is of minimum valid length. These fields are transferred transparently through the FIFO's.

Data Transparency (Zero insertion/deletion)

Transparency ensures that the contents of a data packet do not imitate a flag, go-ahead, frame abort or idle channel. The contents of a transmitted frame, between the flags, is examined on a bit-by-bit basis and a 0 bit is inserted after all sequences of five contiguous 1 bits (including the last five bits of the FCS). Upon receiving five contiguous 1s within a frame the receiver deletes the following 0 bit.

Invalid Frames

A frame is invalid if one of the following four conditions exists. Inserted zeros are not part of a valid bit count:

1. If the FCS pattern generated from the received data does not match the 'F0B8' pattern then the last data byte of the packet is written to the receive FIFO with a 'bad packet' indication.
2. A short frame exists if there are less than 25 bits between the flags. Short frames are ignored by the receiver and nothing is written into the receive FIFO.
3. Packets which are at least 25 bits in length but less than 32 bits (between the flags) are also invalid. In this case the data is written to the FIFO but the last byte is tagged with a 'bad packet' indication.
4. If a frame abort sequence is detected the packet is invalid. Some or all of the current packet will reside in the receive FIFO, assuming the packet length before the abort sequence was at least 26 bits long.

Frame Abort

The transmitter will abort a current packet by substituting a zero followed by seven contiguous 1s in place of the normal data. The receiver will abort upon reception of seven contiguous 1s occurring between the flags of a packet which contains at least 26 bits.

Note that should the last receive byte before the frame abort end with contiguous 1s, these are included in the seven 1s required for a receiver abort. This means that the location of the abort sequence in the receiver may occur before the location of the abort sequence in the originally transmitted packet. If this happens, then the last data written to the receive FIFO will not correspond exactly with the last byte received before the frame abort.

Interframe Time Fill and Link Channel States

When the HDLC transmitter is not sending packets it will wait in one of two states.

Interframe Time Fill: This is a continuous series of flags occurring between frames indicating that the channel is active but that no data is being sent.

Idle: An idle channel occurs when at least fifteen contiguous 1s are transmitted or received.

In both cases the transmitter will exit the wait state when data is loaded into the transmit FIFO.

Go-Ahead

A go-ahead is defined as the pattern '011111110' (contiguous 7F's) and is the occurrence of a frame abort sequence followed by a zero, outside of the boundaries of a normal packet. Being able to distinguish a proper (in packet) frame abort sequence from one occurring outside of a packet allows a higher level of signalling protocol which is not part of the HDLC specifications.

Transmitter

Following initialization and enabling, via the HTxEN bit (address 03h), the transmitter is in the Idle Channel State (Mark Idle). Interframe time fill may be selected by setting the Mark Idle bit (address 03h) high. The transmitter remains in its programmed state until data is written to the Tx FIFO. The transmitter will then proceed as follows:

1) If the transmitter is in the idle state the present byte of ones will be completely transmitted before the opening flag and packet data is sent.
2) If the transmitter is in the interframe time fill state the flag currently being transmitted will be used as the opening flag followed by the packet data.

To assist in loading multiple packets into the transmit FIFO the last packet byte is tagged with either EOP (to indicate the end of the current packet) or FA. Control Register 1 (address 03h) bits EOP (end of packet) and FA (frame abort) are set before writing the last packet byte to the Tx FIFO. The act of loading the last packet byte will then automatically reset the EOP and FA bits. Tx FIFO bytes are continuously transmitted until the FIFO is empty, by which time an EOP or FA tag should have been encountered by the transmitter.

After the last bit of the EOP byte has been transmitted a 16 bit FCS is sent followed by a closing flag. When multiple packets of data are loaded into the Tx FIFO only one flag is sent between packets.

When the transmitter encounters a byte tagged FA then a frame abort sequence is sent instead of the tagged byte. All bytes previous to but not including the tagged byte are sent.

The transmitter returns to its programmed wait state after concluding the transmission of EOP or FA if the Tx FIFO is empty.

Transmit FIFO Status

The transmit FIFO is 19 bytes deep (address 02h). As data is loaded into (from the microport) and extracted from (via the serial port) the Tx FIFO the present 'fill state' can be monitored using the Txstat1 and Txstat2 bits found in the HDLC Status Register (address 04h). These states are encoded as shown in Table 2. Note that the FIFO emptying threshold, where an interrupt (TxFL if unmasked) will occur, can be set to a low level 4 (default) or to a high level 14 by the Fltx bit in the HDLC Control Register 2 (address 05h).

A Tx FIFO underrun occurs if the Tx FIFO empties without the occurrence of an EOP or FA tagged byte. A frame abort sequence is automatically transmitted under this condition.

Transmit Interrupts

The HDLC Interrupt Enable Register (address 06h) is used to select (unmask) only those interrupts which are deemed important to the microprocessor. After a $\overline{\text{PWRST}}$ or software RST all enable bits will be cleared causing all interrupts to be masked.

All selected interrupt events will cause the $\overline{\text{IRQ}}$ pin to become active. Unselected interrupt events will not cause $\overline{\text{IRQ}}$ to become active however, the event will still be represented by the appropriate bit in the HDLC Interrupt Status Register (address 07h). This register must be read after receiving an $\overline{\text{IRQ}}$ or may be polled at any time. The $\overline{\text{IRQ}}$ output pin is reset coincident with the first SCLK falling edge following a Command/Address byte which indicates a microport read of address 07h. Since all interrupts are generated by the occurrence of an HDLC event (i.e., a transition), this register informs that an event has occurred but does not guarantee that it is still valid. To determine current validity the HDLC Status Register (address 04h) should be read. Due to the asynchronous nature of the interrupts an interrupt occurring during a read of the Interrupt Status register will be held until the read cycle is over, unless it is an interrupt which is already valid.

There are three interrupts associated with the transmitter.

TEOP Transmit End Of Packet:

Set when the transmitter has finished sending the closing flag of a packet or after an abort sequence has been completed.

TxFL Transmit FIFO Low:

Set when a transition from 5 to 4 bytes in the Tx FIFO has occurred. This is an early warning to the microprocessor that the FIFO is emptying and should be serviced before it empties completely; a condition which will result in a transmit underrun unless an EOP or FA byte has been written to the FIFO. By setting the FItx bit (address 05h) high the FIFO emptying condition will occur at the transition from 15 to 14 bytes. This will allow the microport more time to react to this interrupt condition.

Txunder Transmit underrun:

Set when the Tx FIFO empties without the occurrence of an EOP or FA tagged byte. A frame abort sequence is automatically transmitted under this condition. Note that this register bit position is shared with the frame abort (FA) interrupt (see receive interrupts). For this bit to reflect Txunder the Intsel bit in Control Register 2 (address 05h) must be set high.

Disabling, Reset, Transparent Operation and CRC

Disabling the transmitter via the HTxEn bit will occur after the current packet is completely transmitted. The status and Interrupt registers may still be read and the Tx FIFO and control registers written while the transmitter is disabled.

The Tx FIFO may be reset by setting the Txfrst bit in the HDLC Control Register 2 (address 05h). The HDLC Status Register will identify the Tx FIFO as being empty although the actual data in the FIFO will not be reset. Txfrst will be cleared by the next write to the Tx FIFO.

Transparent data may be sent by setting the TRANS bit (address 03h) high. The transmitter will no longer generate the flag, abort and idle sequences, nor will it insert zeros and append the FCS. Data will still be transmitted LSB first. If there is no data in the Tx FIFO or the Tx FIFO empties the last byte transmitted will be repetitively sent until new data is presented to the FIFO. It will take typically two ST-BUS frames, after writing TRANS, before this mode begins. Note that CH_0EN must also be set.

Transmission of the FCS field CRC may be inhibited using the Tcrci (Transmit Crc Inhibit) bit at address 05h. While this bit is set the opening flag followed by the data fields and closing flag is transmitted, including zero insertion, but the calculated CRC is not. This allows the processor to insert the CRC as part of the data field. This usage is for V.120 terminal adaptation for synchronous protocol sensitive UI frames.

Receiver

Following initialization and enabling, via the HRxEN bit at address 03h, the receiver begins clocking in serial data checking for flags (0111 1110), go-aheads (0111 1111 0), and idle channel states (at least fifteen contiguous ones). Upon detecting a flag the receiver synchronizes itself to the data stream and begins calculating the CRC. If the packet length, between the flags and after zero deletion, is less than 25 bits the packet is ignored and nothing is written to the Rx FIFO. If the packet length, after zero deletion, is between 25 and 31 bits a last byte, bad packet indication is written into the Rx FIFO.

Idle Channel

When the receiver detects at least 15 contiguous ones it declares an idle channel condition exists and sets the IdleChan bit in the HDLC status register high (address 04h). This bit remains set until the received condition changes.

Address Recognition

When Adrec (HDLC Control Register 1, address 03h) is low all valid received packets, regardless of the address field information, are loaded into the Rx FIFO.

If address recognition is required, Receive Address Recognition Registers 1 and/or 2 (addresses 00h and 01h respectively) are loaded with the desired address comparison information, the Adrec bit is set high and A1EN and A2EN are set as required. Bit 0 (A1EN and A2EN) of both recognition registers is used as an enable for that byte. When either of these bits are low their respective address mask information is ignored. In this way either or both of the first two received bytes can be compared to the expected mask values. Only those packets passing the appropriate comparison test will be loaded into the Rx FIFO. The appropriate comparison test (single/dual byte address, All-call) is defined by the logic state of bit 0 of the first byte received after the opening flag.

Bit 0 of the first received address byte (address extension bit) is monitored to determine if a single or dual byte address is being received.

1. If the address extension bit is 1 then a single byte address is being received. If A1EN is high the stored bit mask (Adr11 - Adr16 and sometimes Adr10) is compared to the received first address byte. Any packet failing this address comparison will not be stored in the Rx FIFO except for the All-call condition. A1EN must be set high for a single-byte All-call (11111111) address to be recognized. The second mask byte is ignored. Seven bits of address comparison may be realized for single byte recognition by setting the SEVEN bit (address 05h) high. This mode will then include Adr10 as part of the mask information. The first received byte must also have bit 0 set to a 1 indicating single byte addressing.

2. If the address extension bit is 0 then a two byte address is being received and the six most significant bits of the first received byte are compared. The seven most significant bits of the second received byte are compared (Adr20 - Adr26, note A2EN must be set high also). Any packet failing this address comparison will not be stored in the Rx FIFO. An All-call condition (1111111x) is also monitored for in the second received address byte and, if found, the first and second byte masks are ignored (not compared with the mask byte). Packets addressed with All-call are written into the Rx FIFO.

In CCITT Q.921 parlance the Adr11 - Adr16 bits are defined as Sapi0 - Sapi5 (Service Access Point Identifier n). Adr10 is defined as C/R (Command/ Response). Adr20 - Adr26 are defined as Tei0 - Tei6 (Terminal Endpoint Identifier n).

Receive Byte Status

As each received packet byte is written into the Rx FIFO two bits are appended to indicate the status of that byte. As these bytes are read from the Rx FIFO the status bits are made available to the microprocessor in the HDLC Status Register (address 04h) as RxBS1 and RxBS2. Since the information contained in RxBS1 & RxBS2 pertains to the byte about to be read from the Rx FIFO, it is important that this information be read before reading the data byte from the FIFO. RxBS1 and RxBS2 are encoded as shown in Table 2. A good packet indication means a good FCS and no frame abort whereas a bad packet indication means either an incorrect FCS or a frame abort occurred.

Receive FIFO Status

The receive FIFO is 19 bytes deep (address 02h). As data is loaded into (from the serial port) and extracted from (via the microport) the Rx FIFO the present 'fill state' can be monitored using the Rxstat1 and Rxstat2 bits found in the HDLC Status Register (address 04h). These states are encoded as shown in Table 2. Note that the FIFO filling threshold, where an interrupt (RxFf if unmasked) will occur, can be set to a high level 15 (default) or to a low level 5 by the Flrx bit in the HDLC Control Register 2 (address 05h).

In the case of an Rx FIFO overflow, an attempt by the receiver to write data into an already full FIFO, the receiver is disabled causing it to stop writing to the Rx FIFO. The remainder of the current receive packet is therefore ignored. The receiver will be re-enabled when the next flag is detected but will overflow again if the Rx FIFO level has not been reduced to less than full. If two 'first byte' (RxBS1 and RxBS2) conditions are observed in the FIFO without an intervening 'last byte' then an overflow occurred for the first packet.

Receive Interrupts

The HDLC Interrupt Enable Register (address 06h) is used to select (unmask) only those interrupts which are deemed important to the microprocessor. After a $\overline{\text{PWRST}}$ or software RST all enable bits will be cleared causing all interrupts to be masked.

All selected interrupt events will cause the $\overline{\text{IRQ}}$ pin to become active. Unselected interrupt events will not cause $\overline{\text{IRQ}}$ to become active however, the event will still be represented by the appropriate bit in the HDLC Interrupt Status Register (address 07h). This register must be read after receiving an $\overline{\text{IRQ}}$ or may be polled at any time. The IRQ output pin is reset coincident with the first SCLK falling edge following a Command/Address byte which indicates a microport read of address 07h. Since all interrupts are generated by the occurrence of an HDLC event (i.e., a transition), this register informs that an event has occurred but does not guarantee that it is still valid. To determine current validity the HDLC Status Register (address 04h) should be read. Due to the asynchronous nature of the interrupts an interrupt occurring during a read of the Interrupt Status register will be held until the read cycle is over, unless it is an interrupt which is already valid.

There are six interrupts associated with the receiver.

GA Go Ahead:
Set when a go-ahead pattern (011111110) has been detected by the receiver.

EOPD End Of Packet Detect:
Set when an end of packet byte has been written into the Rx FIFO by the receiver. This event may be due to receiving a closing flag, an abort sequence or an invalid packet.

EopR End of packet Read:
Set when the next byte to be read from the Rx FIFO is the last byte of a packet or when a read to an empty Rx FIFO has occurred.

FA Frame Abort:
Set when a frame abort sequence is received during packet reception. The aborted packet must contain a minimum of 26 bits for the FA sequence to be recognized. Note that this register bit position is shared with the transmitter under-run (Txunder) interrupt (see transmit interrupts). For this bit to reflect FA the Intsel bit in Control Register 2 (address 05h) must be set low.

RxFf - Receive FIFO filling:
Set when a transition from 14 to 15 bytes in the Rx FIFO has occurred. This is an early warning to the microprocessor that the FIFO is filling and should be serviced before it becomes completely full; a condition which may result in a receive overflow condition. By setting the Flrx bit (address 05h) high the FIFO filling condition will occur when a transition from 4 to 5 bytes occurs. This will allow the microport more time to react to this interrupt condition.

RxOvfl - Receive FIFO Overflow:
Set when the receiver attempts to write data into an already full Rx FIFO. Under this condition the HDLC will disable the receiver until a new flag is detected. See also Receive FIFO Status.

Disabling, Reset and Transparent Operation

Disabling of the receiver via the HRxEn bit will occur after the current packet is completely loaded into the Rx FIFO. Disabling can occur during packet reception if no bytes have been written to the Rx FIFO yet. The Rx FIFO, status and Interrupt registers may still be read and control registers written while the receiver is disabled. Note that the receiver requires the reception of a flag before processing a packet, thus if the receiver is enabled in the middle of an incoming packet it will ignore that packet and wait for the next complete one.

The Rx FIFO may be reset by setting the Rxfrst bit in the HDLC Control Register 2 (address 05h). The receiver will be disabled until reception of the next flag. The Status Register will identify the Rx FIFO as being empty although the actual data in the FIFO will not be reset. Rxfrst will be cleared by the reception of the next received flag pattern.

Data may be received transparently by setting the TRANS bit (address 03h) high. Timing control bit CH_0EN must also be set. The receiver will disable protocol functions such as flag/abort/go-ahead/idle detection, zero deletion, CRC calculation and address comparison. Data is shifted into the Rx FIFO in a byte-wide format. In transparent mode when an Rx FIFO overflow condition occurs the receiver will continue to write data into the Rx FIFO, overwriting the last byte. The overflow interrupt condition can only be detected again if the Rx FIFO is reset (Rxfrst bit at address 05h) since normally the overflow condition is cleared by the reception of the next flag and transparent data is unlikely to emulate a flag. Also, the Rxfrst bit itself will have to be reset by writing it low since it is usually reset automatically by the occurrence of the next flag.

RxBS2, RxBS1 — Are status bits from the Rx FIFO.

RxBS2	RxBS1	Byte status
1	1	last byte (bad packet)
0	1	first byte
1	0	last byte (good packet)
0	0	packet byte

Note - If two consecutive first byte signals are received without an intervening last byte, then an overflow has occurred and the first packet (or packets) are bad. A bad packet indicates that either a frame abort had occurred or the FCS did not match.

- On power-up these bits are in an indeterminate state until the first byte is written to Rx FIFO.

Txstat2, Txstat1 — These two bits are encoded to indicate the present state of Tx FIFO. This is an asynchronous event.

Txstat2	Txstat1	Tx FIFO Status
0	0	TxFULL
0	1	5 OR MORE BYTES (15 if Fltx set)
1	1	4 OR LESS BYTES (14 if Fltx set)
1	0	TxEMPTY

Rxstat2, Rxstat1 — These two bits are encoded to indicate the present state of Rx FIFO. This is an asynchronous event.

Rxstat2	Rxstat1	Rx FIFO Status
0	0	RxEMPTY
0	1	14 OR LESS BYTES (4 if Flrx set)
1	1	15 OR MORE BYTES (5 if Flrx set)
1	0	RxOVERFLOW EXISTS

Table 2 - HDLC Status Bits

Transducer Interfaces

Four standard telephony transducer interfaces are provided by the HPhone-II. These are:

- The handset microphone inputs (transmitter), pins M+/M- and the speakerphone microphone inputs, pins MIC+/MIC-. The transmit path is muted/not-muted by the MIC EN control bit. Selection of which input pair is to be routed to the transmit filter amplifier is acomplished by the MIC/HNSTMIC control bit. Both of these reside in the Transducer Control Register (address 0Eh). The nominal transmit path gain may be adjusted to either 6.1 dB (suggested for μ-Law) or 15.4 dB (suggested for A-Law). Control of this gain is provided by the MICA/u control bit (General Control Register, address 0Fh). This gain adjustment is in addition to the programmable gain provided by the transmit filter and DSP.

- The handset speaker outputs (receiver), pins HSPKR+/HSPKR-. This internally compensated, fully differential output driver is capable of driving the load shown in Figure 5. This output is enabled/disabled by the HSSPKR EN bit residing in the Transducer Control Register (address 0Eh). The nominal handset receive path gain may be adjusted to either -12.3 dB (suggested for μ-Law) or -9.7 dB (suggested for A-Law). Control of this gain is provided by the RxA/u control bit (General Control Register, address 0Fh). This gain adjustment is in addition to the programmable gain provided by the receive filter and DSP.
- The loudspeaker outputs, pins SPKR+/SPKR-. This internally compensated, fully differential output driver is capable of directlydriving 6.5 vpp into a 40 ohm load. This output is enabled/disabled by the SPKR EN bit residing in the Transducer Control Register (address 0Eh). The nominal gain for this amplifier is 0.2 dB.

C-Channel

Access to the internal control and status registers of Zarlink basic rate, layer 1, transceivers is through the ST-BUS Control Channel (C-Channel), since direct microport access is not usually provided, except in the case of the SNIC (MT8930). The HPhone-II provides asynchronous microport access to the ST-BUS C-Channel information on both DSTo and DSTi via a double-buffered read/write register (address 14h). Data written to this address is transmitted on the C-Channel every frame when enabled by CH_1EN (see ST-BUS/Timing Control).

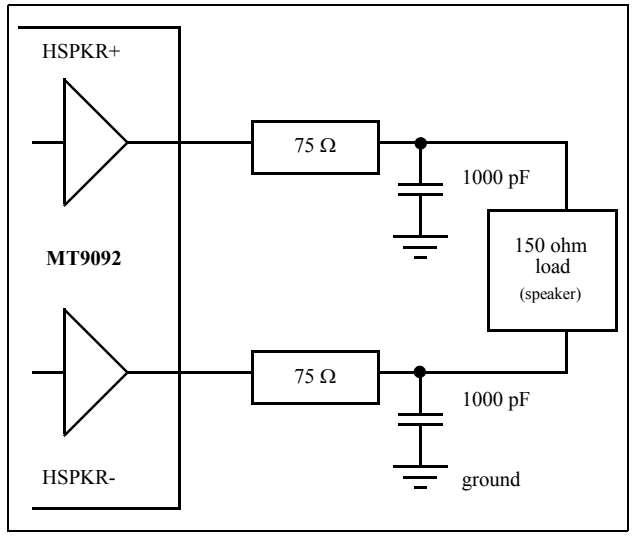

Figure 5 - Handset Speaker Driver

LCD

A twelve segment, non-multiplexed, LCD display controller is provided for easy implementation of various set status and call progress indicators. The twelve output pins (S_n) are used in conjunction with 12 segment control bits, located in LCD Segment Enable Registers 1&2 (addresses 12h and 13h), and the BackPlane output pin (BP) to control the on/off state of each segment individually.

The BP pin drives a continuous 62.5 Hz, 50% duty cycle squarewave output signal. An individual segment is controlled via the phase relationship of its segment driver output pin with respect to the backplane, or common, driver output. Each of the twelve Segment Enable bits corresponds to a segment output pin. The waveform at each segment pin is in-phase with the BP waveform when its control bit is set to logic zero (segment off) and is out-of-phase with the BP waveform when its control bit is set to a logic high (segment on). Refer to the LCD Driver Characteristics for pin loading information.

Microport

A serial microport, compatible with Intel MCS-51 (mode 0) specifications, provides access to all HPhone-II internal read and write registers. This microport consists of three pins; a half-duplex transmit/receive data pin (DATA1), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK).

On power-up reset ($\overline{PWRST}$) or with a software reset (RST), the DATA1 pin becomes a bidirectional (transmit/receive) serial port while the DATA2 pin is internally disconnected and tri-stated.

All data transfers through the microport are two-byte transfers requiring the transmission of a Command/Address byte followed by the data byte written or read from the addressed register. $\overline{CS}$ must remain asserted for the duration of this two-byte transfer. As shown in Figure 6, the falling edge of $\overline{CS}$ indicates to the HPhone-II that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and of what address. The next 8 clock cycles are used to transfer the data byte between the HPhone-II and the microcontroller. At the end of the two-byte transfer $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the output driver of DATA1 which will remain tri-stated as long as $\overline{CS}$ is high.

Receive data is sampled and transmit data is made available on DATA1 concurrent with the falling edge of SCLK.

An open-drain interrupt request ($\overline{IRQ}$) output provides a method for interrupting the microcontroller when an unmasked HDLC event occurs within the HPhone-II. $\overline{IRQ}$ remains active until the HDLC Interrupt Status Register is read or a (hardware/software) reset occurs. More detail is provided in the section pertaining to the HDLC functional block.

Lastly, provision is made to seperate the transmit and receive data streams onto two individual pins. This control is given by the DATASEL pin in the General Control Register (address 0Fh). Setting DATASEL logic high will cause DATA1 to become the data receive pin and DATA2 to become the data transmit pin. Only the signal paths are altered by DATASEL; internal timing remains the same in both cases. Tri-stating on DATA2 follows $\overline{CS}$ as it does on DATA1 when DATASEL is logic low. Use of the DATASEL bit is intended to help in adapting Motorola (SPI) and National Semiconductor (Micro-wire) microcontrollers to the HPhone-II. Note that whereas Intel processor serial ports transmit data LSB first other processor serial ports, including Motorola, transmit data MSB first. It is the responsibility of the microcontroller to provide LSB first data to the HPhone-II.

ST-BUS/Timing Control

A serial link is required for the transport of data between the HPhone-II and the external digital transmission device. The HPhone-II utilizes the ST-BUS architecture defined by Zarlink Semiconductor. Refer to Zarlink Application Note MSAN-126. The HPhone-II ST-BUS consists of output and input serial data streams, DSTo and DSTi respectively, a synchronous clock signal $\overline{C4i}$, and a framing pulse $\overline{F0i}$.

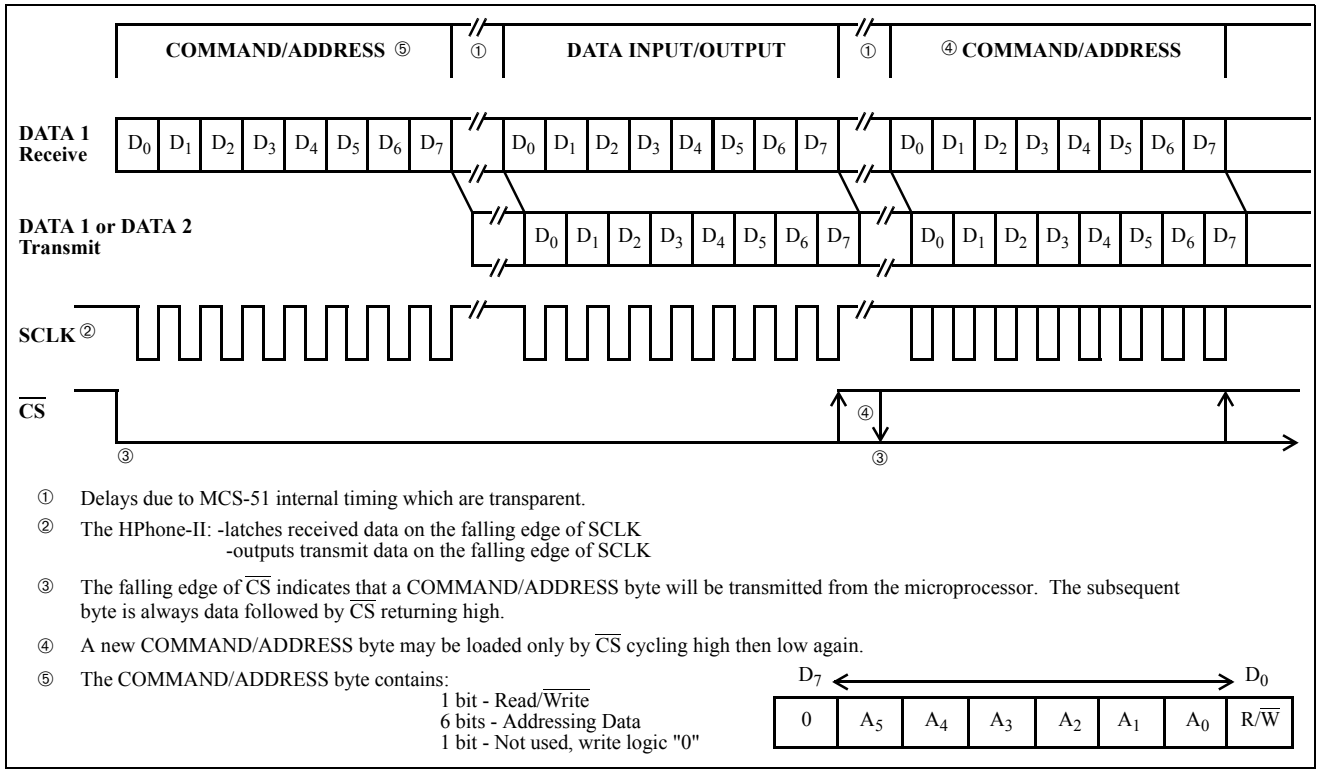

Figure 6 - Serial Port Relative Timing

The data streams operate at 2048 kb/s and are Time Division Multiplexed into 32 identical channels of 64 kb/s bandwidth. Frame Pulse (a 244 nSec low going pulse) is used to parse the continuous serial data streams into the 32 channel TDM frames. Each frame has a 125 μSecond period translating into an 8 kHz frame rate. Valid frame pulse occurs when F0i is logic low coincident with a falling edge of C4i. C4i has a frequency (4096 MHz) which is twice the data rate. This clock is used to sample the data at the 3/4 bit-cell position on DSTi and to make data available on DSTo at the start of the bit-cell. C4i is also used to clock the HPhone-II internal functions (i.e., DSP, Filter/CODEC, HDLC) and to provide the channel timing requirements.

The HPhone-II uses only the first 4 channels of the 32 channel frame. These channels are always defined, beginning with the first channel after frame pulse, as shown in Figure 7 (DSTi and DSTo channel assignments). Channels are enabled independantly by the four control bits Ch_0En -Ch_3En residing in the Timing Control Register (address15h).

Ch_0EN - D-Channel

Channel 0 conveys the D-Channel HDLC information. Since this function is dedicated to 16 kb/s operation, only the first two bits (LSB's) of the octet are required; the remaining six bits of the D-Channel octet carry no information and are tri-stated. When CH_0EN is high, HDLC data is transmitted on DSTo. When low, DSTo is forced to logic 0 for the two least significant bit positions. Incoming DSTi data is always routed to the HDLC block regardless of this control bit's logic state.

Ch_1EN - C-Channel

Channel 1 conveys the control/status information for Zarlink's layer 1 transceiver. The full 64 kb/s bandwidth is available and is assigned according to which transceiver is being used. Consult the data sheet for the selected transceiver for its bit definitions and order of bit transfer. When this bit is high register data is transmitted on DSTo. When low, this timeslot is tri-stated on DSTo. Receive C-Channel data (DSTi) is always routed to the register regardless of this control bit's logic state. C-channel data is transferred on the ST-BUS MSB first by the HPhone-II.

Ch_2EN and Ch_3EN - B1-Channel and B2-Channel

Channels 2 and 3 are the B1 and B2 channels, respectively. These bits (Ch_2EN and Ch_3EN) are used to enable the PCM channels from/to the HPhone-II as required.

Transmit PCM on DSTo

When high, PCM from the Filter/CODEC and DSP is transmitted on DSTo in the selected ST-BUS channel. When low, DSTo is forced to logic 0 for the corresponding timeslot. If both Ch_2EN and Ch_3EN are enabled, default is to channel 2.

Receive PCM from DSTi

When high, PCM from DSTi is routed to the DSP and Filter/CODEC in the associated channel. If both Ch_2EN and Ch_3EN are enabled the default is to channel 2.

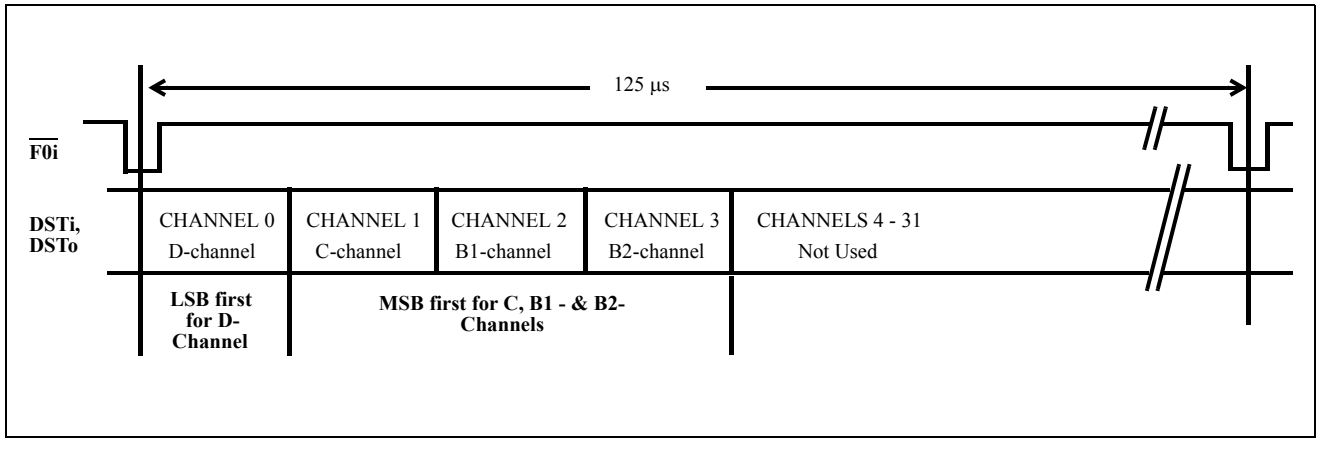

Figure 7 - ST-BUS Channel Assignment

New Call Tone

The New Call Tone Generator produces a frequency shifted square-wave used to toggle the speaker driver outputs. This is intended for use where a ringing signal is required concurrently with an already established voice conversation in the handset.

Programming of the DSP for New Call generator is exactly as is done for the tone ringer micro-program except that the OPT bit (DSP Control Register, address 1Eh) is set high. In this mode the DSP does not produce a frequency shifted squarewave output to the filter CODEC section. Instead the DSP uses the contents of the tone coefficient registers, along with the tone warble rate register, to produce a gated squarewave control signal output which toggles between the programmed frequencies. This control signal is routed to the New Call Tone block when the NCT EN control bit is set (General Control Register, address 0Fh). NCT EN also enables a separate gain control block, for controlling the loudness of the generated ringing signal. With the gain control block set to 0 dB the output is at maximum or 6 volts p-p. Attenuation of the applied signal, in three steps of 8 dB, provide the four settings for New Call tone (0, -8, -16, -24 dB). The NCT gain bits ($NCTG_0$-$NCTG_1$) reside in the FCODEC Gain Control Register 2 (address 0Bh).

Watchdog

To maintain program integrity an on-chip watchdog timer is provided for connection to the microcontroller reset pin. The watchdog output WD (pin 17) goes high while the HPhone-II is held in reset via the $\overline{\text{PWRST}}$ (pin 6). Release of $\overline{\text{PWRST}}$ will cause WD to return low immediately and will also start the watchdog timer. The watchdog timer is clocked on the falling edge of $\overline{\text{F0i}}$ and requires only this input, along with V_{DD}, for operation.

If the watchdog reset word is written to the watchdog register (address 11h) after $\overline{\text{PWRST}}$ is released, but before the timeout period (T=512 mSec) expires, a reset of the timer results and WD will remain low. Thereafter, if the reset word is loaded correctly at intervals less than 'T' then WD will continue low. The first break from this routine, in which the watchdog register is not written to within the correct interval or it is written to with incorrect data, will result in a high going WD output after the current interval 'T' expires. WD will then toggle at this rate until the watchdog register is again written to correctly.

5-BIT WATCHDOG RESET WORD

			W4	**W3**	**W2**	**W1**	**W0**
X	X	X	0	1	0	1	0

x=don’t care

Test Loops

Detail LBio and LBoi Loopback Register (address 16h)

LBio Setting this bit causes data on DSTi to be looped back to DSTo directly at the pins. The appropriate channel enables Ch_0EN -Ch_3EN must also be set.

LBoi Setting this bit causes data on DSTo to be looped back to DSTi directly at the pins.

HPhone-II Register Map

Address (Hex)	WRITE	READ
00	HDLC ADDRESS RECOGNITION REGISTER 1	VERIFY
01	HDLC ADDRESS RECOGNITION REGISTER 2	VERIFY
02	HDLC TRANSMIT FIFO	HDLC RECEIVE FIFO
03	HDLC CONTROL REGISTER 1	VERIFY
04	NOT USED	HDLC STATUS REGISTER
05	HDLC CONTROL REGISTER 2	VERIFY
06	HDLC INTERRUPT ENABLE REGISTER	VERIFY
07	NOT USED	HDLC INTERRUPT STATUS REGISTER
08	RESERVED	RESERVED
09	RESERVED	RESERVED
0A	FCODEC GAIN CONTROL REGISTER 1	VERIFY
0B	FCODEC GAIN CONTROL REGISTER 2	VERIFY
0C	RESERVED	RESERVED
0D	RESERVED	RESERVED
0E	TRANSDUCER CONTROL REGISTER	VERIFY
0F	GENERAL CONTROL REGISTER	VERIFY
10	RESERVED	RESERVED
11	WATCHDOG REGISTER	NOT USED
12	LCD SEGMENT ENABLE REGISTER 1	VERIFY
13	LCD SEGMENT ENABLE REGISTER 2	VERIFY
14	C-CHANNEL REGISTER (to DSTo)	C-CHANNEL REGISTER (from DSTi)
15	TIMING CONTROL REGISTER	VERIFY
16	LOOP-BACK REGISTER	VERIFY
17-1C	RESERVED	RESERVED
1D	RECEIVE GAIN CONTROL REGISTER	VERIFY
1E	DSP CONTROL REGISTER	VERIFY
1F	RESERVED	RESERVED
20	TRANSMIT AUDIO GAIN REGISTER	VERIFY
21	TRANSMIT DTMF GAIN REGISTER	VERIFY
22	RESERVED	RESERVED
23	TONE COEFFICIENT REGISTER 1	VERIFY
24	TONE COEFFICIENT REGISTER 2	VERIFY
25	RESERVED	RESERVED
26	TONE RINGER WARBLE RATE REGISTER	VERIFY
27-3F	RESERVED	RESERVED

Register Summary

This section contains a complete listing of the HPhone-II register addresses, the control/status bit mapping associated with each register and a definition of the function of each control/status bit. The Register Summary may be used for future reference to review each of the control/status bit definitions without the need to locate them in the text of the functional block descriptions.

HDLC Address Recognition Register 1 ADDRESS = 00h WRITE/READ VERIFY

Power Reset Value
0000 0000

Adr16	Adr15	Adr14	Adr13	Adr12	Adr11	Adr10	A1EN
7	6	5	4	3	2	1	0

Adr 16-11 A six bit mask used to interrogate the first byte of the received address. Adr16 is MSB. In the Q.921 specification these bits are defined to be Sapi5-0.

Adr 10 This bit is used in address comparison if a seven bit address is being checked for (Control bit Seven of Control Register 2 is set). In the Q.921 specification this bit is defined to be C/R (Command/Response).

A1EN When this bit is high, this six (or seven) bit mask is used in address comparison of the first address byte. If address recognition is enabled, any packet failing the address comparison will not be stored in the RX FIFO. A1EN must be high for All-call (1111111) address recognition for single byte address. When this bit is low, this bit mask is ignored in address comparison.

HDLC Address Recognition Register 2 ADDRESS = 01h WRITE/READ VERIFY

Power Reset Value
0000 0000

Adr26	Adr25	Adr24	Adr23	Adr22	Adr21	Adr20	A2EN
7	6	5	4	3	2	1	0

Adr 26-20 A seven bit mask used to interrogate the second byte of the received address. Adr26 is MSB. This mask is ignored (as well as first byte mask) if an All call address (1111111) is received. In the Q.921 specification these bits are defined to be Tei6-0.

A2EN When this bit is high this seven bit mask is used in address comparison of the second address byte. If address recognition is enabled, any packet failing the address comparison will not be stored in the RX FIFO. A2EN must be high for All-call address recognition. When this bit is low, this bit mask is ignored in address comparison.

HDLC Transmit/Receive FIFO Register ADDRESS = 02h WRITE/READ

Power Reset Value
Not Applicable

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

The Transmitter FIFO is 19 words deep. Each word consists of 8 bits of data from the internal data bus and 2 status bits from CONTROL Register 1 (EOP and FA). If there is data in the Tx FIFO then the lowest data byte in it is loaded into an output shift register for transmission, and the remaining data shifts down by one word position (Tx FIFO read). A write to a full Tx FIFO will update the top byte only.

The receiver FIFO is 19 words deep. During a receiver write, the last 8 bits of a shift register buffer and two status bits are loaded into Rx FIFO. Data shifts down into the Rx FIFO following a microprocessor read. A write to a full RX FIFO will not update the FIFO.

HDLC Control Register 1 ADDRESS = 03h WRITE/READ VERIFY

Power Reset Value
0000 0000

Adrec	HRxEN	HTxEN	EOP	FA	Mark Idle	Trans	-
7	6	5	4	3	2	1	0

Adrec When high this bit will enable address recognition. This forces the receiver to recognize only those packets having the unique address as programmed in the Receive Address Recognition Registers or if the address is an All-Call address. When low, all packets are recognized.

HRxEN When low this bit will disable the HDLC receiver. The receiver will disable after the rest of the packet presently being received is finished. When high the receiver will be immediately enabled (depending on the state of CHoEN) and will begin searching for flags, Go-aheads etc.

HTxEN When low this bit will disable the HDLC transmitter. The transmitter will disable after the completion of the packet presently being transmitted. When high the transmitter will be immediately enabled (depending on the state of CHoEN) and will begin transmitting data, if any, or go to a Mark idle or Interframe time fill state.

EOP Forms a tag on the next byte written to the Tx FIFO and when set will indicate an EOP byte to the transmitter which will transmit an FCS following this byte. This facilitates loading of multiple packets into Tx FIFO. This bit is reset automatically after a write to the Tx FIFO occurs.

FA Forms a tag on the next byte written to Tx FIFO and when set will indicate to the transmitter that it should abort the packet in which that byte is being transmitted. This bit is reset automatically after a write to the Tx FIFO.

Mark Idle When low, the transmitter will be in an idle state. When high it is in an Interframe time fill state. These two states will only occur when the Tx FIFO is empty.

Trans When high this bit will enable transparent mode. The HDLC will perform the serial-to-parallel and parallel-to-serial conversion without inserting or deleting zeros. No CRC bytes are sent or monitored nor are flags, aborts or Go-aheads. No address recognition is monitored. The receiver or transmitter must be enabled through Control Register 1 as well as setting CH_0EN.

HDLC Status Register ADDRESS = 04h READ

Intgen	Idle Chan	RxBS2	RxBS1	Txstat 2	Txstat 1	Rxstat 2	Rxstat 1
7	6	5	4	3	2	1	0

Power Reset Value
00XX 1000

Intgen Is set to a 1 when an interrupt (in conjunction with the Interrupt Mask Register) has been generated by the HDLC. This is an asynchronous event. It is reset when the Interrupt Register is read.

Idle Chan Is set to a 1 when an Idle Channel state (15 or more ones) has been detected by the receiver. This is an asynchronous event. Status becomes valid after first 15 bits or the first zero bit received.

RxBS2, RxBS1 Indicates the status of the next byte to be read from the Rx FIFO.

RxBS2	RxBS1	Byte status
1	1	last byte (bad packet)
0	1	first byte
1	0	last byte (good packet)
0	0	packet byte

Note - If two consecutive first byte signals are received without an intervening last byte, then an overflow has occurred and the first packet (or packets) are bad. A bad packet indicates that either a frame abort has occurred or the FCS did not match.

- On power-up these bits are in an indeterminate state until the first byte is written to Rx FIFO.

Txstat2, Txstat1 These two bits are encoded to indicate the present state of Tx FIFO. This is an asynchronous event.

Txstat2	Txstat1	Tx FIFO Status
0	0	TxFULL
0	1	5 OR MORE BYTES (15 if Fltx set)
1	1	4 OR LESS BYTES (14 if Fltx set)
1	0	TxEMPTY

Rxstat2, Rxstat1 These two bits are encoded to indicate the present state of Rx FIFO. This is an asynchronous event.

Rxstat2	Rxstat1	Rx FIFO Status
0	0	RxEMPTY
0	1	14 OR LESS BYTES (4 if Flrx set)
1	1	15 OR MORE BYTES (5 if Flrx set)
1	0	RxOVERFLOW EXISTS

Note: Bits marked "-" are reserved bits and should be written with logic "0".