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MT93L04

128-Channel Voice Echo Canceller

Data Sheet

January 2006

Features

- **MT93L04** is a Multi-chip Module (MCM) consisting of 4 **MT93L00** devices thus providing 128 channels of 64 msec Echo Cancellation
- Each device (MT93L00) is independent of the each other
- Each device has the capability of cancelling echo over 32 channels
- The MCM module provides more than 40% board space savings
- Each device (MT93L00) can be programmed independently in any mode e.g back to back or extended delay to provide capability of cancelling different echo tails
- Each device has the same Jtag identification code

Applications

- Voice over IP network gateways
- Voice over ATM, Frame Relay
- T1/E1/J1 multichannel echo cancellation
- Wireless base stations

Ordering Information

MT93L04AG	365 Ball BGA	Trays
MT93L04AG2	365 Ball BGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Echo Canceller pools
- DCME, satellite and multiplexer systems

Description

The MT93L04 Voice Echo Canceller implements a cost effective solution for telephony voice-band echo cancellation conforming to ITU-T G.168 requirements. The MT93L04 architecture contains 64 groups of two echo cancellers (ECA and ECB) which can be configured to provide two channels of 64 milliseconds or one channel of 128 milliseconds echo cancellation. This provides 128 channels of 64 milliseconds to 64 channels of 128 milliseconds echo cancellation or any combination of the two configurations. The MT93L04 supports ITU-T G.165 and G.164 tone disable requirements.

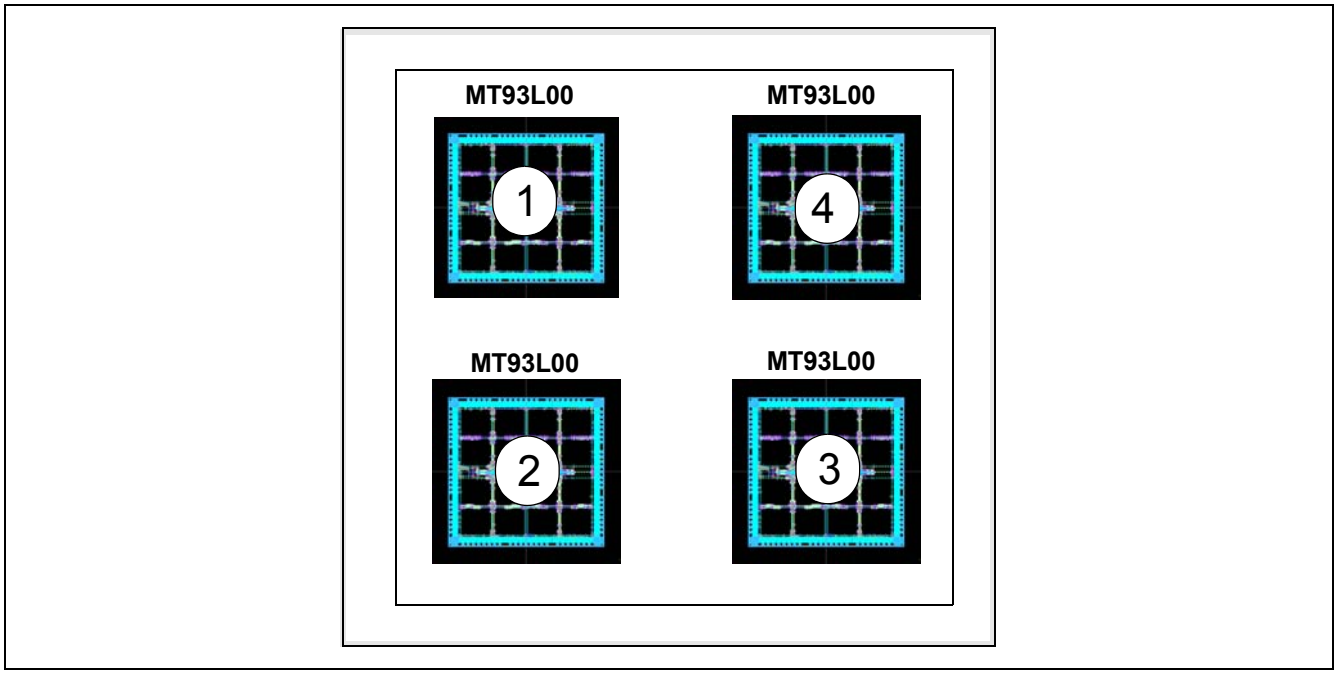


Figure 1 - MT93L04 is MULTI-CHIP Module Consisting of 4 MT93L00 Devices

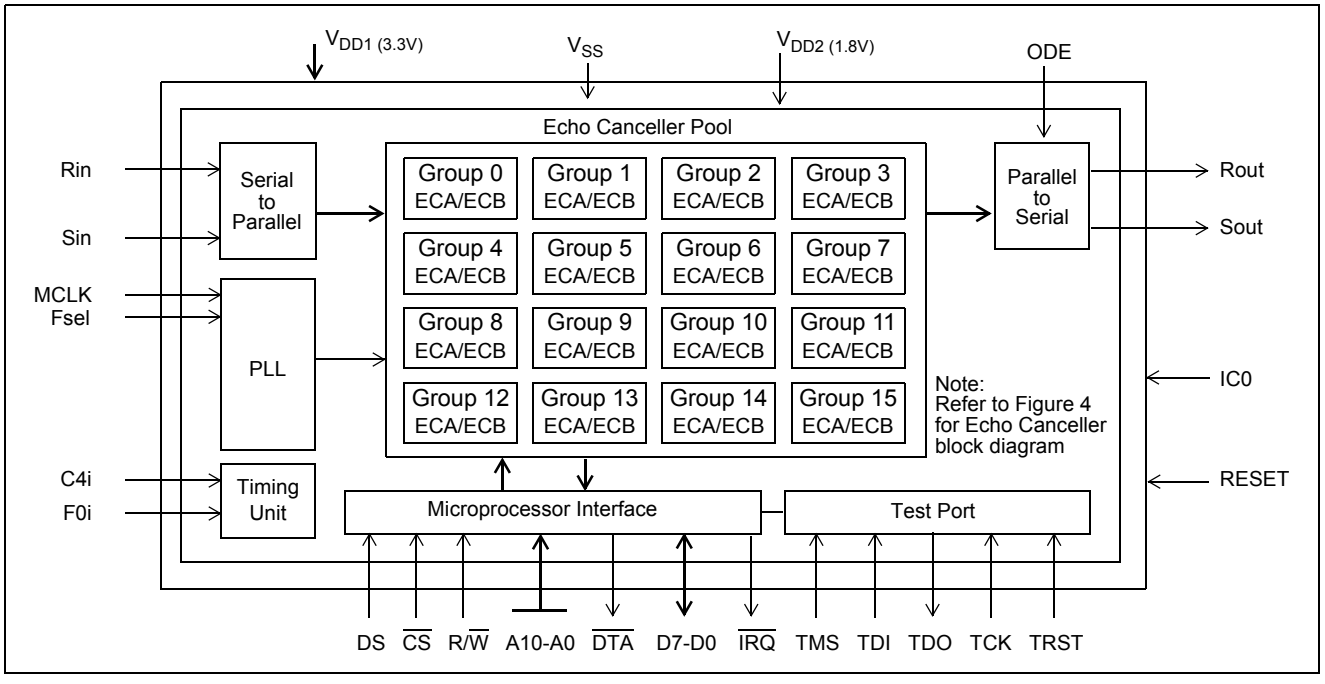
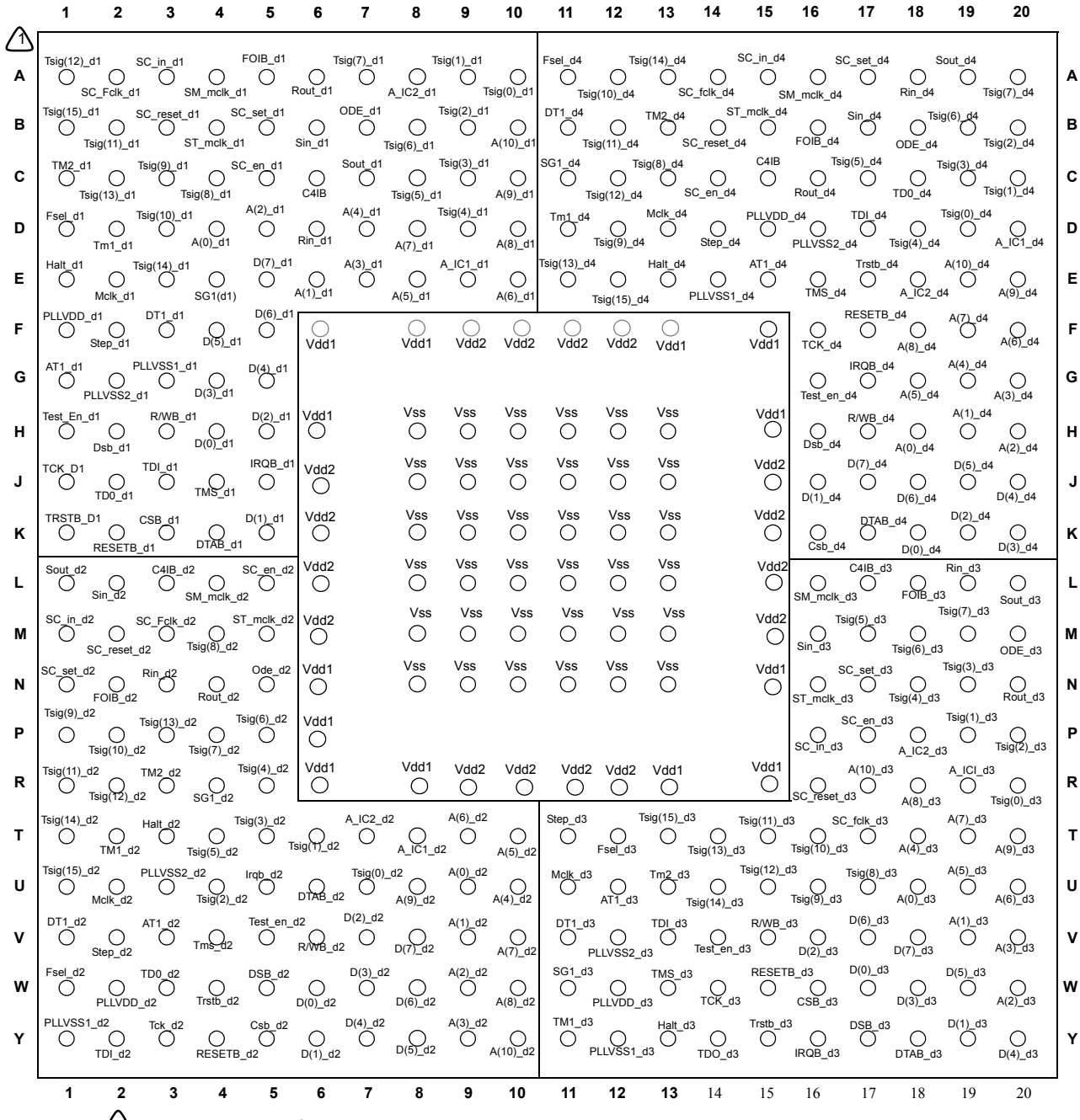


Figure 2 - Functional Block Diagram for Single MT93L00 (32 channels)

Features of Single MT93L00

- Independent multiple channels of echo cancellation; from 32 channels of 64 ms to 16 channels of 128 ms with the ability to mix channels at 128 ms or 64 ms in any combination
- Independent Power Down mode for each group of 2 channels for power management
- ITU-T G.165 and G.168 compliant
- Field proven, high quality performance
- Compatible to ST-BUS and GCI interface at 2 Mb/s serial PCM
- PCM coding, μ/A-Law ITU-T G.711 or sign magnitude
- Per channel Fax/Modem G.164 2100 Hz or G.165 2100 Hz phase reversal Tone Disable
- Per channel echo canceller parameters control
- Transparent data transfer and mute
- Fast reconvergence on echo path changes
- Non-Linear Processor with high quality subjective performance
- Protection against narrow band signal divergence
- Offset nulling of all PCM channels
- 10 MHz or 20 MHz master clock operation
- 3.3 V pads and 1.8 V Logic core operation with 5-Volt tolerant inputs
- No external memory required
- Non-multiplexed microprocessor interface
- IEEE-1149.1 (JTAG) Test Access Port



△ - A1 corner is identified by metallized markings.

Figure 3 - 365 Ball BGA

Pin Description

Signal Name	Signal Type	BGA Ball #	Signal Description
V_{DD1} = 3.3V	Power	R6, R8, R13, R15, N15,H15, F15,F13,F8,F6,H6,N6, P6,	Positive Power Supply. Nominally 3.3 volt. V_{DD1} = I/O Voltage
V_{DD2} = 1.8V	Power	R9,R10,R11,R12,M15, L15,K15,J15,F12,F11, F10,F9,J6, K6, L6,M6,	Positive Power Supply. Nominally 1.8 volt. V_{DD2} = Core Voltage
VSS	Power	H8,H9,H10,H11,H12, H13, J8, J9,J10,J11, J12,J13,K8,K9,K10,K11,K12,K13 L8,L9,L10, L11,L12,L13,M8,M9,M10,M11,M12, M13, N8, N9,N10,N11,N12,N13	Ground
DEVICE 1			
TMS_d1	User Signal	J4	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI_d1	User Signal	J3	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d1	User Signal	J2	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d1	User Signal	J1	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d1	User Signal	K1	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
Test_En_d1	ICO	H1	**Internal Connection.** Connected to VSS for normal operation
RESETB_d1	User Signal	K2	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
IRQB_d1	User Signal	J5	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d1	User Signal	H2	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.
CSB_d1	User Signal	K3	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d1	User Signal	H3	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTAB_d1	User Signal	K4	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D(0)_d1	User Signal	H4	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1)_d1	User Signal	K5	
D(2)_d1	User Signal	H5	
D(3)_d1	User Signal	G4	
D(4)_d1	User Signal	G5	
D(5)_d1	User Signal	F4	
D(6)_d1	User Signal	F5	
D(7)_d1	User Signal	E5	
A(0)_d1	User Signal	D4	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d1	User Signal	E6	
A(2)_d1	User Signal	D5	
A(3)_d1	User Signal	E7	
A(4)_d1	User Signal	D7	
A(5)_d1	User Signal	E8	
A(6)_d1	User Signal	E10	
A(7)_d1	User Signal	D8	
A(8)_d1	User Signal	D10	
A(9)_d1	User Signal	C10	
A(10)_d1	User Signal	B10	

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
A_IC1_d1	ICO	E9	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d1	ICO	A8	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d1	NC	A10	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d1	NC	A9	**No connection.** The pin must be left open for normal operation.
Tsig(2)_d1	NC	B9	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d1	NC	C9	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d1	NC	D9	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d1	NC	C8	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d1	NC	B8	**No connection.** The pin must be left open for normal operation.
Tsig(7)_d1	NC	A7	**No connection.** The pin must be left open for normal operation.
ODE_d1	User Signal	B7	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout_d1	User Signal	C7	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d1	User Signal	A6	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d1	User Signal	B6	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d1	User Signal	D6	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
FOIb_d1	User Signal	A5	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d1	User Signal	C6	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d1	ICO	B5	**Internal Connection.** Connected to VSS for normal operation
SM_mclk_d1	ICO	A4	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d1	ICO	B4	**Internal Connection.** Connected to VSS for normal operation
SC_en_d1	ICO	C5	**Internal Connection.** Connected to VSS for normal operation
SC_In_d1	ICO	A3	**Internal Connection.** Connected to VSS for normal operation
SC_Reset:_d1	ICO	B3	**Internal Connection.** Connected to VSS for normal operation
SC_Fclk_d1	ICO	A2	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d1	NC	C4	**Internal Connection.** The pin must be left open for normal operation.
Tsig(9)_d1	NC	C3	**Internal Connection.** The pin must be left open for normal operation.
Tsig(10)_d1	NC	D3	**Internal Connection.** The pin must be left open for normal operation.
Tsig(11)_d1	NC	B2	**Internal Connection.** The pin must be left open for normal operation.
Tsig(12)_d1	NC	A1	**Internal Connection.** The pin must be left open for normal operation.
Tsig(13)_d1	NC	C2	**Internal Connection.** The pin must be left open for normal operation.
Tsig(14)_d1	NC	E3	**Internal Connection.** The pin must be left open for normal operation.
Tsig(15)_d1	NC	B1	**Internal Connection.** The pin must be left open for normal operation.
Tm1_d1	ICO	D2	**Internal Connection.** Connected to VSS for normal operation
Tm2_d1	ICO	C1	**Internal Connection.** Connected to VSS for normal operation

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Sg1_d1	ICO	E4	**Internal Connection.** Connected to VSS for normal operation
DT1_d1	NC	F3	**No connection.** The pin must be left open for normal operation.
MCLK_d1	User Signal	E2	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel_d1	User Signal	D1	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d1	ICO	E1	**Internal Connection.** Connected to VSS for normal operation
Step_d1	ICO	F2	**Internal Connection.** Connected to VSS for normal operation
PLLVSS1_d1	Power	G3	**PLL Ground.** Must be connected to VSS
PLLVDD_d1	Power	F1	**PLL Power Supply.** Must be connected to VDD2
PLLVSS2_d1	Power	G2	**PLL Ground.** Must be connected to VSS
AT1_d1	NC	G1	**No connection.** The pin must be left open for normal operation.
DEVICE 2			
TMS_d2	Signal	V4	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI_d2	Signal	Y2	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d2	Signal	W3	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d2	Signal	Y3	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d2	Signal	W4	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Test_En_d2	ICO	V5	**Internal Connection.** Connected to VSS for normal operation
RESETB_d2	Signal	Y4	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.
IRQB_d2	Signal	U5	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d2	Signal	W5	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.
CSB_d2	Signal	Y5	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d2	Signal	V6	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTAB_d2	Signal	U6	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D(0)_d2	Signal	W6	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1)_d2	Signal	Y6	
D(2)_d2	Signal	V7	
D(3)_d2	Signal	W7	
D(4)_d2	Signal	Y7	
D(5)_d2	Signal	Y8	
D(6)_d2	Signal	W8	
D(7)_d2	Signal	V8	

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
A(0)_d2	Signal	U9	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d2	Signal	V9	
A(2)_d2	Signal	W9	
A(3)_d2	Signal	Y9	
A(4)_d2	Signal	U10	
A(5)_d2	Signal	T10	
A(6)_d2	Signal	T9	
A(7)_d2	Signal	V10	
A(8)_d2	Signal	W10	
A(9)_d2	Signal	U8	
A(10)_d2	Signal	Y10	
A_IC1_d2	ICO	T8	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d2	ICO	T7	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d2	NC	U7	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d2	NC	T6	**No connection.** The pin must be left open for normal operation.
Tsig(2)_d2	NC	U4	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d2	NC	T5	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d2	NC	R5	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d2	NC	T4	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d2	NC	P5	**No connection.** The pin must be left open for normal operation.
Tsig(7)_d2	NC	P4	**No connection.** The pin must be left open for normal operation.
ODE_d2	Signal	N5	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Sout_d2	Signal	L1	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d2	Signal	N4	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d2	Signal	L2	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d2	Signal	N3	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
FOIb_d2	Signal	N2	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d2	Signal	L3	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d2	ICO	N1	**Internal Connection.** Connected to VSS for normal operation
SM_mclk_d2	ICO	L4	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d2	ICO	M5	**Internal Connection.** Connected to VSS for normal operation
SC_en_d2	ICO	L5	**Internal Connection.** Connected to VSS for normal operation
SC_In_d2	ICO	M1	**Internal Connection.** Connected to VSS for normal operation
SC_Reset:_d2	ICO	M2	**Internal Connection.** Connected to VSS for normal operation
SC_Fclk_d2	ICO	M3	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d2	NC	M4	**No connection.** The pin must be left open for normal operation.
Tsig(9)_d2	NC	P1	**No connection.** The pin must be left open for normal operation.
Tsig(10)_d2	NC	P2	**No connection.** The pin must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Tsig(11)_d2	NC	R1	**No connection.** The pin must be left open for normal operation.
Tsig(12)_d2	NC	R2	**No connection.** The pin must be left open for normal operation.
Tsig(13)_d2	NC	P3	**No connection.** The pin must be left open for normal operation.
Tsig(14)_d2	NC	T1	**No connection.** The pin must be left open for normal operation.
Tsig(15)_d2	NC	U1	**No connection.** The pin must be left open for normal operation.
Tm1_d2	ICO	T2	**Internal Connection.** Connected to VSS for normal operation
Tm2_d2	ICO	R3	**Internal Connection.** Connected to VSS for normal operation
Sg1_d2	ICO	R4	**Internal Connection.** Connected to VSS for normal operation
DT1_d2	NC	V1	**No connection.** The pin must be left open for normal operation.
MCLK_d2	Signal	U2	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel_d2	Signal	W1	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d2	ICO	T3	**Internal Connection.** Connected to VSS for normal operation
Step_d2	ICO	V2	I**nternal Connection.** Connected to VSS for normal operation
PLLVSS1_d2	Power	Y1	**PLL Ground.** Must be connected to VSS
PLLVDD_d2	Power	W2	**PLL Power Supply**. Must be connected to VDD2
PLLVSS2_d2	Power	U3	**PLL Ground.** Must be connected to VSS
AT1_d2	NC	V3	**No connection.** The pin must be left open for normal operation.
DEVICE 3			
TMS_d3	Signal	W13	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
TDI_d3	Signal	V13	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d3	Signal	Y14	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d3	Signal	W14	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d3	Signal	Y15	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
Test_En_d3	ICO	V14	**Internal Connection.** Connected to VSS for normal operation
RESETB_d3	Signal	W15	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.
IRQB_d3	Signal	Y16	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d3	Signal	Y17	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.
CSB_d3	Signal	W16	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d3	Signal	V15	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
B_d3	Signal	Y18	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
D(0)_d3	Signal	W17	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1) _d3	Signal	Y19	
D(2)_d3	Signal	V16	
D(3)_d3	Signal	W18	
D(4)_d3	Signal	Y20	
D(5)_d3	Signal	W19	
D(6)_d3	Signal	V17	
D(7)_d3	Signal	V18	
A(0)_d3	Signal	U18	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d3	Signal	V19	
A(2)_d3	Signal	W20	
A(3)_d3	Signal	V20	
A(4)_d3	Signal	T18	
A(5)_d3	Signal	U19	
A(6)_d3	Signal	U20	
A(7)_d3	Signal	T19	
A(8)_d3	Signal	R18	
A(9)_d3	Signal	T20	
A(10)_d3	Signal	R17	
A_IC1_d3	ICO	R19	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d3	ICO	P18	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d3	NC	R20	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d3	NC	P19	**No connection.** The pin must be left open for normal operation.
Tsig(2)_d3	NC	P20	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d3	NC	N19	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d3	NC	N18	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d3	NC	M17	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d3	NC	M18	**No connection.** The pin must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Tsig(7)_d3	NC	M19	**No connection.** The pin must be left open for normal operation.
ODE_d3	Signal	M20	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout_d3	Signal	L20	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d3	Signal	N20	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d3	Signal	M16	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d3	Signal	L19	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
FOIb_d3	Signal	L18	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d3	Signal	L17	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d3	ICO	N17	**Internal Connection.** Connected to VSS for normal operation
SM_mclk_d3	ICO	L16	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d3	ICO	N16	**Internal Connection.** Connected to VSS for normal operation
SC_en_d3	ICO	P17	**Internal Connection.** Connected to VSS for normal operation
SC_In_d3	ICO	P16	**Internal Connection**. Connected to VSS for normal operation
SC_Reset:_d3	ICO	R16	**Internal Connection.** Connected to VSS for normal operation

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
SC_Fclk_d3	ICO	T17	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d3	NC	U17	**No connection.** The pin must be left open for normal operation.
Tsig(9)_d3	NC	U16	**No connection.** The pin must be left open for normal operation.
Tsig(10)_d3	NC	T16	**No connection.** The pin must be left open for normal operation.
Tsig(11)_d3	NC	T15	**No connection.** The pin must be left open for normal operation.
Tsig(12)_d3	NC	U15	**No connection.** The pin must be left open for normal operation.
Tsig(13)_d3	NC	T14	**No connection.** The pin must be left open for normal operation.
Tsig(14)_d3	NC	U14	**No connection.** The pin must be left open for normal operation.
Tsig(15)_d3	NC	T13	**No connection.** The pin must be left open for normal operation.
Tm1_d3	ICO	Y11	**Internal Connection.** Connected to VSS for normal operation
Tm2_d3	ICO	U13	**Internal Connection.** Connected to VSS for normal operation
Sg1_d3	ICO	W11	**Internal Connection.** Connected to VSS for normal operation
DT1_d3	NC	V11	**No connection.** The pin must be left open for normal operation.
MCLK_d3	Signal	U11	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel_d3	Signal	T12	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d3	ICO	Y13	**Internal Connection.** Connected to VSS for normal operation
Step_d3	ICO	T11	**Internal Connection.** Connected to VSS for normal operation
PLLVSS1_d3	Power	Y12	**PLL Ground.** Must be connected to VSS
PLLVDD_d3	Power	W12	**PLL Power Supply.** Must be connected to VDD2

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
PLLVSS2_d3	Power	V12	**PLL Ground.** Must be connected to VSS
AT1_d3	NC	U12	**No connection.** The pin must be left open for normal operation.
DEVICE 4			
TMS_d4	Signal	E16	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI_d4	Signal	D17	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d4	Signal	C18	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d4	Signal	F16	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d4	Signal	E17	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
Test_En_d4	ICO	G16	**Internal Connection.** Connected to VSS for normal operation
RESETB_d4	Signal	F17	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.
IRQB_d4	Signal	G17	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d4	Signal	H16	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
CSB_d4	Signal	K16	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d4	Signal	H17	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTAB_d4	Signal	K17	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D(0)_d4	Signal	K18	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1)_d4	Signal	J16	
D(2)_d4	Signal	K19	
D(3)_d4	Signal	K20	
D(4)_d4	Signal	J20	
D(5)_d4	Signal	J19	
D(6)_d4	Signal	J18	
D(7)_d4	Signal	J17	
A(0)_d4	Signal	H18	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d4	Signal	H19	
A(2)_d4	Signal	H20	
A(3)_d4	Signal	G20	
A(4)_d4	Signal	G19	
A(5)_d4	Signal	G18	
A(6)_d4	Signal	F20	
A(7)_d4	Signal	F19	
A(8)_d4	Signal	F18	
A(9)_d4	Signal	E20	
A(10)_d4	Signal	E19	
A_IC1_d4	ICO	D20	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d4	ICO	E18	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d4	NC	D19	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d4	NC	C20	**No connection.** The pin must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Tsig(2)_d4	NC	B20	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d4	NC	C19	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d4	NC	D18	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d4	NC	C17	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d4	NC	B19	**No connection.** The pin must be left open for normal operation.
Tsig(7)_d4	NC	A20	**No connection.** The pin must be left open for normal operation.
ODE_d4	Signal	B18	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout_d4	Signal	A19	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d4	Signal	C16	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d4	Signal	B17	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d4	Signal	A18	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
FOIb_d4	Signal	B16	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d4	Signal	C15	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d4	ICO	A17	**Internal Connection.** Connected to VSS for normal operation

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
SM_mclk_d4	ICO	A16	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d4	ICO	B15	**Internal Connection.** Connected to VSS for normal operation
SC_en_d4	ICO	C14	**Internal Connection.** Connected to VSS for normal operation
SC_In_d4	ICO	A15	**Internal Connection.** Connected to VSS for normal operation
SC_Reset:_d4	ICO	B14	**Internal Connection.** Connected to VSS for normal operation
SC_Fclk_d4	ICO	A14	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d4	NC	C13	**No connection.** The pin must be left open for normal operation.
Tsig(9)_d4	NC	D12	**No connection.** The pin must be left open for normal operation.
Tsig(10)_d4	NC	A12	**No connection.** The pin must be left open for normal operation.
Tsig(11)_d4	NC	B12	**No connection. T**he pin must be left open for normal operation.
Tsig(12)_d4	NC	C12	**No connection.** The pin must be left open for normal operation.
Tsig(13)_d4	NC	E11	**No connection.** The pin must be left open for normal operation.
Tsig(14)_d4	NC	A13	No connection. The pin must be left open for normal operation.
Tsig(15)_d4	NC	E12	**No connection.** The pin must be left open for normal operation.
Tm1_d4	ICO	D11	**Internal Connection.** Connected to VSS for normal operation
Tm2_d4	ICO	B13	**Internal Connection.** Connected to VSS for normal operation
Sg1_d4	ICO	C11	**Internal Connection.** Connected to VSS for normal operation
DT1_d4	NC	B11	**No connection.** The pin must be left open for normal operation.
MCLK_d4	Signal	D13	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Fsel_d4	Signal	A11	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d4	ICO	E13	**Internal Connection.** Connected to VSS for normal operation
Step_d4	ICO	D14	**Internal Connection.** Connected to VSS for normal operation
PLLVSS1_d4	Power	E14	**PLL Ground.** Must be connected to VSS
PLLVDD_d4	Power	D15	**PLL Power Supply.** Must be connected to VDD2
PLLVSS2_d4	Power	D16	**PLL Ground.** Must be connected to VSS
AT1_d4	NC	E15	**No connection.** The pin must be left open for normal operation.

Description of the Single MT93L00

Device Overview

The MT93L00 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers, Echo Canceller A and Echo Canceller B. Each group can be configured in Normal, Extended Delay or Back-to-Back configurations. In Normal configuration, a group of echo cancellers provides two channels of 64 ms echo cancellation, which run independently on different channels. In Extended Delay configuration, a group of echo cancellers achieves 128 ms of echo cancellation by cascading the two echo cancellers (A & B). In Back-to-Back configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel, providing full-duplex 64 ms echo cancellation.

Each echo canceller contains the following main elements (see Figure 4).

- Adaptive Filter for estimating the echo channel
- Subtractor for cancelling the echo
- Double-Talk detector for disabling the filter adaptation during periods of double-talk
- Path Change detector for fast reconvergence on major echo path changes
- Instability Detector to combat oscillation in very low ERL environments
- Non-Linear Processor for suppression of residual echo
- Disable Tone Detectors for detecting valid disable tones at send and receive path inputs
- Narrow-Band Detector for preventing Adaptive Filter divergence from narrow-band signals
- Offset Null filters for removing the DC component in PCM channels
- 12 dB attenuator for signal attenuation
- Parallel controller interface compatible with Motorola microcontrollers
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711 or Sign-Magnitude coding

Each echo canceller in the MT93L00 has four functional states: Mute, Bypass, Disable Adaptation and Enable Adaptation. These are explained in the section entitled Echo Canceller Functional States.

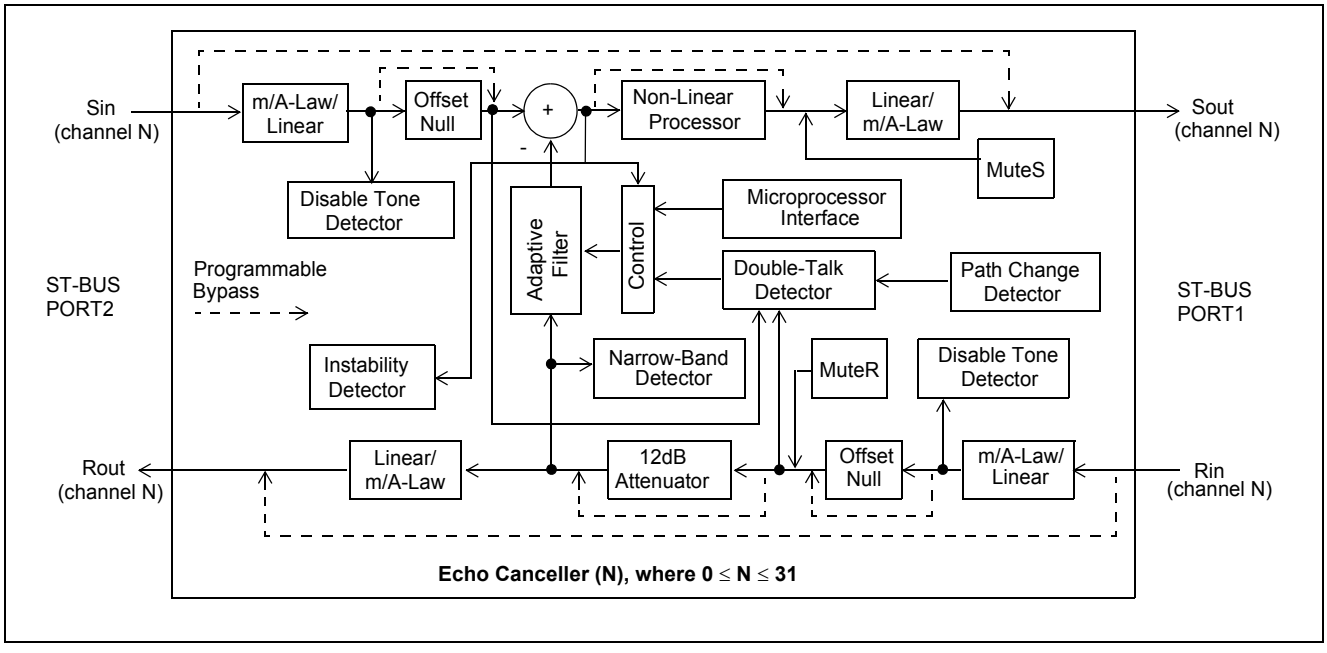


Figure 4 - Echo Canceller Functional Block Diagram

Adaptive Filter

The adaptive filter adapts to the echo path and generates an estimate of the echo signal. This echo estimate is then subtracted from Sin. For each group of echo cancellers, the adaptive filter is a 1024 tap FIR adaptive filter which is divided into two sections. Each section contains 512 taps providing 64 ms of echo estimation. In Normal configuration, the first section is dedicated to channel A and the second section to channel B. In Extended Delay configuration, both sections are cascaded to provide 128ms of echo estimation in channel A. In Back-to Back configuration, the first section is used in the receive direction and the second section is used in the transmit direction for the same channel.

Double-Talk Detector

Double-Talk is defined as those periods of time when signal energy is present in both directions simultaneously. When this happens, it is necessary to disable the filter adaptation to prevent divergence of the Adaptive Filter coefficients. Note that when double-talk is detected, the adaptation process is halted but the echo canceller continues to cancel echo using the previous converged echo profile.

A double-talk condition exists whenever the relative signal levels of Rin (Lrin) and Sin (Lsin) meet the following condition:

$$Lsin > Lrin + 20log10(DTDT)$$

where DTDT is the Double-Talk Detection Threshold.
Lsin and Lrin are signal levels expressed in dBm0.

A different method is used when it is uncertain whether Sin consists of a low level double-talk signal or an echo return. During these periods, the adaptation process is slowed down but it is not halted.

In G.168 standard, the echo return loss is expected to be at least 6 dB. This implies that the Double-Talk Detector Threshold (DTDT) should be set to 0.5 (-6 dB). However, in order to get additional guardband, the DTDT is set internally to 0.5625 (-5 dB).

In some applications the return loss can be higher or lower than 6 dB. The MT93L00 allows the user to change the detection threshold to suit each application's need. This threshold can be set by writing the desired threshold value into the DTDT register.

The DTDT register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$DTDT(hex) = hex(DTDT(dec) * 32768)$$

$$where\ 0 < DTDT(dec) < 1$$

Example: For DTDT = 0.5625 (-5dB), the hexadecimal value becomes hex(0.5625 * 32768) = 4800h

Path Change Detector

Integrated into the MT93L00A is a Path Change Detector. This permits fast reconvergence when a major change occurs in the echo channel. Subtle changes in the echo channel are also tracked automatically once convergence is achieved, but at a much slower speed.

The Path Change Detector is activated by setting the PathDet bit in Control Register A3/B3 to "1". An optional path clearing feature can be enabled by setting the PathClr bit in Control Register A3/B3 to "1". With path clearing turned on, the existing echo channel estimate will also be cleared (i.e. the adaptive filter will be filled with zeroes) upon detection of a major path change.

Non-Linear Processor (NLP)

After echo cancellation, there is always a small amount of residual echo which may still be audible. The MT93L00 uses an NLP to remove residual echo signals which have a level lower than the Adaptive Suppression Threshold (TSUP in G.168). This threshold depends upon the level of the Rin (Lrin) reference signal as well as the programmed value of the Non-Linear Processor Threshold register (NLPTHR). TSUP can be calculated by the following equation:

$$TSUP = Lrin + 20\log10(NLPTHR)$$

where NLPTHR is the Non-Linear Processor Threshold register value
and Lrin is the relative power level expressed in dBm0.

When the level of residual error signal falls below TSUP, the NLP is activated further attenuating the residual signal by an additional 36 dB. To prevent a perceived decrease in background noise due to the activation of the NLP, a spectrally-shaped comfort noise, equivalent in power level to the background noise, is injected. This keeps the perceived noise level constant. Consequently, the user does not hear the activation and de-activation of the NLP.

The NLP processor can be disabled by setting the NLPDis bit to “1” in Control Register 2.

The NLPTHR register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$NLPTHR(hex) = hex(NLPTHR(dec) * 32768)$$

$$where\ 0 < NLPTHR(dec) < 1$$

The comfort noise injector can be disabled by setting the INJDis bit to “1” in Control Register A1/B1. It should be noted that the NLPTHR is valid and the comfort noise injection is active only when the NLP is enabled.

If the comfort noise injector is unable to correctly match the level of the background noise (because of peculiar spectral characteristics, for example), the injected level can be fine-tuned using the Noise Scaling register. A neutral value of 80(hex) will prevent any scaling. Values less than 80(hex) will reduce the noise level, values greater than 80(hex) will increase the noise level. The scaling is done linearly.

Example: To decrease the comfort noise level by 3 dB, the register value would be 10 ^ (-3 / 20) • 128 = 0.71 • 128 = 91(dec) = 5B(hex)

The default factory setting for the Noise Scaling register should be adequate for most operating environments. It is unlikely that it will need to be changed. It has also been set to a value which will ensure G.168 compliance.

Disable Tone Detector

G.165 recommendation defines the disable tone as having the following characteristics: 2100 Hz (±21 Hz) sine wave, a power level between -6 to -31 dBm0, and a phase reversal of 180 degrees (± 25 degrees) every 450 ms (± 25 ms). If the disable tone is present for a minimum of one second with at least one phase reversal, the Tone Detector will trigger.

G.164 recommendation defines the disable tone as a 2100 Hz (±21 Hz) sine wave with a power level between 0 to -31 dBm0. If the disable tone is present for a minimum of 400 milliseconds, with or without phase reversal, the Tone Detector will trigger.

The MT93L00 has two Tone Detectors per channels (for a total of 64) in order to monitor the occurrence of a valid disable tone on both Rin and Sin. Upon detection of a disable tone, TD bit of the Status Register will indicate logic high and an interrupt is generated (i.e., IRQ pin low). Refer to Figure 5 and to the Interrupts section.

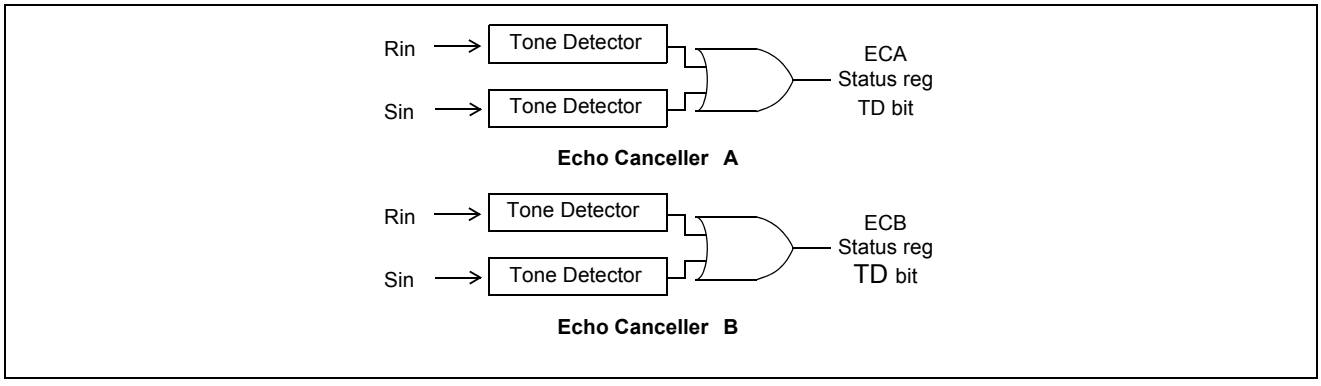


Figure 5 - Disable Tone Detection

Once a Tone Detector has been triggered, there is no longer a need for a valid disable tone (G.164 or G.165) to maintain Tone Detector status (i.e., TD bit high). The Tone Detector status will only release (i.e., TD bit low) if the signals Rin and Sin fall below -30 dBm0, in the frequency range of 390 Hz to 700 Hz, and below -34 dBm0, in the