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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DDR2 SDRAM Unbuffered DIMM

## MT9HTF3272A – 256MB
MT9HTF6472A – 512MB
MT9HTF12872A – 1GB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/products/modules

Features

- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- 256MB (32 Meg x 72), 512MB (64 Meg x 72) 1GB (128 Meg x 72)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 1: 240-Pin DIMM (MO-237 R/C "A")

Height 1.18in. (29.97mm)
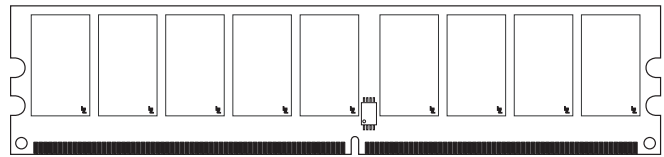
Options	Marking
- Package	
240-pin DIMM (lead-free)	Y
- Frequency/CAS Latency[1]	
3ns @ CL = 5 (DDR2-667)[2]	-667
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)	-40E
- PCB Height	
1.18in. (29.97mm)	

Notes: 1. CL = CAS (READ) Latency.
2. Not available in 1GB density.

Products and specifications discussed herein are subject to change by Micron without notice.

Table 1: Address Table

	256MB	512MB	1GB
Refresh Count	8K	8K	8K
Row Addressing	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device Page Size per Bank	1KB	1KB	1KB
Device Configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column Addressing	1K (A0–A9)	1K (A0-A9)	1K (A0-A9)
Module Rank Addressing	1 (S0#)	1 (S0#)	1 (S0#)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MT/s)			^tRCD (ns)	^tRP (ns)	^tRC (ns)
	CL = 3	CL = 4	CL = 5			
-667	—	533	667	15	15	55
-53E	400	533	—	15	15	55
-40E	400	400	—	15	15	55

Table 3: Part Numbers and Timing Parameters

Part Number[1]	Module Densit	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^tRCD - ^tRP)
MT9HTF3272AY-667__	256MB	32 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF3272AY-53E__	256MB	32 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF3272AY-40E__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9HTF6472AY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472AY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF6472AY-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9HTF12872AY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872AY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF12872AY-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF6472AY-40EC2.

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Pin Assignments and Descriptions

Table 4:   Pin Assignment

	240-Pin DIMM Front							240-Pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	Vss	121	Vss	151	Vss	181	VDDQ	211	DM5
2	Vss	32	Vss	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	Vss
4	DQ1	34	DQ25	64	VDD	94	Vss	124	Vss	154	Vss	184	VDD	214	DQ46
5	Vss	35	Vss	65	Vss	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	Vss	96	DQ43	126	NC	156	NC	186	CK0#	216	Vss
7	DQS0	37	DQS3	67	VDD	97	Vss	127	Vss	157	Vss	187	VDD	217	DQ52
8	Vss	38	Vss	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	Vss
10	DQ3	40	DQ27	70	A10/AP	100	Vss	130	Vss	160	Vss	190	BA1	220	RFU
11	Vss	41	Vss	71	BA0	101	SA2	131	DQ12	161	CB4	191	VDDQ	221	RFU
12	DQ8	42	CB0	72	VDDQ	102	NC	132	DQ13	162	CB5	192	RAS#	222	Vss
13	DQ9	43	CB1	73	WE#	103	Vss	133	Vss	163	Vss	193	S0#	223	DM6
14	Vss	44	Vss	74	CAS#	104	DQS6#	134	DM1	164	DM8	194	VDDQ	224	NC
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6	135	NC	165	NC	195	ODT0	225	Vss
16	DQS1	46	DQS8	76	NC	106	Vss	136	Vss	166	Vss	196	NC/A13	226	DQ54
17	Vss	47	Vss	77	NC	107	DQ50	137	RFU	167	CB6	197	VDD	227	DQ55
18	NC	48	CB2	78	VDDQ	108	DQ51	138	RFU	168	CB7	198	Vss	228	Vss
19	NC	49	CB3	79	Vss	109	Vss	139	Vss	169	Vss	199	DQ36	229	DQ60
20	Vss	50	Vss	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	NC	201	Vss	231	Vss
22	DQ11	52	CKE0	82	Vss	112	Vss	142	Vss	172	VDD	202	DM4	232	DM7
23	Vss	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC	233	NC
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	NC	204	Vss	234	Vss
25	DQ17	55	NC	85	Vss	115	Vss	145	Vss	175	VDDQ	205	DQ38	235	DQ62
26	Vss	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	Vss	237	Vss
28	DQS2	58	A7	88	Vss	118	Vss	148	Vss	178	VDD	208	DQ44	238	VDDSPD
29	Vss	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	Vss	240	SA1

Note: Pin 196 is NC for 256MB, or A13 for 512MB and 1GB; pin 54 is NC for 256MB and 512MB, or BA2 for 1GB.

Figure 2:   Pin Locations

Front View

Back View

No Components This Side of Module

PIN 1   PIN 64   PIN 65   PIN 120   PIN 240   PIN 185   PIN 184   PIN 121

▌ Indicates a VDD or VDDQ pin   ▌ Indicates a Vss pin

Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
195	ODT0	Input	On-Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, CB, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
137, 138, 185, 186, 220, 221	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
52	CKE0	Input	Clock Enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained to this input.
193	S0#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
73, 74, 192	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
54 (1GB), 71, 190	BA0, BA1, BA2 (1GB)	Input	Bank Address Inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
57, 58, 60, 61, 63, 70, 176, 177, 179, 180, 182, 183, 188, 196 (1GB)	A0–A12 (256MB) A0–A13 (512MB, 1GB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
125, 134, 146, 155, 164, 202, 211, 223, 232	DM0–DM8	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.

Table 5:   Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
3, 4, 9, 10, 12, 13, 21, 22, 24, 25, 30, 31, 33, 34, 39, 40, 80, 81, 86, 87, 89, 90, 95, 96, 98, 99, 107, 108, 110, 111, 116, 117, 122, 123, 128, 129, 131, 132, 140, 141, 143, 144, 149, 150, 152, 153, 158, 159, 199, 200, 205, 206, 208, 209, 214, 215, 217, 218, 226, 227, 229, 230, 235, 236	DQ0–DQ63	I/O	Data Input/Output: Bidirectional data bus.
6, 7, 15, 16, 27, 28, 36, 37, 45, 46, 83, 84, 92, 93, 104, 105, 113, 114	DQS0–DQS8, DQS0#–DQS8#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
42, 43, 48, 49, 161, 162, 167, 168	CB0–CB7	I/O	Check Bits.
120	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
101, 239, 240	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
119	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197,	V$_{DD}$	Supply	Power Supply: +1.8V ±0.1V.
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194,	V$_{DDQ}$	Supply	DQ Power Supply: +1.8V ±0.1V.
1	V$_{REF}$	Supply	SSTL_18 reference voltage.
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97,100, 103, 106, 109,112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V$_{SS}$	Supply	Ground.
238	V$_{DDSPD}$	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
18, 19, 42, 43, 48, 49, 54 (256MB, 512MB), 55, 68, 76, 77, 102, 126, 135, 147, 156, 161, 162, 165, 167, 168, 171, 196 (256MB), 173, 174, 203, 212, 224, 233	NC	—	No Connect: These pins should be left unconnected.

Functional Block Diagram

Unless otherwise noted, resistor values are 22Ω Micron module part numbers are explained in the Module Part Numbering Guide a *www.micron.com/support/numbering.html*. Modules use the following DDR2 SDRAM devices: MT47H32M8BP (256MB); MT47H64M8BT (512MB); and MT47H128M8BT (1GB).

Figure 3:   Functional Block Diagram
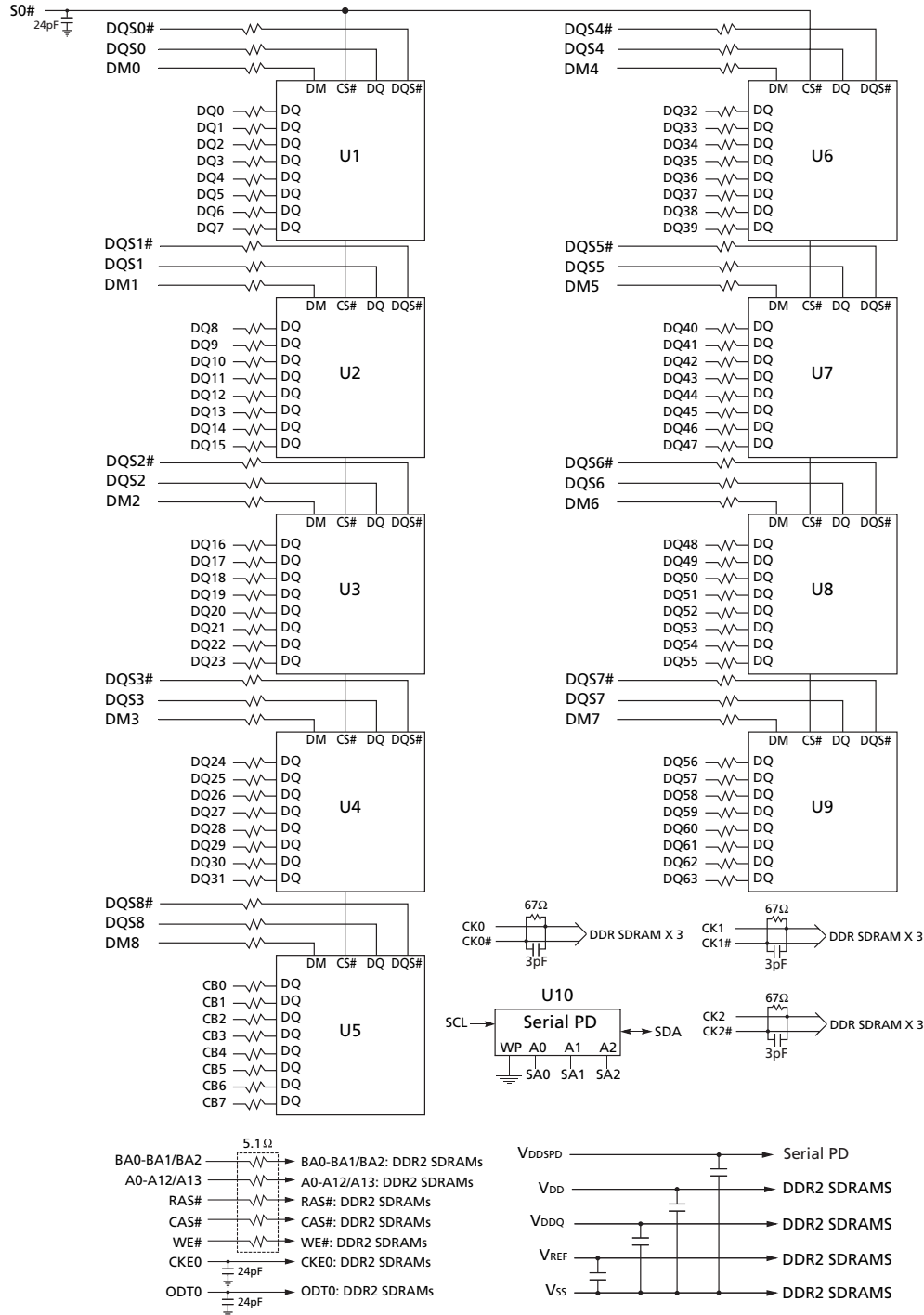
General Description

The MT9HTF3272A, MT9HTF6472A, and MT9HTF12872A DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x64 configuration. DDR2 SDRAM modules use internally configured quad-bank (256MB, 512MB) or eight-bank (1GB) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR2 SDRAM modules are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting column location for the burst access.

DDR2 SDRAM modules provide for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM devices support interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR2 SDRAM devices allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^{2}C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

The following sequence is required for power-up and initialization and is shown in Figure 4, DDR2 Power-Up and Initialization, on page 12.

1. Apply power; if CKE is maintained below 20 percent of V_{DDQ}, outputs remain disabled. To guarantee R_{TT} (ODT Resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT pin (all other inputs may be undefined). The time from when V_{DD} first starts to power-up to the completion of V_{DDQ} must be equal to or less than 20ms. At least one of the following two sets of conditions (A or B) must be met:

   A. CONDITION SET A
      - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V MAX
      - V_{REF} tracks $V_{DDQ}/2$
   B. CONDITION SET B
      - Apply V_{DD} before or at the same time as V_{DDL}.
      - Apply V_{DDL} before or at the same time as V_{DDQ}
      - Apply V_{DDQ} before or at the same time as V_{TT} and V_{REF}

3. The voltage difference between any V_{DD} supply can not exceed 0.3V. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH

4. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.

5. Issue a LOAD MODE command to the EMR(2) register. (To issue an EMR(2) command, provide LOW to BA0 and BA2, provide HIGH to BA1.)

6. Issue a LOAD MODE command to the EMR(3) register. (To issue an EMR(3) command, provide HIGH to BA0 and BA1, provide LOW to BA2.)

7. Issue a LOAD MODE command to the EMR register to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1, BA2, and A0, provide HIGH to BA0. Bits E7, E8, and E9 must all be set to 0.

8. Issue a LOAD MODE command for DLL Reset. 200 cycles of clock input is required to lock the DLL. (To issue a DLL Reset, provide HIGH to A8 and provide LOW to BA2, BA1 and BA0.) CKE must be HIGH the entire time.

9. Issue PRECHARGE ALL command.

10. Issue two or more REFRESH commands.

11. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).

12. Issue a LOAD MODE command to the EMR to enable OCD default by setting Bits E7, E8, and E9 to 1 and set all other desired parameters.

13. Issue a LOAD MODE command to the EMR to enable OCD exit by setting Bits E7, E8, and E9 to 0 and set all other desired parameters.

The DDR2 SDRAM device is now intialized and ready for normal operation 200 clocks after DLL Reset in step 8.

Figure 4:   DDR2 Power-Up and Initialization
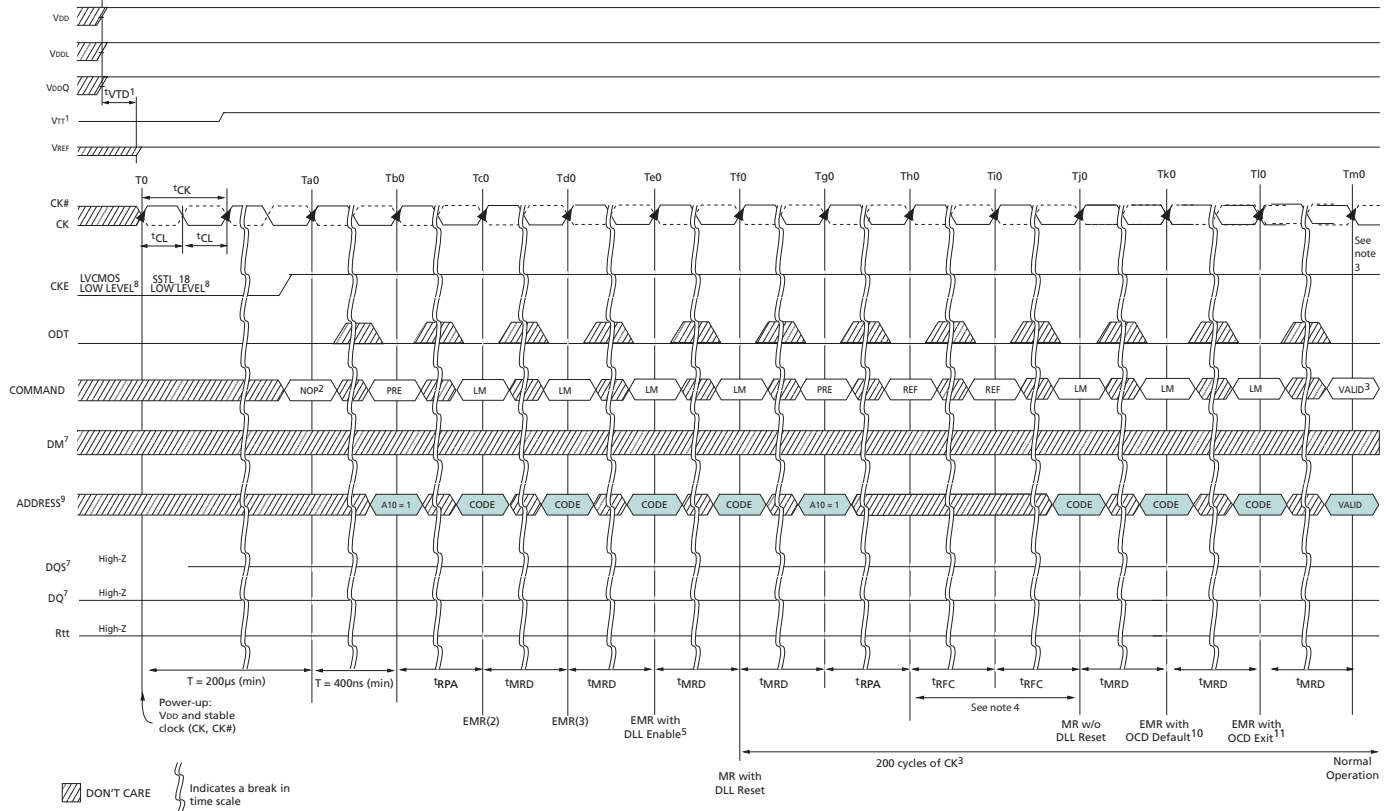
Notes: 1. V_{TT} is not applied directly to the device; however, ^{t}VTD should be greater than or equal to zero to avoid device latch-up.

The time from when V_{DD} first starts to power-up to the completion of V_{DDQ} must be equal to or less than 20ms. One of the following two conditions (a or b) MUST be met:

- A.   V_{DD}, V_{DDL}, and V_{DDQ} are driven from a single power converter output.
      V_{TT} may be 0.95V maximum during power up.
      V_{REF} tracks V_{DDQ}/2.
- B.   Apply V_{DD} before or at the same time as V_{DDL}.
      Apply V_{DDL} before or at the same time as V_{DDQ}.

2. Apply V_{DDQ} before or at the same time as V_{TT} and V_{REF}. The voltage difference between any V_{DD} supply can not exceed 0.3V.

3. Either a NOP or DESELECT command may be applied.

4. 200 cycles of clock (CK, CK#) are required before a READ command can be issued. CKE must be HIGH the entire time.

5. Two or more REFRESH commands are required.

6. Bits E7, E8, and E9 must all be set to 0 with all other operating parameters of EMRS set as required.

7. PRE = PRECHARGE command, LM = LOAD MODE command, REF = REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.

8. DM represents all DM. DQS represents all DQS, DQS#, RDQS,and RDQS# (RDQS/RDQS# only functional on RDIMMs using x8 components). DQ represents all DQ.

9. CKE pin uses LVCMOS input levels prior to state T0. After state T0, CKE pin uses SSTL_18 input levels.

10. A10 should be HIGH at states Tb0 and Tg0 to ensure a PRECHARGE (all banks) command is issued.

11. Bits E7, E8, and E9 must be set to 1 to set OCD default.

12. Bits E7, E8, and E9 must be set to 0 to set OCD exit and all other operating parameters of EMRS set as required.

Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM device. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL reset, write recovery, and power-down mode as shown in Figure 5, Mode Register (MR) Definition. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the LOAD MODE command is issued.

The mode register is programmed via the LM command (bits BA0–BA1/BA2 all = 0) and other bits (M0–M13 or M0–M14) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LOAD MODE command can only be issued (or reissued) when all banks are in the precharged state. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M2 as shown in Figure 5, Mode Register (MR) Definition. Read and write accesses to the DDR2 SDRAM device are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3 as shown in Figure 5, Mode Register (MR) Definition. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address as shown in Table 6, Burst Definition, on page 15. DDR2 SDRAM devices support 4-bit burst and 8-bit burst modes only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

Figure 5:   Mode Register (MR) Definition

256MB Address Bus

1GB Address Bus

M7	Mode
0	Normal
1	Test

M12	PD mode
0	Fast Exit (Normal)
1	Slow Exit (Low Power)

M8	DLL Reset
0	No
1	Yes

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M11	M10	M9	WRITE RECOVERY
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

Table 6:   Burst Definition

Burst Length	Starting Column Address (A2, A1, A0)	Order of Accesses Within a Burst	
		Burst Type = Sequential	Burst Type = Interleaved
4	0 0 0	0,1,2,3	0,1,2,3
	0 0 1	1,2,3,0	1,0,3,2
	0 1 0	2,3,0,1	2,3,0,1
	0 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE command with bit M7 set to zero, and all other bits set to the desired values as shown in Figure 5, Mode Register (MR) Definition, on page 14. When bit M7 is '1,' no other bits of the mode register are programmed. Programming bit M7 to '1' places the DDR2 SDRAM device into a test mode that is only used by the Manufacturer and should NOT be used. No operation or functionality is guaranteed if M7 bit is '1.'

DLL Reset

DLL reset is defined by bit M8 as shown in Figure 5, Mode Register (MR) Definition, on page 14. Programming bit M8 to '1' will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of '0' after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^tAC or ^tDQSCK parameters.

Write Recovery

Write recovery (WR) time is defined by bits M9–M11 as shown in Figure 5, Mode Register (MR) Definition, on page 14. The WR Register is used by the DDR2 SDRAM device during WRITE with AUTO PRECHARGE operation. During WRITE with AUTO PRECHARGE operation, the DDR2 SDRAM device delays the internal AUTO PRECHARGE operation by WR clocks (programmed in bits M9–M11) from the last data burst.

Write Recovery (WR) values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of write recovery, which is calculated by dividing ^tWR (in ns) by ^tCK (in ns) and rounding up a noninteger value to the next integer; WR [cycles] = ^tWR [ns] / ^tCK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12 as shown in Figure 5, Mode Register (MR) Definition, on page 14. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit M12 does not apply to precharge power-down mode.

When bit M12 = 0, standard Active Power-down mode or 'fast-exit' active power-down mode is enabled. The ^{t}XARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The ^{t}XARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the I$_{DD}$ table.

CAS Latency (CL)

The CAS Latency (CL) is defined by bits M4–M6 as shown in Figure 5, Mode Register (MR) Definition, on page 14. CAS Latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CAS Latency can be set to 3, 4, or 5 clocks. CAS Latency of 2 clocks is a JEDEC optional feature and may be enabled in future speed grades. DDR2 SDRAM devices do not support any half clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM devices also support a feature called Posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD(MIN) by delaying the internal command to the DDR2 SDRAM device by AL clocks. The AL feature is described in more detail in the Extended Mode Register (EMR) and Operational sections.

Examples of CL = 3 and CL = 4 are shown in Figure 6, CAS Latency (CL); both assume AL = 0. If a READ command is registered at clock edge n, and the CAS Latency is m clocks, the data will be available nominally coincident with clock edge $n + m$ (this assumes AL = 0).

Figure 6:   CAS Latency (CL)

Burst length = 4
Posted CAS# additive latency (AL) = 0
Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

TRANSITIONING DATA   DON'T CARE
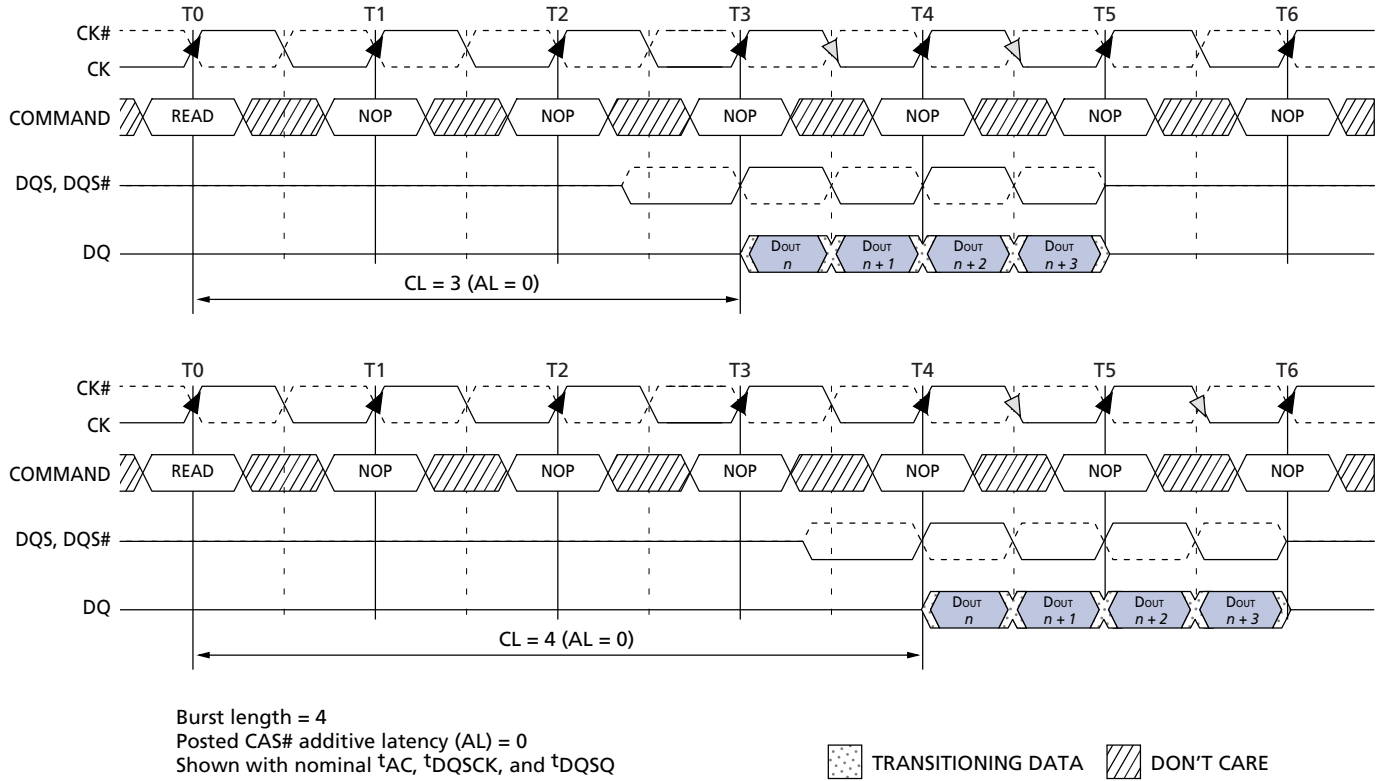
Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (RTT), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT disable/enable. These functions are controlled via the bits shown in Figure 7, Extended Mode Register Definition. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LOAD MODE command as shown in Figure 7, Extended Mode Register Definition. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using a LOAD MODE command.

The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled and reset upon exit of self refresh operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Output Drive Strength

The output drive strength is defined by bit E1 as shown in Figure 7, Extended Mode Register Definition. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (100 percent) drive strength for all outputs. Selecting a reduced drive strength option (bit E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of the lighter load and/or point-to-point environments.

Figure 7: Extended Mode Register Definition

256MB Address Bus

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMR		out	RDQS	DQS#	OCD Program			Rtt	Posted CAS#			Rtt	ODS	DLL

Extended Mode Register (Ex)

512MB Address Bus

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMR		0	out	RDQS	DQS#	OCD Program			Rtt	Posted CAS#			Rtt	ODS	DLL

Extended Mode Register (Ex)

1GB Address Bus

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	EMR		0	out	RDQS	DQS#	OCD Program			Rtt	Posted CAS#			Rtt	ODS	DLL

Extended Mode Register (Ex)

E12	Outputs
0	Enabled
1	Disabled

E11	RDQS Enable
0	Disabled
1	Reserved

E10	DQS# Enable
0	Enable
1	Disable

E9	E8	E7	OCD Operation
0	0	0	OCD Not Supported[†]
0	0	1	Reserved
0	1	0	Reserved
1	0	0	Reserved
1	1	1	OCD default state[†]

E6	E2	Rtt (nominal)
0	0	Rtt Disabled
0	1	75Ω
1	0	150Ω
1	1	50Ω[‡]

E0	DLL Enable
0	Enable (Normal)
1	Disable (Test/Debug)

E1	Output Drive Strength
0	Full Strength
1	Reduced Strength

E5	E4	E3	Posted CAS# Additive Latency (AL)
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

E15	E14	Mode Register Set
0	0	Mode Register Set (MRS)
0	1	Extended Mode Register (EMRS)
1	0	Extended Mode Register (EMRS2)
1	1	Extended Mode Register (EMRS3)

[†]During initialization, all three bits must be set to '1' for OCD Default State, then must be set to '0' before initialization is finished, as detailed in the initialization procedure.
[‡]Available on -667 speed grade parts only.

DQS# Enable/Disable

The DQS# enable function is defined by bit E10. When enabled (bit E10 = 0), DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (bit E10 = 1), DQS is used in a single-ended mode and the DQS# pin is disabled. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled. RDQS/RDQS# is supported only on RDIMMs using x8 DDR2 SDRAM devices.

RDQS Enable/Disable

RDQS/RDQS# is supported only on RDIMMs using x8 DDR2 SDRAM devices. The RDQS enable function is defined by bit E11 as shown in Figure 7, Extended Mode Register Definition, on page 19. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM device.

Output Enable/Disable

The OUTPUT enable function is defined by bit E12 as shown in Figure 7, Extended Mode Register Definition, on page 19. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM device outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled removing output buffer current. The OUTPUT disable feature is intended to be used during I$_{DD}$ characterization of read current.

On Die Termination (ODT)

ODT effective resistance R$_{TT(EFF)}$ is defined by bits E2 and E6 of the EMR as shown in Figure 7, Extended Mode Register Definition, on page 19. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM device controller to independently turn on/off ODT for any or all devices. R$_{TT}$ effective resistance values of 75Ω and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, and DM signals. Additionally, the -667 speed modules offer a third option of 50Ω. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control pin is used to determine when R$_{TT(EFF)}$ is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input pin are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. If SELF REFRESH operation is used, R$_{TT(EFF)}$ should *always* be disabled and the ODT input pin is disabled by the DDR2 SDRAM device. During power-up and initialization of the DDR2 SDRAM device, ODT should be disabled until the EMR command is issued to enable the ODT feature, at which point the ODT pin will determine the R$_{TT(EFF)}$ value. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for ODT timing diagrams.

Off-Chip Driver (OCD) Impedance Calibration

The OCD function is not supported and must be set to the default state. e "Initialization" on page 11, to properly set OCD defaults.
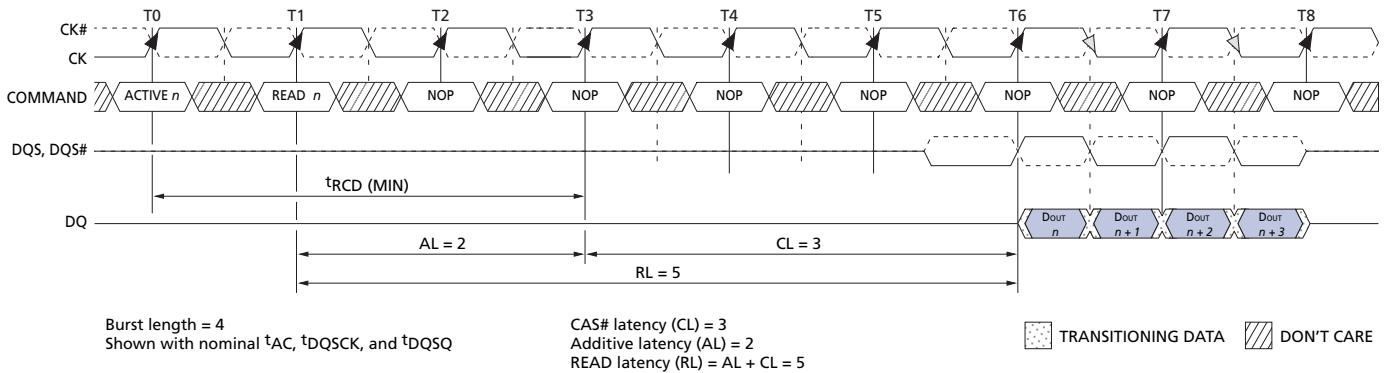
Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM device. Bits E3–E5 define the value of AL as shown in Figure 7, Extended Mode Register Definition, on page 19. Bits E3–E5 allow the user to program the DDR2 SDRAM device with a CAS# additive latency of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM device allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD(MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 x ^{t}CK. The READ or WRITE command is held for the time of the additive latency (AL) before it is issued internally to the DDR2 SDRAM device. READ Latency (RL) is controlled by the sum of the Posted CAS

additive latency (AL) and CAS Latency (CL); RL = AL + CL. Write latency (WL) is equal to READ latency minus one clock; WL = AL + CL - 1 x ^{t}CK. An example of a READ latency is shown in Figure 8, READ Latency. An example of a WRITE latency is shown in Figure 9, Write Latency.

Figure 8: READ Latency

Burst length = 4
Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

CAS# latency (CL) = 3
Additive latency (AL) = 2
READ latency (RL) = AL + CL = 5

TRANSITIONING DATA   DON'T CARE

Figure 9: Write Latency

Burst length = 4

CAS# latency (CL) = 3
Additive latency (AL) = 2
WRITE latency = AL + CL -1 = 4

TRANSITIONING DATA   DON'T CARE
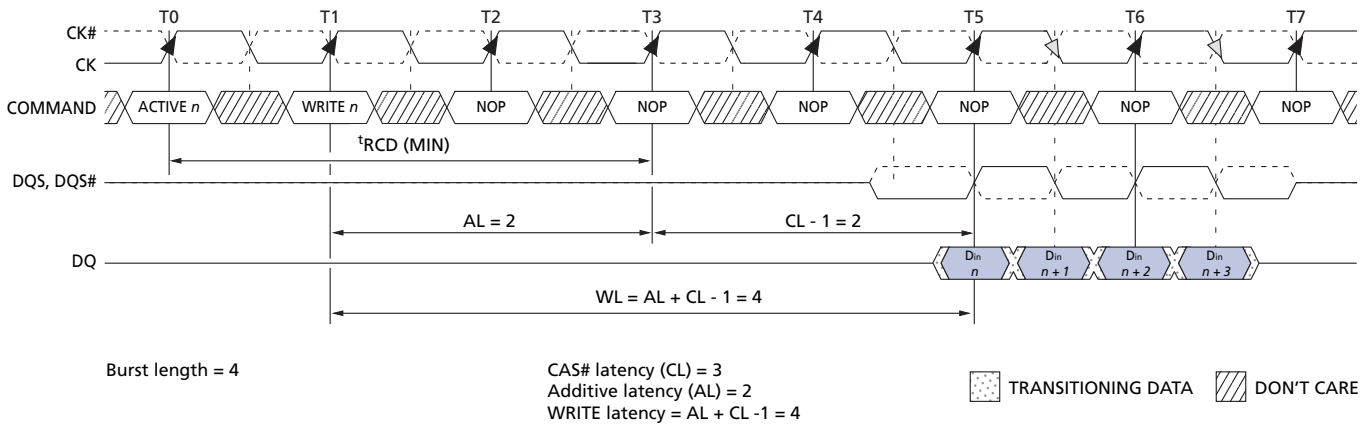
Extended Mode Register 2 (EMR2)

The Extended Mode Register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved as shown in Figure 10, Extended Mode Register 2 (EMR2) Definition. The EMR2 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 10:   Extended Mode Register 2 (EMR2) Definition

E15	E14	Mode Register Set
0	0	Mode Register Set (MRS)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

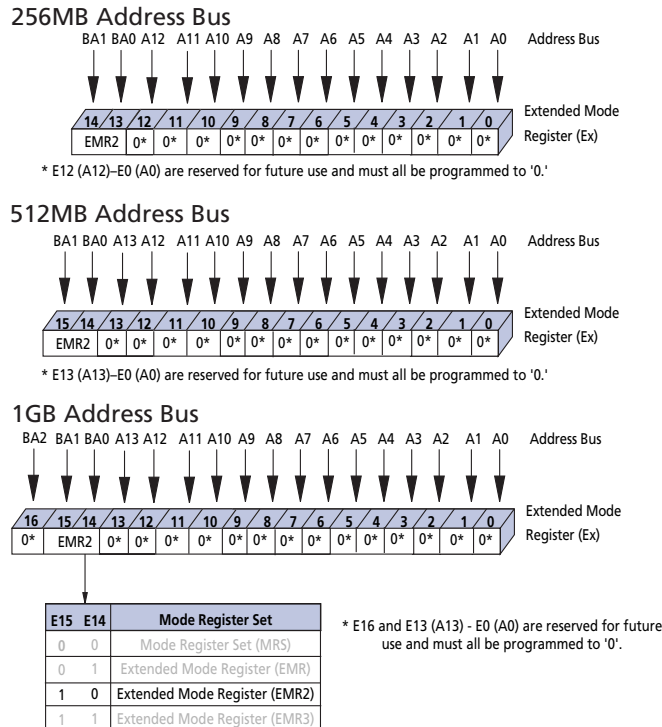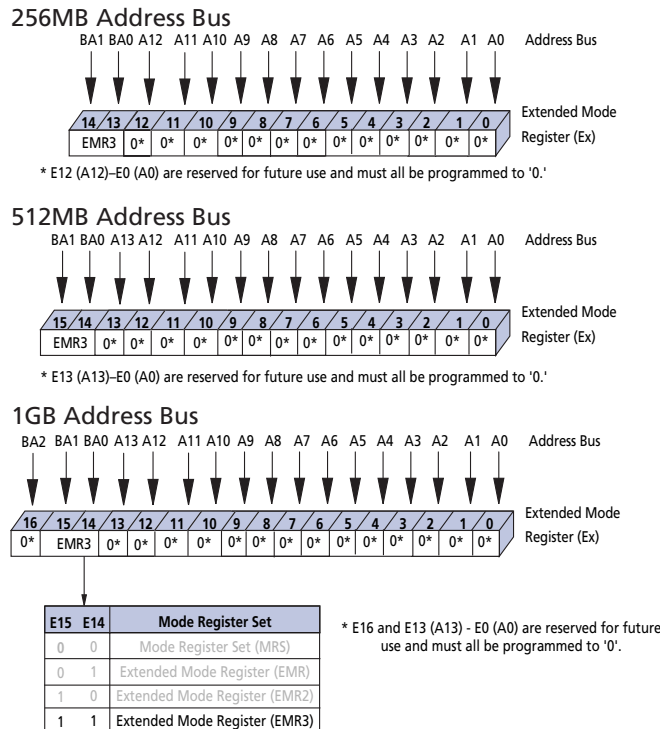* E16 and E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.

Extended Mode Register 3 (EMR3)

The Extended Mode Register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved as shown in Figure 11, Extended Mode Register 3 (EMR3) Definition. The EMR3 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^tMRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 11: Extended Mode Register 3 (EMR3) Definition

256MB Address Bus

* E12 (A12)–E0 (A0) are reserved for future use and must all be programmed to '0.'

512MB Address Bus

* E13 (A13)–E0 (A0) are reserved for future use and must all be programmed to '0.'

1GB Address Bus

* E16 and E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.

E15	E14	Mode Register Set
0	0	Mode Register Set (MRS)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

Command Truth Tables

Table 7, Commands Truth Table provides a quick reference of DDR2 SDRAM device available commands. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM component data sheet for more Truth Table definitions, including CKE power-down modes and device bank-to-bank commands.

Table 7: Commands Truth Table
Notes: 1, 5, 6

Function	CKE		S#	RAS#	CAS#	WE#	BA2[8], BA1, BA0	A13[8]– A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
Mode Register Set	H	H	L	L	L	L	BA	OP Code			2
Refresh	H	H	L	L	L	H	X	X	X	X	
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	
Self Refresh Exit	L	H	X	X	X	X	X	X	X	X	7
			L	H	H	H	X	X	X	X	
Single Device Bank Precharge	H	H	L	L	H	L	BA	X	L	X	2
ALL Device Banks Precharge	H	H	L	L	H	L	X	X	H	X	
Device Bank Activate	H	H	L	L	H	H	BA	Row Address			2
Write	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
Read	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
Read with Auto Precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Power-Down Entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H	X	X	X	X	
Power-Down Exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H	X	X	X	X	

Notes:
1. All DDR2 SDRAM device commands are defined by states of S#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. Device Bank addresses (BA) BA0–BA1/BA2 determine which device bank is to be operated upon. For EMR, BA selects an extended mode register.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for other restrictions or details.
4. The Power Down Mode does not perform any refresh operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM discrete data sheet for other restrictions or details.
6. "X" means "H or L" (but a defined logic level).
7. Self refresh exit is asynchronous.
8. BA2 valid for 1GB only; A13 valid for 512MB and 1GB only.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum DC Ratings

Symbol	Parameter		MIN	MAX	Units
VDD	V_{DD} Supply Voltage Relative to Vss		-1.0	2.3	V
VDDQ	V_{DDQ} Supply Voltage Relative to Vss		-0.5	2.3	V
VDDL	V_{DDL} Supply Voltage Relative to Vss		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any Pin Relative to Vss		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	°C
T_{case}	DDR2 SDRAM Device Operating Temperature (Ambient)		0	85	°C
T_{OPR}	Operating Temperature (Ambient)		0	55	°C
I_I	Input Leakage Current; Any input $0V \leq V_{IN} \leq V_{DD}$; V_{REF} input $0V \leq V_{IN} \leq 0.95V$; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE	-45	45	µA
		CK, CK#	-15	15	
		DM	-5	5	
I_{OZ}	Output Leakage Current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} Leakage Current; V_{REF} = Valid V_{REF} level		-18	18	µA

DC Operating Specifications

Table 9: Recommended DC Operating Conditions

All voltages referenced to Vss

Parameter	Symbol	MIN	NOM	MAX	Units	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	1
V_{DDL} Supply Voltage	V_{DDL}	1.7	1.8	1.9	V	4
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	4
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3

Notes: 1. V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.