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MT9M021, MT9M031

MT9M021/MT9M031 1/3-inch CMOS Digital Image Sensor

Description

The MT9M021/MT9M031 from ON Semiconductor is a 1/3-inch CMOS digital image sensor with an active-pixel array of 1280 (H) × 960 (V). It includes sophisticated camera functions such as auto exposure control, windowing, scaling, row skip mode, and both video and single frame modes. It is designed for low light performance and features a global shutter for accurate capture of moving scenes. It is programmable through a simple two-wire serial interface. The MT9M021/MT9M031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and HD video.

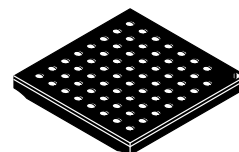
Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/3-inch (6 mm)
Active Pixels	1280 (H) × 960 (V) = 1.2 Mp
Pixel Size	3.75 μm
Color Filter Array	RGB Bayer or Monochrome
Shutter Type	Global Shutter
Input Clock Range	6–50 MHz
Output Pixel Clock (Maximum)	74.25 MHz
Output Serial Parallel	HiSPi (iBGA Package Only) 12-bit
Frame Rate Full Resolution 720p	45 fps 60 fps
Responsivity Monochrome Color	6.1 V/lux-sec 5.3 V/lux-sec
SNR _{MAX}	38 dB
Dynamic Range	64 dB
Supply Voltage I/O Digital Analog HiSPi	1.8 or 2.8 V 1.8 V 2.8 V 0.4 V
Power Consumption	< 400 mW
Operating Temperature (Ambient)	-30°C to + 70°C
Package Options	9 × 9 mm 63-pin iBGA 10 × 10 mm 48-pin iLCC

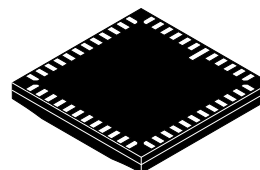


ON Semiconductor®

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**iBGA63 9 × 9
CASE 503AQ**



**iLCC48 10 × 10
CASE 847AJ**

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Superior Low-light Performance
- HD Video (720p60)
- Global Shutter
- Video/Single Frame Mode
- Flexible Row-skip Modes
- On-chip AE and Statistics Engine
- Parallel and Serial Output
- Support for External LED or Flash
- Auto Black Level Calibration
- Context Switching

Applications

- Scene Processing
- Scanning and Machine Vision
- 720p60 Video Applications

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ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9M021IA3XTC-DPBR1	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M021IA3XTC-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M021IA3XTM-DPBR1	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M021IA3XTM-DRBR1	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M021IA3XTMZ-DPBR	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M021IA3XTMZ-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M021IA3XTMZ-TPBR	1.2 MP 1/3" GS CIS	Tape & Reel with Protective Film, Double Side BBAR Glass
MT9M031D00STMC24BC1-200	1 MP 1/6" SOC	Die Sales, 200 μm Thickness
MT9M031112STC-DPBR1	1 MP 1/6" SOC	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M031112STC-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M031112STM-DPBR	1.2 MP 1/3" GS CIS	Dry Pack with Protective Film, Double Side BBAR Glass
MT9M031112STM-DRBR1	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass
MT9M031112STMZ-DRBR	1.2 MP 1/3" GS CIS	Dry Pack without Protective Film, Double Side BBAR Glass

See the ON Semiconductor Device Nomenclature document ([TND310/D](#)) for a full description of the naming convention used for image sensors. For reference

documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

GENERAL DESCRIPTION

The ON Semiconductor MT9M021/MT9M031 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 45 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (HiSPi) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock.

A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

The MT9M021/MT9M031 includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, and row skip and digital binning modes.

The sensor is designed to operate in a wide temperature range (-30°C to +70°C).

FUNCTIONAL OVERVIEW

The MT9M021/MT9M031 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from

a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

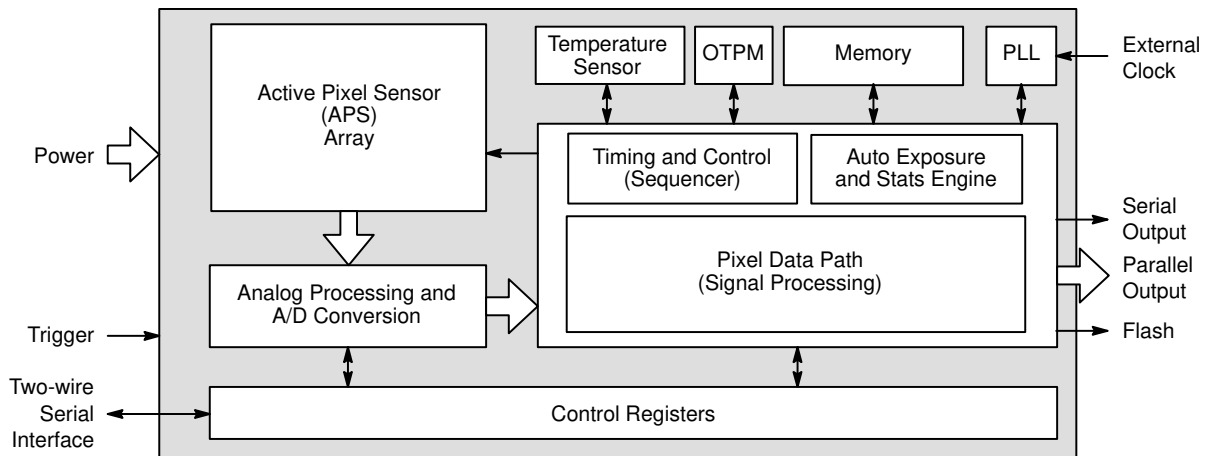


Figure 1. Block Diagram

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User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active-Pixel Sensor array. The MT9M021/MT9M031 features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data

from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

FEATURES OVERVIEW

The MT9M021/MT9M031 Global Sensor shutter has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the MT9M021/MT9M031 Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- Operating Modes

The MT9M021/MT9M031 works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.

NOTE: Trigger mode is not compatible with the HiSPi interface.

- Window Control

Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.

- Context Switching

Context switching may be used to rapidly switch between two sets of register values. Refer to the MT9M021/MT9M031 Developer Guide for a complete set of context switchable registers.

- Gain

The MT9M021/MT9M031 Global Shutter sensor can be configured for analog gain of up to 8x, and digital gain of up to 8x.

- Automatic Exposure Control

The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the MT9M021/MT9M031 Developer Guide for more details.

- HiSPi

The MT9M021/MT9M031 Global Shutter image sensor supports two or three lanes of Streaming-SP or Packetized-SP protocols of ON Semiconductor's High-Speed Serial Pixel Interface.

- PLL

An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.

- Reset

The MT9M021/MT9M031 may be reset by a register write, or by a dedicated input pin.

- Output Enable

The MT9M021/MT9M031 output pins may be tri-stated using a dedicated output enable pin.

- Temperature Sensor

- Black Level Correction

- Row Noise Correction

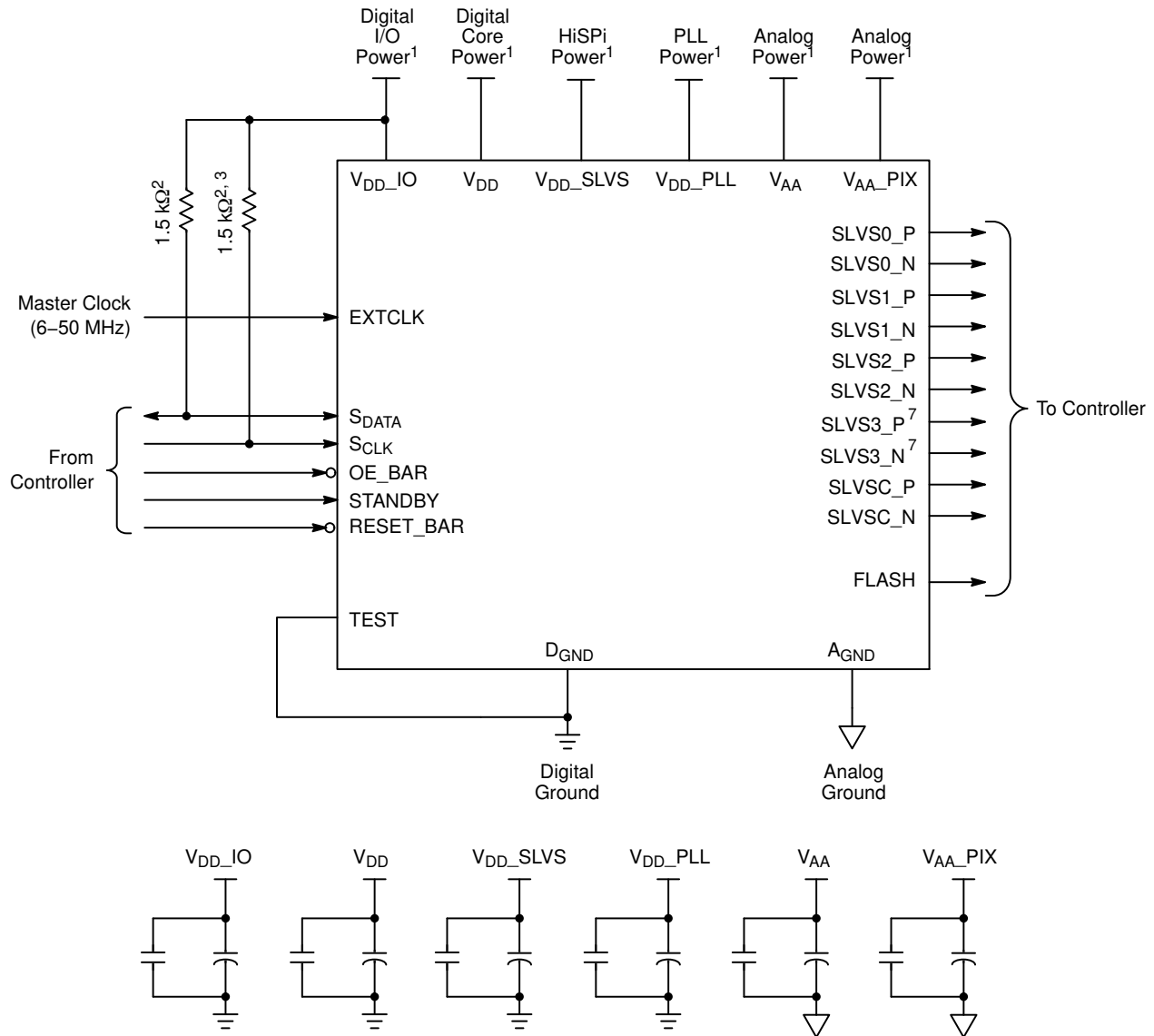
- Column Correction

- Test Patterns

Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to grey, and a walking 1s test pattern.

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TYPICAL CONFIGURATION AND PINOUT

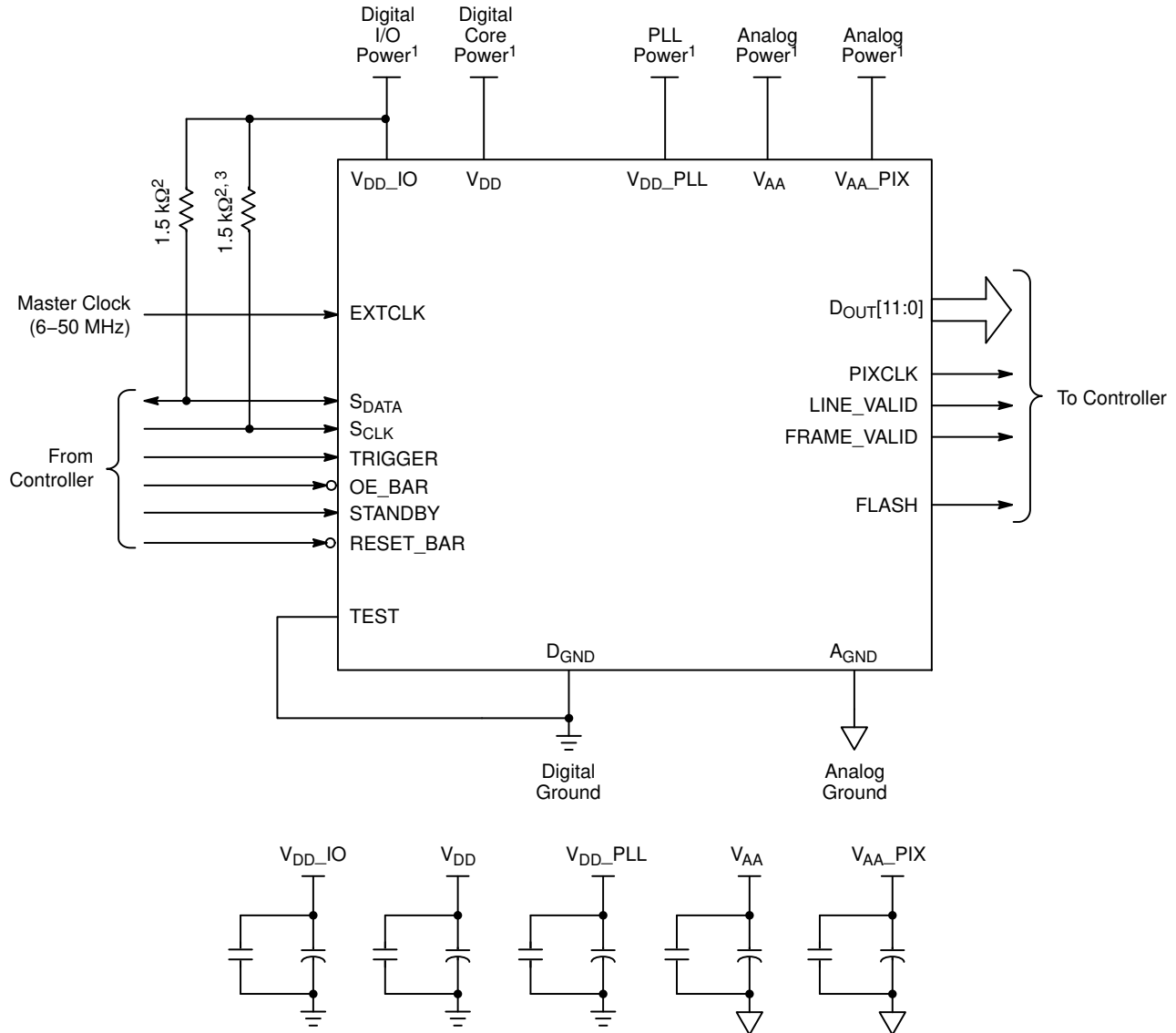


Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the MT9M021/MT9M031 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
7. Although 4 serial lanes are shown, the MT9M021/MT9M031 supports only 2- or 3-lane HiSPi.

Figure 2. Serial 4-lane HiSPi Interface

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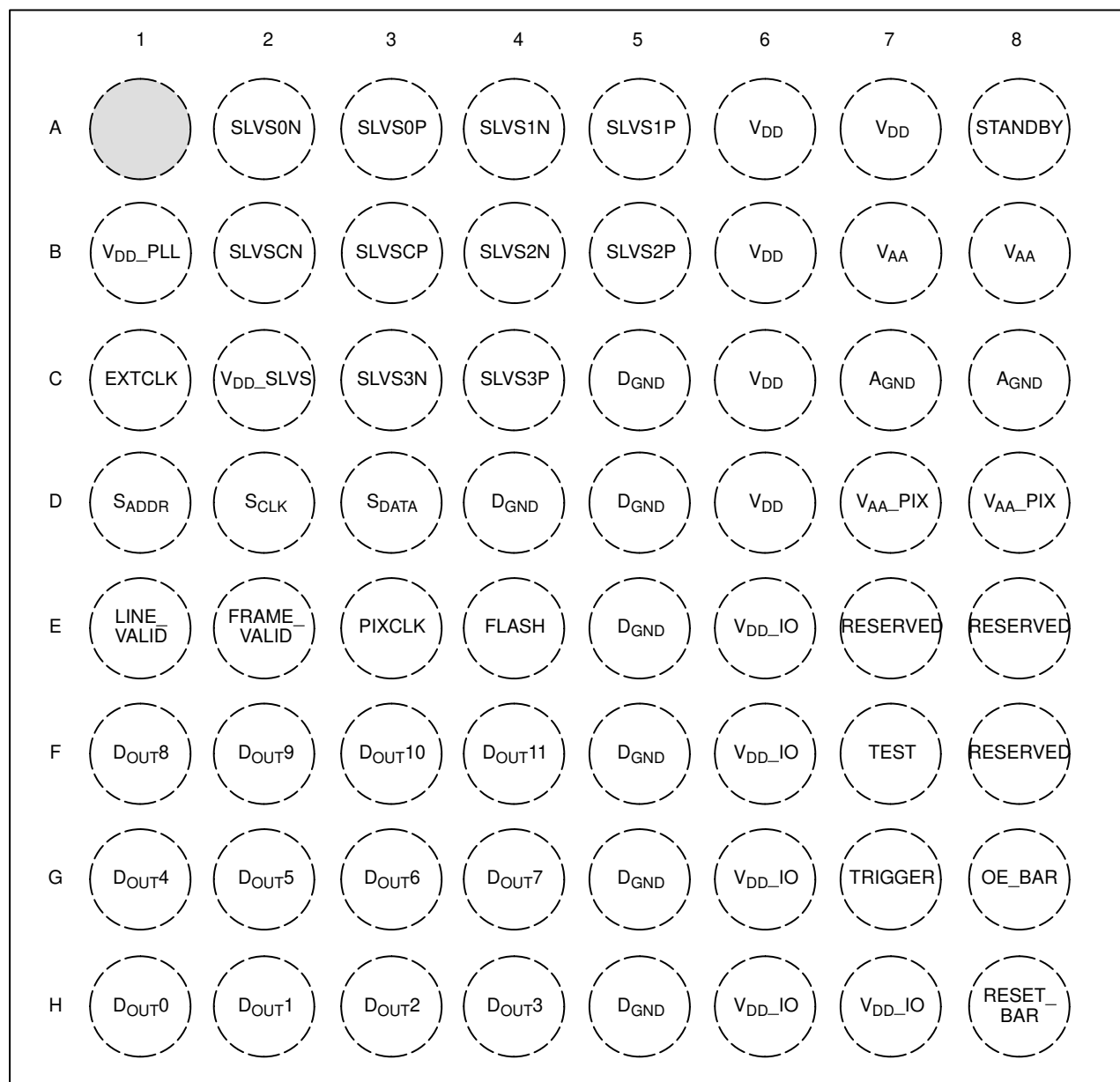


Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the MT9M021/MT9M031 demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 3. Parallel Pixel Data Interface

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Top View
(Ball Down)

Figure 4. 9 × 9 mm 63-ball iBGA Package

Table 3. PIN DESCRIPTIONS – 63-BALL IBGA PACKAGE

Name	iBGA Pin	Type	Description
SLVS0_N	A2	Output	HiSPi serial data, lane 0, differential N
SLVS0_P	A3	Output	HiSPi serial data, lane 0, differential P
SLVS1_N	A4	Output	HiSPi serial data, lane 1, differential N
SLVS1_P	A5	Output	HiSPi serial data, lane 1, differential P
STANDBY	A8	Input	Standby-mode enable pin (active HIGH)
VDD_PLL	B1	Power	PLL power
SLVSC_N	B2	Output	HiSPi serial DDR clock differential N

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Table 3. PIN DESCRIPTIONS – 63-BALL IBGA PACKAGE (continued)

Name	iBGA Pin	Type	Description
SLVSC_P	B3	Output	HiSPi serial DDR clock differential P
SLVS2_N	B4	Output	HiSPi serial data, lane 2, differential N
SLVS2_P	B5	Output	HiSPi serial data, lane 2, differential P
V _{AA}	B7, B8	Power	Analog power
EXTCLK	C1	Input	External input clock
V _{DD_SLVS}	C2	Power	HiSPi power
SLVS3_N	C3	Output	HiSPi serial data, lane 3, differential N
SLVS3_P	C4	Output	HiSPi serial data, lane 3, differential P
D _{GND}	C5, D4, D5, E5, F5, G5, H5	Power	Digital GND
V _{DD}	A6, A7, B6, C6, D6	Power	Digital power
A _{GND}	C7, C8	Power	Analog GND
S _{ADDR}	D1	Input	Two-Wire Serial address select
S _{CLK}	D2	Input	Two-Wire Serial clock input
S _{DATA}	D3	I/O	Two-Wire Serial data I/O
V _{AA_PIX}	D7, D8	Power	Pixel power
LINE_VALID	E1	Output	Asserted when D _{OUT} line data is valid
FRAME_VALID	E2	Output	Asserted when D _{OUT} frame data is valid
PIXCLK	E3	Output	Pixel clock out. D _{OUT} is valid on rising edge of this clock
FLASH	E4	Output	Control signal to drive external light sources
V _{DD_IO}	E6, F6, G6, H6, H7	Power	I/O supply power
D _{OUT8}	F1	Output	Parallel pixel data output
D _{OUT9}	F2	Output	Parallel pixel data output
D _{OUT10}	F3	Output	Parallel pixel data output
D _{OUT11}	F4	Output	Parallel pixel data output (MSB)
TEST	F7	Input	Manufacturing test enable pin (connect to D _{GND})
D _{OUT4}	G1	Output	Parallel pixel data output
D _{OUT5}	G2	Output	Parallel pixel data output
D _{OUT6}	G3	Output	Parallel pixel data output
D _{OUT7}	G4	Output	Parallel pixel data output
TRIGGER	G7	Input	Exposure synchronization input
OE_BAR	G8	Input	Output enable (active LOW)
D _{OUT0}	H1	Output	Parallel pixel data output (LSB)
D _{OUT1}	H2	Output	Parallel pixel data output
D _{OUT2}	H3	Output	Parallel pixel data output
D _{OUT3}	H4	Output	Parallel pixel data output
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default
Reserved	E7, E8, F8	N/A	Reserved (do not connect)

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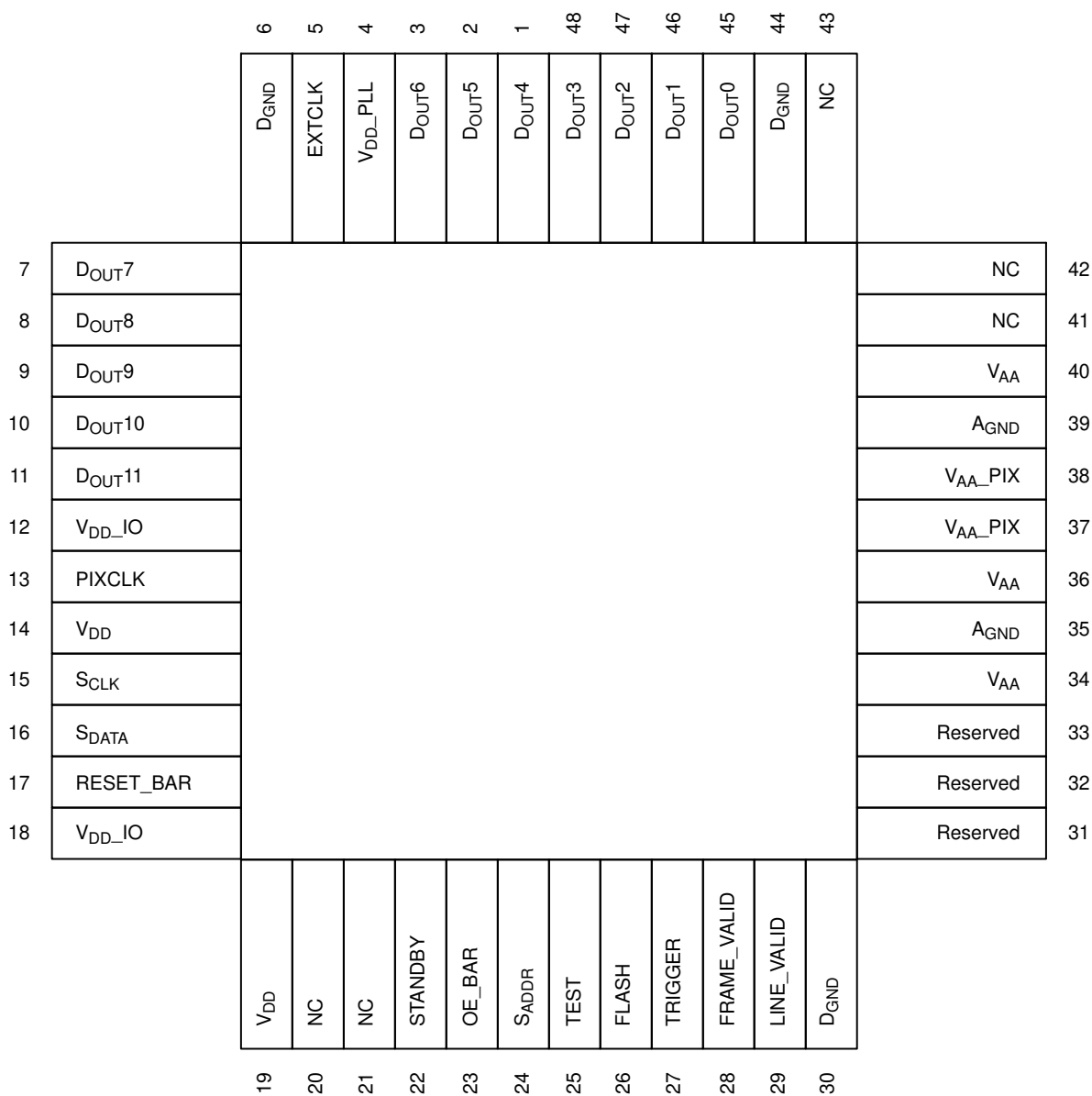


Figure 5. 10 × 10 mm 48-pin iLCC Package, Parallel Output

Table 4. PIN DESCRIPTIONS – 48-PIN ILCC PACKAGE, PARALLEL

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel pixel data output
2	DOUT5	Output	Parallel pixel data output
3	DOUT6	Output	Parallel pixel data output
4	VDD_PLL	Power	PLL power
5	EXTCLK	Input	External input clock
6	D_GND	Power	Digital ground
7	DOUT7	Output	Parallel pixel data output
8	DOUT8	Output	Parallel pixel data output
9	DOUT9	Output	Parallel pixel data output

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Table 4. PIN DESCRIPTIONS – 48-PIN ILCC PACKAGE, PARALLEL (continued)

Pin Number	Name	Type	Description
10	D _{OUT} 10	Output	Parallel pixel data output
11	D _{OUT} 11	Output	Parallel pixel data output (MSB)
12	V _{DD_IO}	Power	I/O supply power
13	PIXCLK	Output	Pixel clock out. D _{OUT} is valid on rising edge of this clock
14	V _{DD}	Power	Digital power
15	S _{CLK}	Input	Two-Wire Serial clock input
16	S _{DATA}	I/O	Two-Wire Serial data I/O
17	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default
18	V _{DD_IO}	Power	I/O supply power
19	V _{DD}	Power	Digital power
20	NC		No connection
21	NC		No connection
22	STANDBY	Input	Standby-mode enable pin (active HIGH)
23	OE_BAR	Input	Output enable (active LOW)
24	S _{ADDR}	Input	Two-Wire Serial address select
25	TEST	Input	Manufacturing test enable pin (connect to D _{GND})
26	FLASH	Output	Flash output control
27	TRIGGER	Input	Exposure synchronization input
28	FRAME_VALID	Output	Asserted when D _{OUT} frame data is valid
29	LINE_VALID	Output	Asserted when D _{OUT} line data is valid
30	D _{GND}	Power	Digital ground
31	Reserved	N/A	Reserved (do not connect)
32	Reserved	N/A	Reserved (do not connect)
33	Reserved	N/A	Reserved (do not connect)
34	V _{AA}	Power	Analog power
35	A _{GND}	Power	Analog ground
36	V _{AA}	Power	Analog power
37	V _{AA_PIX}	Power	Pixel power
38	V _{AA_PIX}	Power	Pixel power
39	A _{GND}	Power	Analog ground
40	V _{AA}	Power	Analog power
41	NC		No connection
42	NC		No connection
43	NC		No connection
44	D _{GND}	Power	Digital ground
45	D _{OUT} 0	Output	Parallel pixel data output (LSB)
46	D _{OUT} 1	Output	Parallel pixel data output
47	D _{OUT} 2	Output	Parallel pixel data output
48	D _{OUT} 3	Output	Parallel pixel data output

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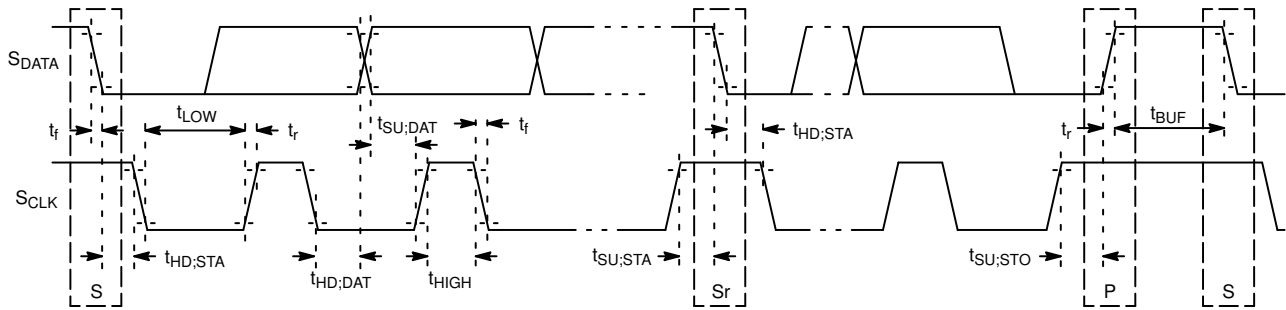
ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply to the following conditions:

$V_{DD} = 1.8 \text{ V } -0.10/+0.15$;
 $V_{DD_IO} = V_{DD_PLL} = V_{AA} = V_{AA_PIX} = 2.8 \text{ V } \pm 0.3 \text{ V}$;
 $V_{DD_SLVS} = 0.4 \text{ V } -0.1/+0.2$;
 $T_A = -30^\circ\text{C to } +70^\circ\text{C}$;
 Output Load = 10 pF;
 PIXCLK Frequency = 74.25 MHz;
 HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (S_{CLK} , S_{DATA}) are shown in Figure 6 and Table 5.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 6. Two-Wire Serial Bus Timing Parameters

Table 5. TWO-WIRE SERIAL BUS CHARACTERISTICS

($f_{EXTCLK} = 27 \text{ MHz}$; $V_{DD} = 1.8 \text{ V}$; $V_{DD_IO} = 2.8 \text{ V}$; $V_{AA} = 2.8 \text{ V}$; $V_{AA_PIX} = 2.8 \text{ V}$; $V_{DD_PLL} = 2.8 \text{ V}$; $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Standard Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW Period of the S_{CLK} Clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH Period of the S_{CLK} Clock	t_{HIGH}	4.0	–	0.6	–	μs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data Hold Time	$t_{HD;DAT}$	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	μs
Data Set-up Time	$t_{SU;DAT}$	250	–	100 (Note 6)	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	$20 + 0.1C_b$ (Note 7)	300	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	$20 + 0.1C_b$ (Note 7)	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive Load for each Bus Line	C_b	–	400	–	400	pF
Serial Interface Input Pin Capacitance	C_{IN_SI}	–	3.3	–	3.3	pF

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Table 5. TWO-WIRE SERIAL BUS CHARACTERISTICS (continued)

($f_{EXTCLK} = 27\text{ MHz}$; $V_{DD} = 1.8\text{ V}$; $V_{DD_IO} = 2.8\text{ V}$; $V_{AA} = 2.8\text{ V}$; $V_{AA_PIX} = 2.8\text{ V}$; $V_{DD_PLL} = 2.8\text{ V}$; $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Standard Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
S _{DATA} Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
S _{DATA} Pull-up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I²C-compatible.
3. All values referred to $V_{IHmin} = 0.9 V_{DD_IO}$ and $V_{ILmax} = 0.1 V_{DD_IO}$ levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
5. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU,DAT} 250\text{ ns}$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line $t_r\text{ max} + t_{SU,DAT} = 1000 + 250 = 1250\text{ ns}$ (according to the Standard-mode I²C-bus specification) before the S_{CLK} line is released.
7. C_b = total capacitance of one bus line in pF.

I/O Timing

By default, the MT9M021/MT9M031 launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures D_{OUT}[11:0], FV and LV

using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 7 and Table 6 for I/O timing (AC) characteristics.

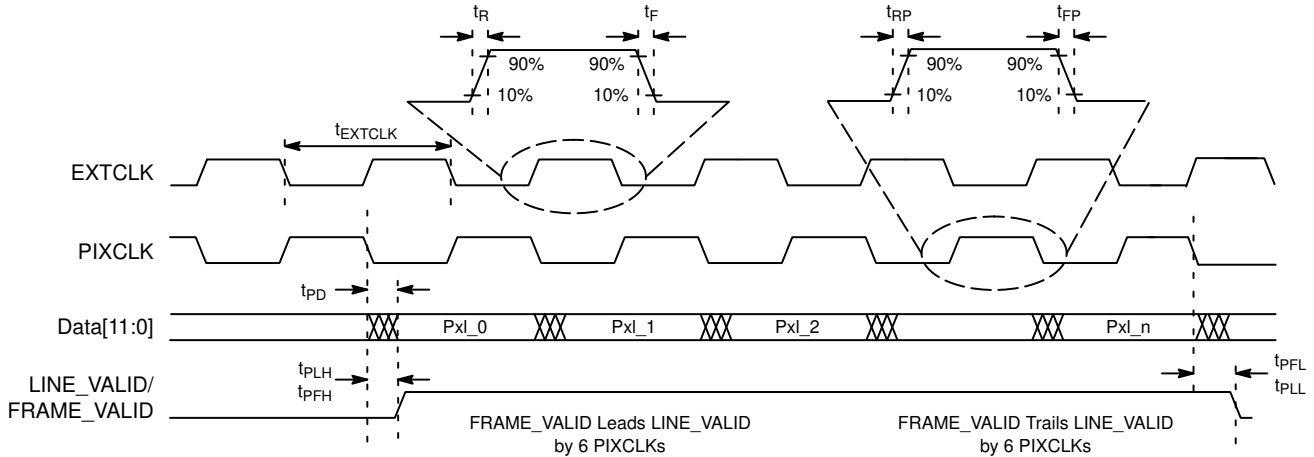


Figure 7. I/O Timing Diagram

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Table 6. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (1.8 V V_{DD_IO}) (Note 1)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f _{EXTCLK}	Input Clock Frequency		6	–	50	MHz
t _{EXTCLK}	Input Clock Period		20	–	166	ns
t _R	Input Clock Rise Time	PLL Enabled	–	3	4	ns
t _F	Input Clock Fall Time	PLL Enabled	–	3	4	ns
t _{RP}	PIXCLK Rise Time	Slew Setting = 4 (Default)	2.3	–	4.6	ns
t _{FP}	PIXCLK Fall Time	Slew Setting = 4 (Default)	3	–	4.4	ns
	PIXCLK Duty Cycle		40	50	60	%
f _{PIXCLK}	PIXCLK Frequency (Note 2)	Nominal Voltages, PLL Enabled	6	–	74.25	MHz
t _{PD}	PIXCLK to Data Valid	Nominal Voltages, PLL Enabled	–3	2.3	4.5	ns
t _{PFH}	PIXCLK to FV HIGH	Nominal Voltages, PLL Enabled	–3	1.5	4.5	ns
t _{PLH}	PIXCLK to LV HIGH	Nominal Voltages, PLL Enabled	–3	2.3	4.5	ns
t _{PFL}	PIXCLK to FV LOW	Nominal Voltages, PLL Enabled	–3	1.5	4.5	ns
t _{PLL}	PIXCLK to LV LOW	Nominal Voltages, PLL Enabled	–3	2	4.5	ns

1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD_IO}, and –30°C at 110% of V_{DD_IO}. All values are taken at the 50% transition point. The loading used is 20 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 7. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (2.8 V V_{DD_IO}) (Note 1)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f _{EXTCLK}	Input Clock Frequency		6	–	50	MHz
t _{EXTCLK}	Input Clock Period		20	–	166	ns
t _R	Input Clock Rise Time	PLL Enabled	–	3	4	ns
t _F	Input Clock Fall Time	PLL Enabled	–	3	4	ns
t _{RP}	PIXCLK Rise Time	Slew Setting = 4 (Default)	2.3	–	4.6	ns
t _{FP}	PIXCLK Fall Time	Slew Setting = 4 (Default)	3	–	4.4	ns
	PIXCLK Duty Cycle		40	50	60	%
f _{PIXCLK}	PIXCLK Frequency (Note 2)	Nominal Voltages, PLL Enabled	6	–	74.25	MHz
t _{PD}	PIXCLK to Data Valid	Nominal Voltages, PLL Enabled	–3	2.3	4	ns
t _{PFH}	PIXCLK to FV HIGH	Nominal Voltages, PLL Enabled	–3	1.5	4	ns
t _{PLH}	PIXCLK to LV HIGH	Nominal Voltages, PLL Enabled	–3	2.3	4	ns
t _{PFL}	PIXCLK to FV LOW	Nominal Voltages, PLL Enabled	–3	1.5	4	ns
t _{PLL}	PIXCLK to LV LOW	Nominal Voltages, PLL Enabled	–3	2	4	ns

1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD_IO}, and –30°C at 110% of V_{DD_IO}. All values are taken at the 50% transition point. The loading used is 20 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 8. I/O RISE SLEW RATE (2.8 V V_{DD_IO}) (Note 1)

Parallel Slew (R0x306E[15:13])	Condition	Min	Typ	Max	Unit
7	Default	1.08	1.77	2.72	V/ns
6	Default	0.77	1.26	1.94	V/ns
5	Default	0.58	0.95	1.46	V/ns
4	Default	0.44	0.70	1.08	V/ns
3	Default	0.32	0.51	0.78	V/ns
2	Default	0.23	0.37	0.56	V/ns
1	Default	0.16	0.25	0.38	V/ns
0	Default	0.10	0.15	0.22	V/ns

1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD_IO}, and –30°C at 110% of V_{DD_IO}. All values are taken at the 50% transition point. The loading used is 20 pF.

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Table 9. I/O FALL SLEW RATE (2.8 V V_{DD_IO}) (Note 1)

Parallel Slew (R0x306E[15:13])	Condition	Min	Typ	Max	Unit
7	Default	1.00	1.62	2.41	V/ns
6	Default	0.76	1.24	1.88	V/ns
5	Default	0.60	0.98	1.50	V/ns
4	Default	0.46	0.75	1.16	V/ns
3	Default	0.35	0.56	0.86	V/ns
2	Default	0.25	0.40	0.61	V/ns
1	Default	0.17	0.27	0.41	V/ns
0	Default	0.11	0.16	0.24	V/ns

1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD_IO} , and -30°C at 110% of V_{DD_IO} . All values are taken at the 50% transition point. The loading used is 20 pF.

Table 10. I/O RISE SLEW RATE (1.8 V V_{DD_IO}) (Note 1)

Parallel Slew (R0x306E[15:13])	Condition	Min	Typ	Max	Unit
7	Default	0.41	0.65	1.10	V/ns
6	Default	0.30	0.47	0.79	V/ns
5	Default	0.24	0.37	0.61	V/ns
4	Default	0.19	0.28	0.46	V/ns
3	Default	0.14	0.21	0.34	V/ns
2	Default	0.10	0.15	0.24	V/ns
1	Default	0.07	0.10	0.16	V/ns
0	Default	0.04	0.06	0.10	V/ns

1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD_IO} , and -30°C at 110% of V_{DD_IO} . All values are taken at the 50% transition point. The loading used is 20 pF.

Table 11. I/O FALL SLEW RATE (1.8 V V_{DD_IO}) (Note 1)

Parallel Slew (R0x306E[15:13])	Condition	Min	Typ	Max	Unit
7	Default	0.42	0.68	1.11	V/ns
6	Default	0.32	0.51	0.84	V/ns
5	Default	0.26	0.41	0.67	V/ns
4	Default	0.20	0.32	0.52	V/ns
3	Default	0.16	0.24	0.39	V/ns
2	Default	0.12	0.18	0.28	V/ns
1	Default	0.08	0.12	0.19	V/ns
0	Default	0.05	0.07	0.11	V/ns

1. Minimum and maximum values are taken at the temperature and voltage limits; for instance, 70°C ambient at 90% of V_{DD_IO} , and -30°C at 110% of V_{DD_IO} . All values are taken at the 50% transition point. The loading used is 20 pF.

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DC Electrical Characteristics

The DC electrical characteristics are shown in Table 12, Table 13, Table 14, and Table 15.

Table 12. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V _{DD}	Core Digital Voltage		1.7	1.8	1.95	V
V _{DD_IO}	I/O Digital Voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V _{AA}	Analog Voltage		2.5	2.8	3.1	V
V _{AA_PIX}	Pixel Supply Voltage		2.5	2.8	3.1	V
V _{DD_PLL}	PLL Supply Voltage		2.5	2.8	3.1	V
V _{DD_SLVS}	HiSPi Supply Voltage		0.3	0.4	0.6	V
V _{IH}	Input HIGH Voltage		V _{DD_IO} * 0.7	–	–	V
V _{IL}	Input LOW Voltage		–	–	V _{DD_IO} * 0.3	V
I _{IN}	Input Leakage Current	No Pull-up Resistor; V _{IN} = V _{DD_IO} or D _{GND}	20	–	–	μA
V _{OH}	Output HIGH Voltage		V _{DD_IO} – 0.3	–	–	V
V _{OL}	Output LOW Voltage	V _{DD_IO} = 2.8 V	–	–	0.4	V
I _{OH}	Output HIGH Current	At Specified V _{OH}	–22	–	–	mA
I _{OL}	Output LOW Current	At Specified V _{OL}	–	–	22	mA

CAUTION: Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 13. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Unit
V _{SUPPLY}	Power Supply Voltage (All Supplies)	–0.3	4.5	V
I _{SUPPLY}	Total Power Supply Current	–	200	mA
I _{GND}	Total Ground Current	–	200	mA
V _{IN}	DC Input Voltage	–0.3	V _{DD_IO} + 0.3	V
V _{OUT}	DC Output Voltage	–0.3	V _{DD_IO} + 0.3	V
T _{STG}	Storage Temperature (Note 1)	–40	+85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 14. OPERATING CURRENT CONSUMPTION FOR PARALLEL OUTPUT

(V_{AA} = V_{AA_PIX} = V_{DD_IO} = V_{DD_PLL} = 2.8 V; V_{DD} = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; T_A = 25°C; C_{LOAD} = 10 pF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{DD}	Digital Operating Current	Parallel, Streaming, Full Resolution 45 fps	–	45	55	mA
I _{DD_IO}	I/O Digital Operating Current	Parallel, Streaming, Full Resolution 45 fps	–	50 (Note 1)	–	mA
I _{AA}	Analog Operating Current	Parallel, Streaming, Full Resolution 45 fps	–	45	50	mA
I _{AA_PIX}	Pixel Supply Current	Parallel, Streaming, Full Resolution 45 fps	–	6	10	mA
I _{DD_PLL}	PLL Supply Current	Parallel, Streaming, Full Resolution 45 fps	–	6	8	mA

1. I_{DD_IO} operating current is specified with image at 1/2 saturation level.

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Table 15. STANDBY CURRENT CONSUMPTION

(Analog – $V_{AA} + V_{AA_PIX} + V_{DD_PLL}$; Digital – $V_{DD} + V_{DD_IO}$; $T_A = 25^\circ\text{C}$)

Definition	Condition	Min	Typ	Max	Unit
Hard Standby (Clock Off, Driven Low)	Analog, 2.8 V	–	3	10	μA
	Digital, 1.8 V	–	8	75	μA
Hard Standby (Clock On, EXTCLK = 20 MHz)	Analog, 2.8 V	–	12	20	μA
	Digital, 1.8 V	–	0.87	1.3	mA
Soft Standby (Clock Off, Driven Low)	Analog, 2.8 V	–	3	10	μA
	Digital, 1.8 V	–	8	75	μA
Soft Standby (Clock On, EXTCLK = 20 MHz)	Analog, 2.8 V	–	12	20	μA
	Digital, 1.8 V	–	0.87	1.3	mA

HiSPi Electrical Specifications

The ON Semiconductor MT9M021/MT9M031 sensor supports SLVS mode only, and does not have a DLL for timing adjustments. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing

information. The V_{DD_SLVS} supply in this data sheet corresponds to V_{DD_TX} in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD_HiSPi} as referenced in the specification. The HiSPi transmitter electrical specifications are listed at 700 MHz.

Table 16. INPUT VOLTAGE AND CURRENT (HiSPi POWER SUPPLY 0.4 V)

(Measurement Conditions: Max Freq. 700 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
I_{DD_SLVS}	Supply Current (PWR_{HiSPi}) (Driving 100 Ω Load)	–	10	15	mA
V_{CMD}	HiSPi Common Mode Voltage (Driving 100 Ω Load)	$V_{DD_SLVS} \times 0.45$	$V_{DD_SLVS}/2$	$V_{DD_SLVS} \times 0.55$	V
$ V_{OD} $	HiSPi Differential Output Voltage (Driving 100 Ω Load)	$V_{DD_SLVS} \times 0.36$	$V_{DD_SLVS}/2$	$V_{DD_SLVS} \times 0.64$	V
ΔV_{CM}	Change in V_{CM} between Logic 1 and 0	–	–	25	mV
$ V_{OD} $	Change in $ V_{OD} $ between Logic 1 and 0	–	–	25	mV
NM	V_{OD} Noise Margin	–	–	30	%
$ \Delta V_{CM} $	Difference in V_{CM} between any Two Channels	–	–	50	mV
$ \Delta V_{OD} $	Difference in V_{OD} between any Two Channels	–	–	100	mV
ΔV_{CM_ac}	Common-mode AC Voltage (pk) without V_{CM} Cap Termination	–	–	50	mV
ΔV_{CM_ac}	Common-mode AC Voltage (pk) with V_{CM} Cap Termination	–	–	30	mV
V_{OD_ac}	Max Overshoot Peak $ V_{OD} $	–	–	$1.3 \times V_{OD} $	V
V_{diff_pkpk}	Max Overshoot V_{diff} pk-pk	–	–	$2.6 \times V_{OD} $	V
V_{eye}	Eye Height	$1.4 \times V_{OD}$	–	–	
R_o	Single-ended Output Impedance	35	50	70	Ω
ΔR_o	Output Impedance Mismatch	–	–	20	%

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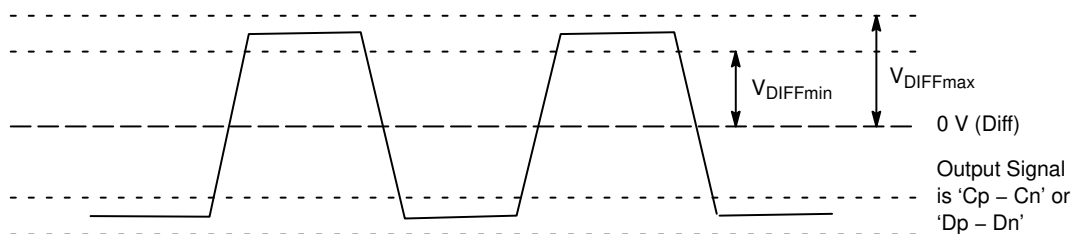


Figure 8. Differential Output Voltage for Clock and Data Pairs

Table 17. RISE AND FALL TIMES

(Measurement Conditions: HiSPi Power Supply 0.4 V, Max Freq. 700 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
1/UI	Data Rate	280	–	700	Mb/s
TxPRE	Max Setup Time from Transmitter (Note 1)	0.3	–	–	UI
TxPost	Max Hold Time from Transmitter	0.3	–	–	UI
RISE	Rise Time (20–80%)	–	0.25 UI	–	
FALL	Fall Time (20–80%)	150 ps	0.25 UI	–	
PLL_DUTY	Clock Duty	45	50	55	%
t _{pw}	Bitrate Period (Note 1)	1.43	–	3.57	ns
t _{eye}	Eye Width (Notes 1, 2)	0.3	–	–	UI
t _{totaljit}	Data Total Jitter (pk pk)@1e–9 (Notes 1, 2)	–	–	0.2	UI
t _{ckjit}	Clock Period Jitter (RMS) (Note 2)	–	–	50	ps
t _{cyj}	Clock Cycle to Cycle Jitter (RMS) (Note 2)	–	–	100	ps
t _{chskew}	Clock to Data Skew (Notes 1, 2)	–0.1	–	0.1	UI
t _{PHYskew}	PHY-to-PHY Skew (Notes 1, 5)	–	–	2.1	UI
t _{DIFFSKEW}	Mean Differential Skew (Note 6)	–100	–	100	ps

1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Taken from 0 V crossing point.
3. Also defined with a maximum loading capacitance of 10 pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3 UI.
4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
5. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean V_{CM} point.

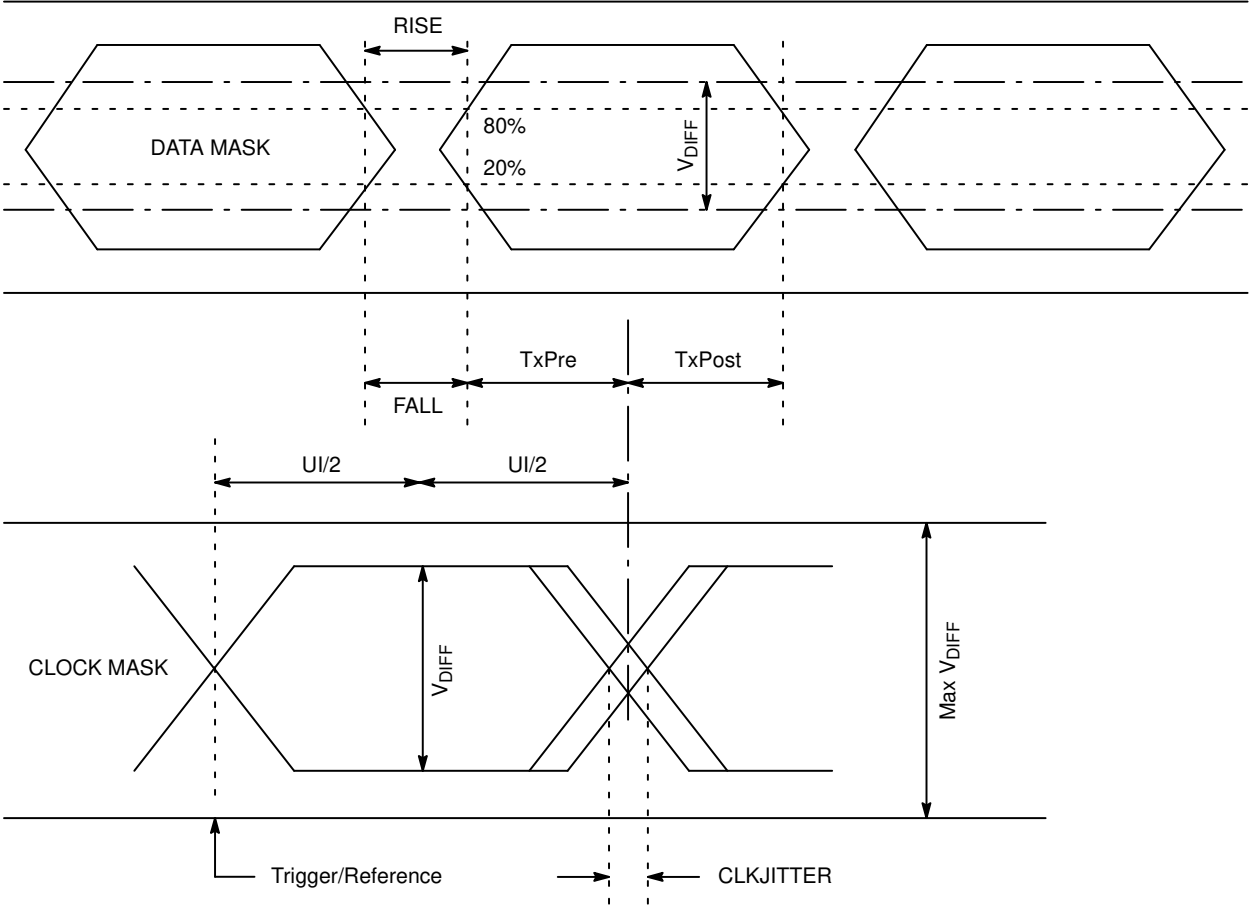


Figure 9. Eye Diagram for Clock and Data Signals

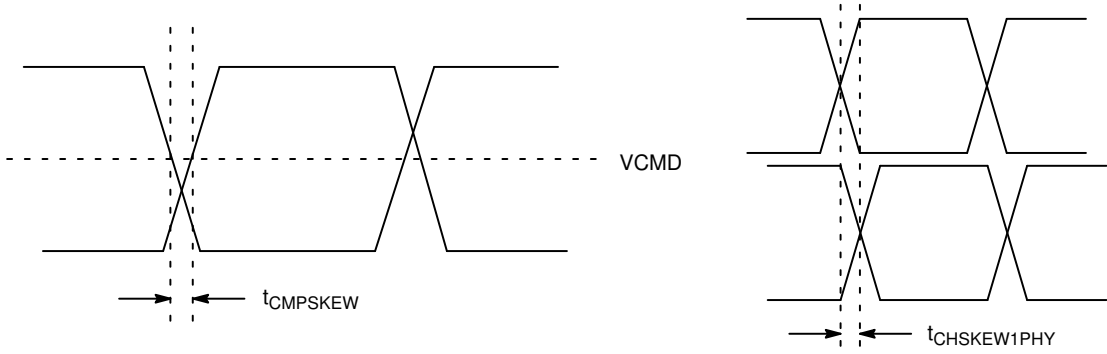


Figure 10. Skew within the PHY and Output Channels

POWER-ON RESET AND STANDBY TIMING

Power-Up Sequence

The recommended power-up sequence for the MT9M021/MT9M031 is shown in Figure 11. The available power supplies (V_{DD_IO} , V_{DD} , V_{DD_SLVS} , V_{DD_PLL} , V_{AA} , V_{AA_PIX}) must have the separation specified below.

1. Turn on V_{DD_PLL} power supply.
2. After 0–10 μ s, turn on V_{AA} and V_{AA_PIX} power supply.
3. After 0–10 μ s, turn on V_{DD_IO} power supply.
4. After the last power supply is stable, enable EXTCLK.

5. Assert RESET_BAR for at least 1 ms.
6. Wait 150000 EXTCLKs (for internal initialization into software standby).
7. Configure PLL, output, and image settings to desired values.
8. Wait 1 ms for the PLL to lock.
9. Set streaming mode ($R0x301a[2] = 1$).

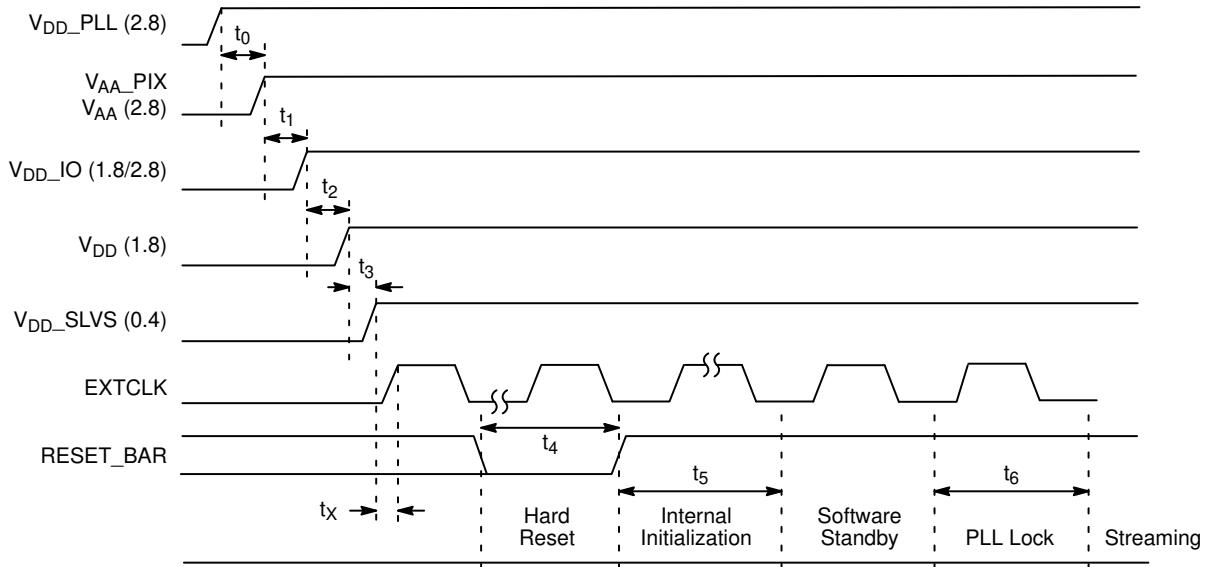


Figure 11. Power Up

Table 18. POWER-UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	V_{DD_PLL} to V_{AA}/V_{AA_PIX}	0	10	–	μ s
t_1	V_{AA}/V_{AA_PIX} to V_{DD_IO}	0	10	–	μ s
t_2	V_{DD_IO} to V_{DD}	0	10	–	μ s
t_3	V_{DD} to V_{DD_SLVS}	0	10	–	μ s
t_x	Xtal Settle Time	–	30 (Note 1)	–	ms
t_4	Hard Reset	1 (Note 2)	–	–	ms
t_5	Internal Initialization	150000	–	–	EXTCLKs
t_6	PLL Lock Time	1	–	–	ms

1. Xtal settling time is component-dependent, usually taking about 10–100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that V_{DD_PLL} is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V_{DD_PLL} is powered after other supplies then the sensor may have functionality issues and will experience high current draw on this supply.

Power-Down Sequence

The recommended power-down sequence for the MT9M021/MT9M031 is shown in Figure 12. The available power supplies (V_{DD_IO} , V_{DD} , V_{DD_SLVS} , V_{DD_PLL} , V_{AA} , V_{AA_PIX}) must have the separation specified below.

1. Disable streaming if output is active by setting standby $R0x301a[2] = 0$.
2. The soft standby is reached after the current row or frame, depending on configuration, has ended.
3. Turn off V_{DD_SLVS} .
4. Turn off V_{DD} .
5. Turn off V_{DD_IO} .
6. Turn off V_{AA}/V_{AA_PIX} .
7. Turn off V_{DD_PLL} .

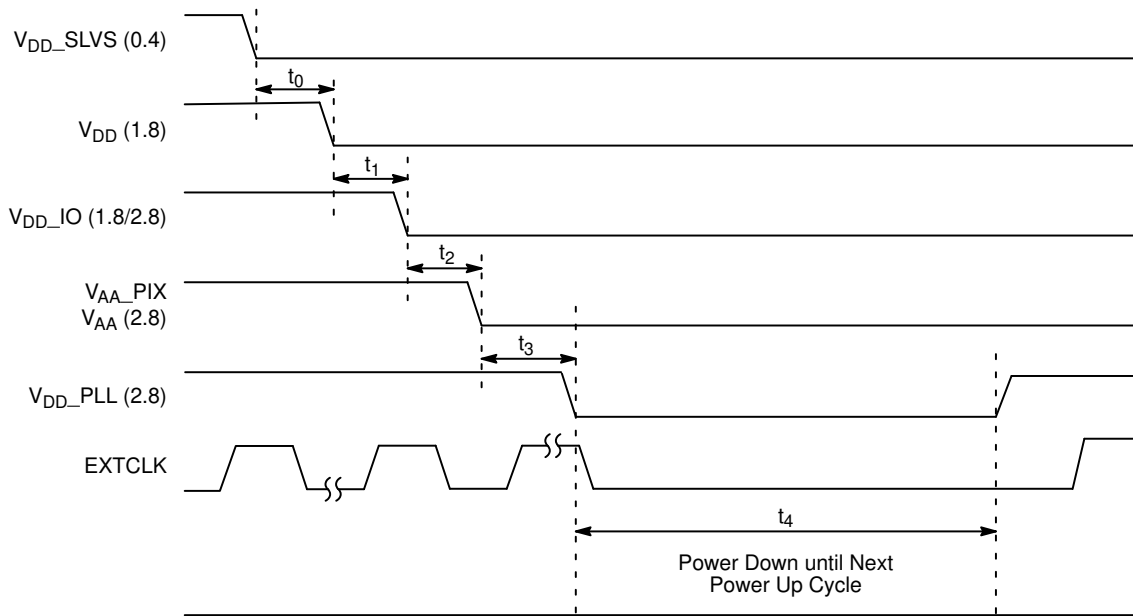


Figure 12. Power Down

Table 19. POWER-DOWN SEQUENCE

Symbol	Parameter	Min	Typ	Max	Unit
t_0	V_{DD_SLVS} to V_{DD}	0	–	–	μs
t_1	V_{DD} to V_{DD_IO}	0	–	–	μs
t_2	V_{DD_IO} to V_{AA}/V_{AA_PIX}	0	–	–	μs
t_3	V_{AA}/V_{AA_PIX} to V_{DD_PLL}	0	–	–	μs
t_4	PwrDn until Next PwrUp Time	100	–	–	ms

1. t_4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

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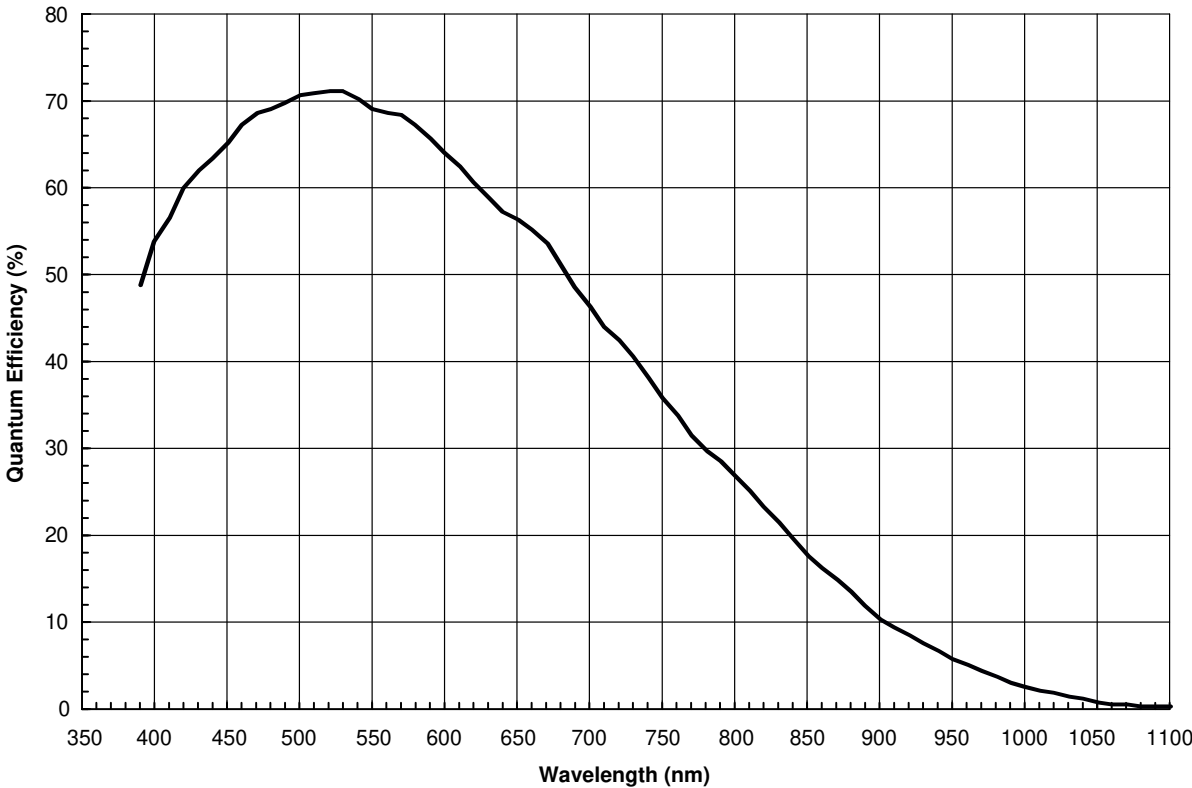


Figure 13. Quantum Efficiency – Monochrome Sensor

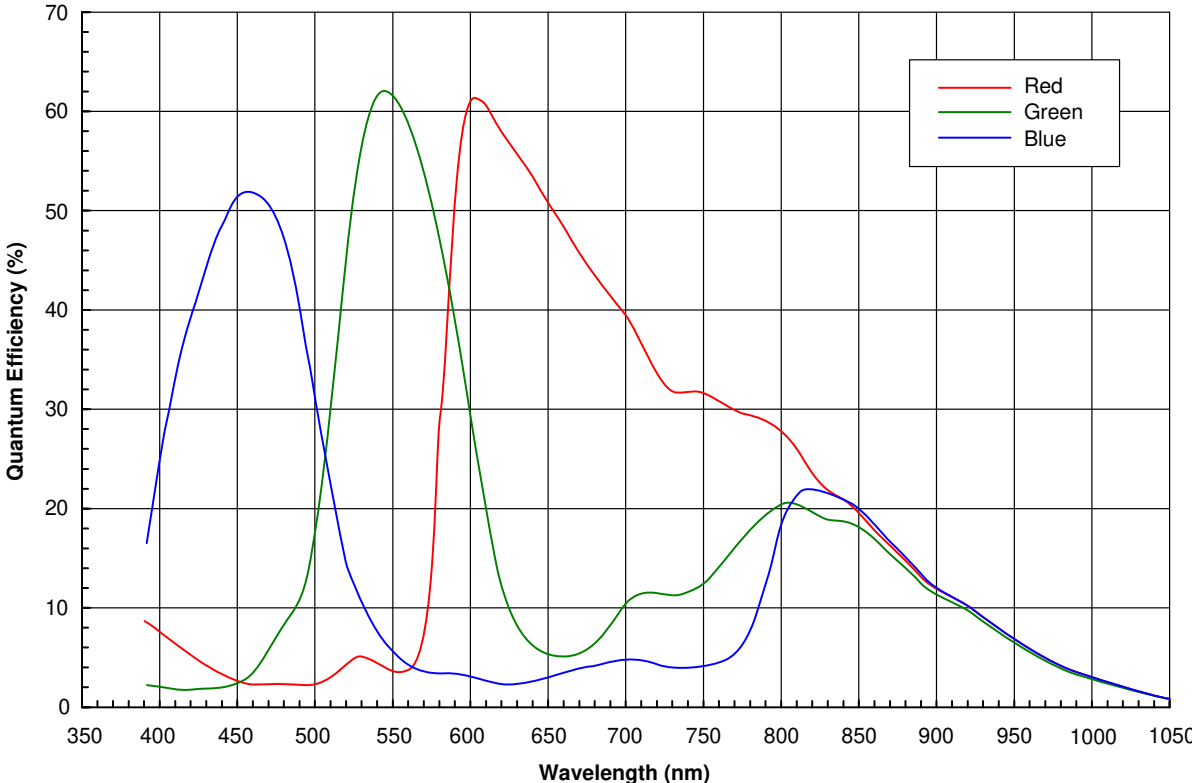
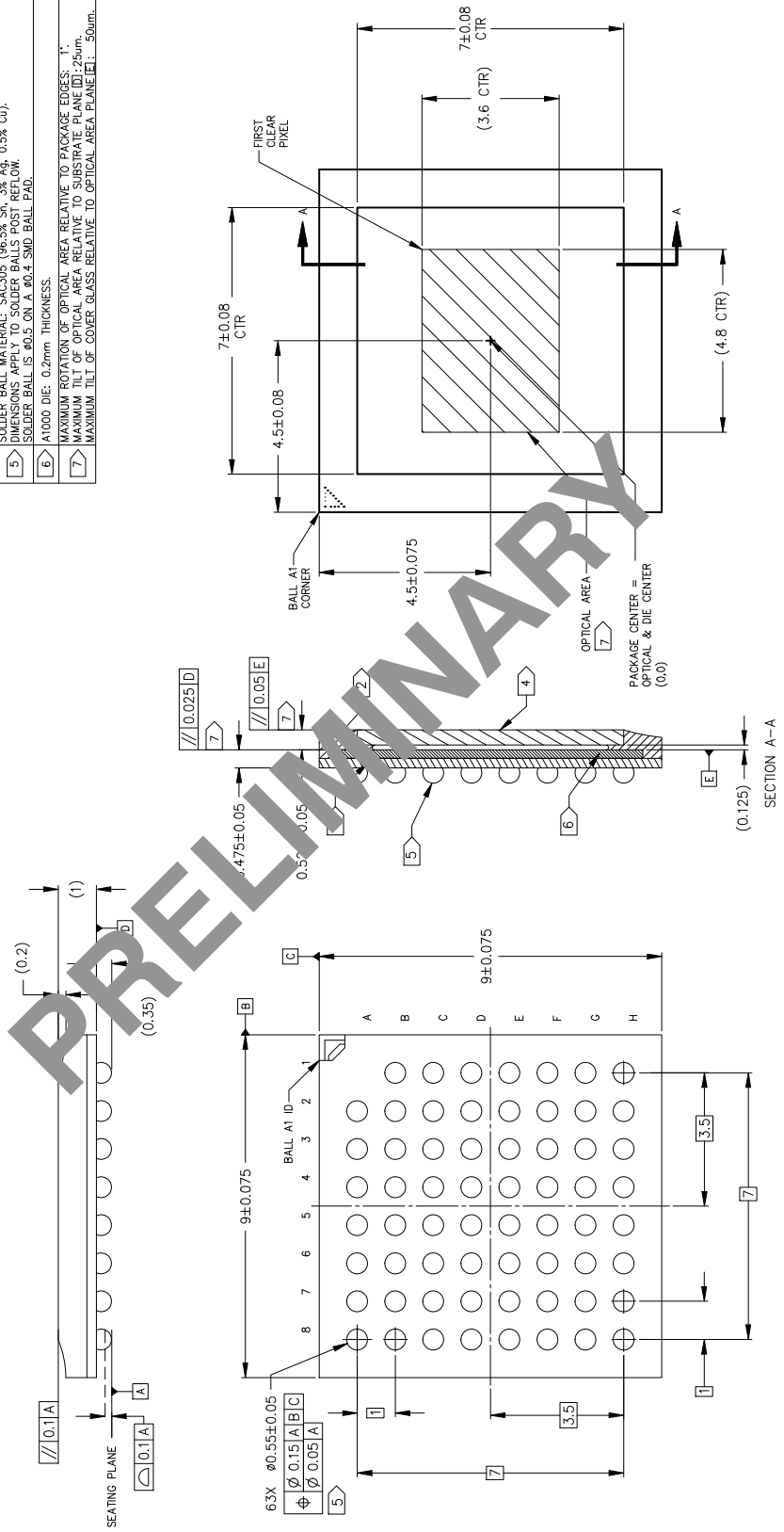


Figure 14. Quantum Efficiency – Color Sensor

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PACKAGE DIMENSIONS

NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN () ARE FOR REFERENCE ONLY.
2	ENCAPSULANT: EPOXY.
3	SUBSTRATE MATERIAL: PLASTIC LAMINATE 0.25 THICKNESS.
4	LID MATERIAL: BOROSILICATE GLASS 0.44±0.04 THICKNESS. REFRACTIVE INDEX AT 20°C = 1.5255 @ 546nm & 1.5231 @ 588nm.
5	SOLDER BALL MATERIAL: SAC305 (98.5% Sn, 3% Ag, 0.5% Cu). DIMENSIONS ARE TO THE CENTER OF THE BALL OR SOLDER BALL U.S. ON A 60.4 μm BALL PAD.
6	A1000 DIE: 0.2mm THICKNESS.
7	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE (D1): 25μm. MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE (E1): 50μm.



Note: All dimensions in millimeters.

Figure 15. 63-Ball iBGA Package Outline Drawing (Case 503AQ)

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PACKAGE DIMENSIONS

NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN () ARE FOR REFERENCE ONLY
2	ENCAPSULANT: EPOXY
3	SUBSTRATE MATERIAL: EPOXY LAMINATE 0.5 THICKNESS
4	LID MATERIAL: BOROSILICATE GLASS 0.4 THICKNESS. REFRACTIVE INDEX AT 20°C = 1.5255 @ 546nm & 1.5231 @ 595nm
5	LEAD FINISH: GOLD PLATING, 0.5 MICRONS MINIMUM THICKNESS
6	IMAGE SENSOR DIE 0.2 THICKNESS
7	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°
8	MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SEATING PLANE: LEAD: .25 MICRONS MAXIMUM TILT OF OPTICAL AREA RELATIVE TO TOP OF COVER GLASS(D): .50 MICRONS
9	OPTICAL CENTER = PACKAGE CENTER

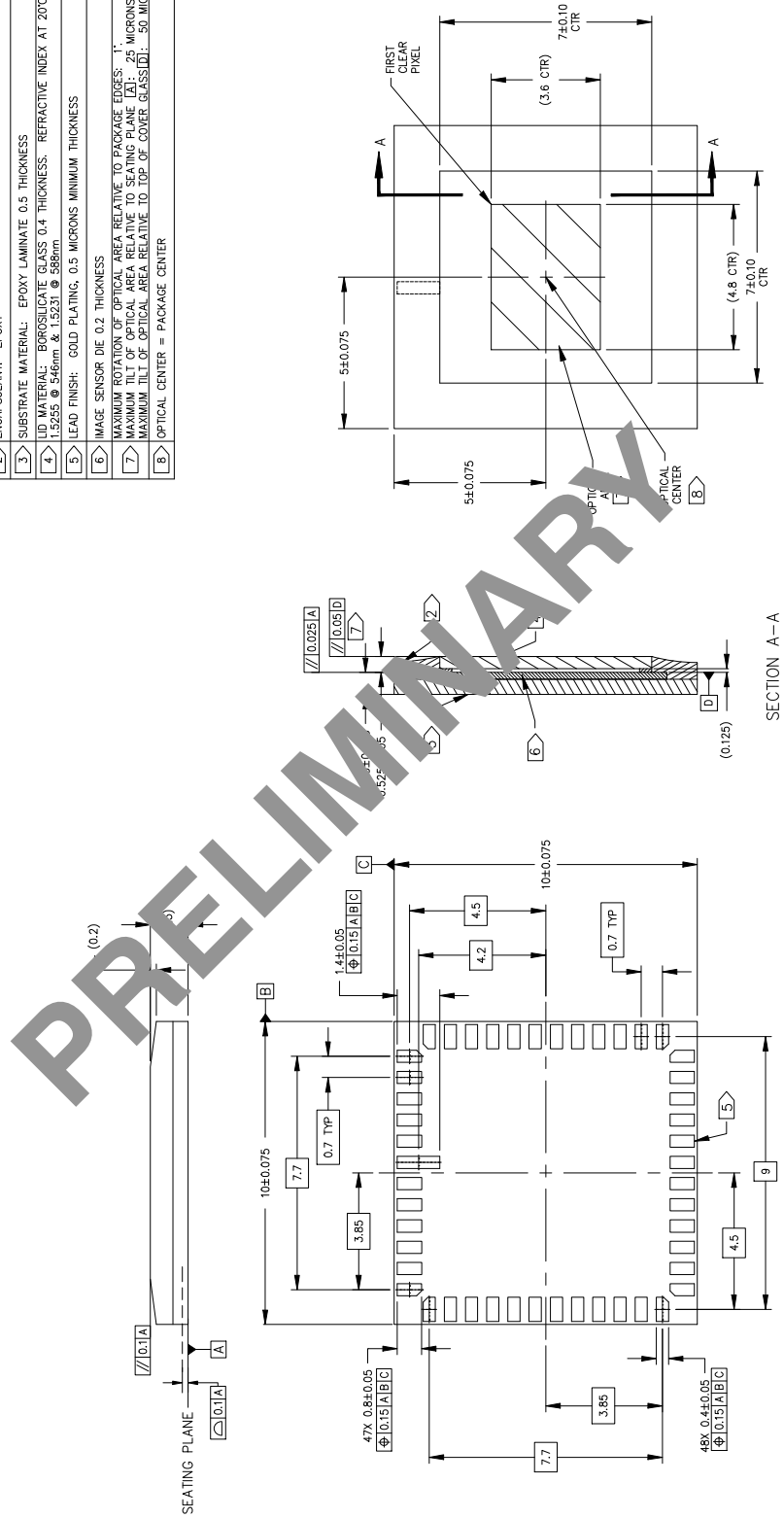



Figure 16. 48-Pin iLCC Package Outline Drawing (Case 847AJ)

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