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# MT9M131

# MT9M131 1/3-inch SOC 1.3 Mp CMOS Digital Image Sensor

**Table 1. KEY PERFORMANCE PARAMETERS**

| Parameter | Typical Value |
|---|---|
| Optical Format | 1/3-inch (5:4) |
| Active Imager Size | 4.6 mm (H) × 3.7 mm (V),<br>5.9 mm Diagonal |
| Active Pixels | 1280 (H) × 1024 (V) |
| Pixel Size | 3.6 × 3.6 μm |
| Color Filter Array | RGB Bayer Pattern |
| Shutter Type | Electronic Rolling Shutter (ERS) |
| Maximum Data Rate/Master Clock | 27 MPS/54 MHz |
| Frame Rate<br>SXGA (1280 × 1024)<br>VGA (640 × 480) | <br>15 fps at 54 MHz<br>30 fps at 54 MHz |
| Maximum Resolution at<br>60 fps/54 MHz Clock | 640 × 512 |
| ADC Resolution | 10-bit, Dual On-chip |
| Responsivity | 1.0 V/lux–sec (550 nm) |
| Dynamic Range | 71 dB |
| $SNR_{MAX}$ | 44 dB |
| Supply Voltage<br>I/O Digital<br>Core Digital<br>Analog | <br>1.8–3.1 V<br>2.5–3.1 V<br>2.5–3.1 V |
| Power Consumption | 170 mW SXGA at 15 fps<br>(54 MHz EXTCLK) |
| Operating Temperature | –30°C to +70°C |
| Packaging | 48-pin CLCC |

### Features

- System-on-a-Chip (SOC) – Completely Integrated Camera System
- Ultra-low Power, Cost Effective, Progressive Scan CMOS Image Sensor
- Superior Low-light Performance
- On-chip Image Flow Processor (IFP) Performs Sophisticated Processing:
  - Color Recovery and Correction
  - Sharpening, Gamma, Lens Shading Correction
  - On-the-Fly Defect Correction
- Electronic Pan, Tilt, and Zoom
- Automatic Features:
  - Auto Exposure (AE), Auto White Balance (AWB), Auto Black Reference (ABR), Auto Flicker Avoidance, Auto Color Saturation, Auto Defect Identification and Correction
  - Fully Automatic Xenon and LED-type Flash Support

**ON Semiconductor®**

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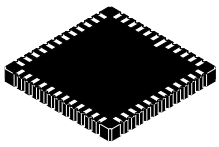


**CLCC48 11.43 x 11.43**
**CASE 848AV**

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

### Features (Continued)

- Fast Exposure Adaptation
- Multiple Parameter Contexts
- Easy and Fast Mode Switching
- Camera Control Sequencer Automates:
  - Snapshots
  - Snapshots with Flash
  - Video Clips
- Simple Two-wire Serial Programming Interface
- ITU–R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB Formats (Progressive Scan)
- Raw and Processed Bayer Formats
- Output FIFO and Integer Clock Divider:
  - Uniform Pixel Clocking

### Applications

- Security
- Biometrics
- Videoconferencing
- Toys

## ORDERING INFORMATION

**Table 2. AVAILABLE PART NUMBERS**

| Part Number | Product Description | Orderable Product Attribute Description |
|---|---|---|
| MT9M131C12STC−DP | 1.3 MP 1/3″ SOC | Dry Pack with Protective Film |
| MT9M131C12STC−DR | 1.3 MP 1/3″ SOC | Dry Pack without Protective Film |
| MT9M131C12STC−TP | 1.3 MP 1/3″ SOC | Tape & Reel with Protective Film |
| MT9M131C12STC−TR | 1.3 MP 1/3″ SOC | Tape & Reel without Protective Film |

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

## GENERAL DESCRIPTION

The MT9M131 is an SXGA-format single-chip camera with a 1/3-inch CMOS active-pixel digital image sensor. This device combines the MT9M011 image sensor core with fourth-generation digital image flow processor technology from ON Semiconductor. It captures high-quality color images at SXGA resolution.

The MT9M131 features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the demands of products such as security, biometrics, and videoconferencing cameras. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9M131 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure (AE), automatic 50 Hz/60 Hz flicker avoidance, lens shading correction (LC), auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both xenon and LED-type flash light sources in several snapshot modes.

The MT9M131 can be programmed to output progressive-scan images up to 30 frames per second (fps) in preview power-saving mode, and 15 fps in full-resolution (SXGA) mode. In either mode, the image data can be output in any one of six formats:

- ITU−R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FV and LV signals are output on dedicated signals, along with a pixel clock that is synchronous with valid data.

## FUNCTIONAL OVERVIEW

The MT9M131 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8- or 10-bit $D_{OUT}$ port, shown in Figure 1.

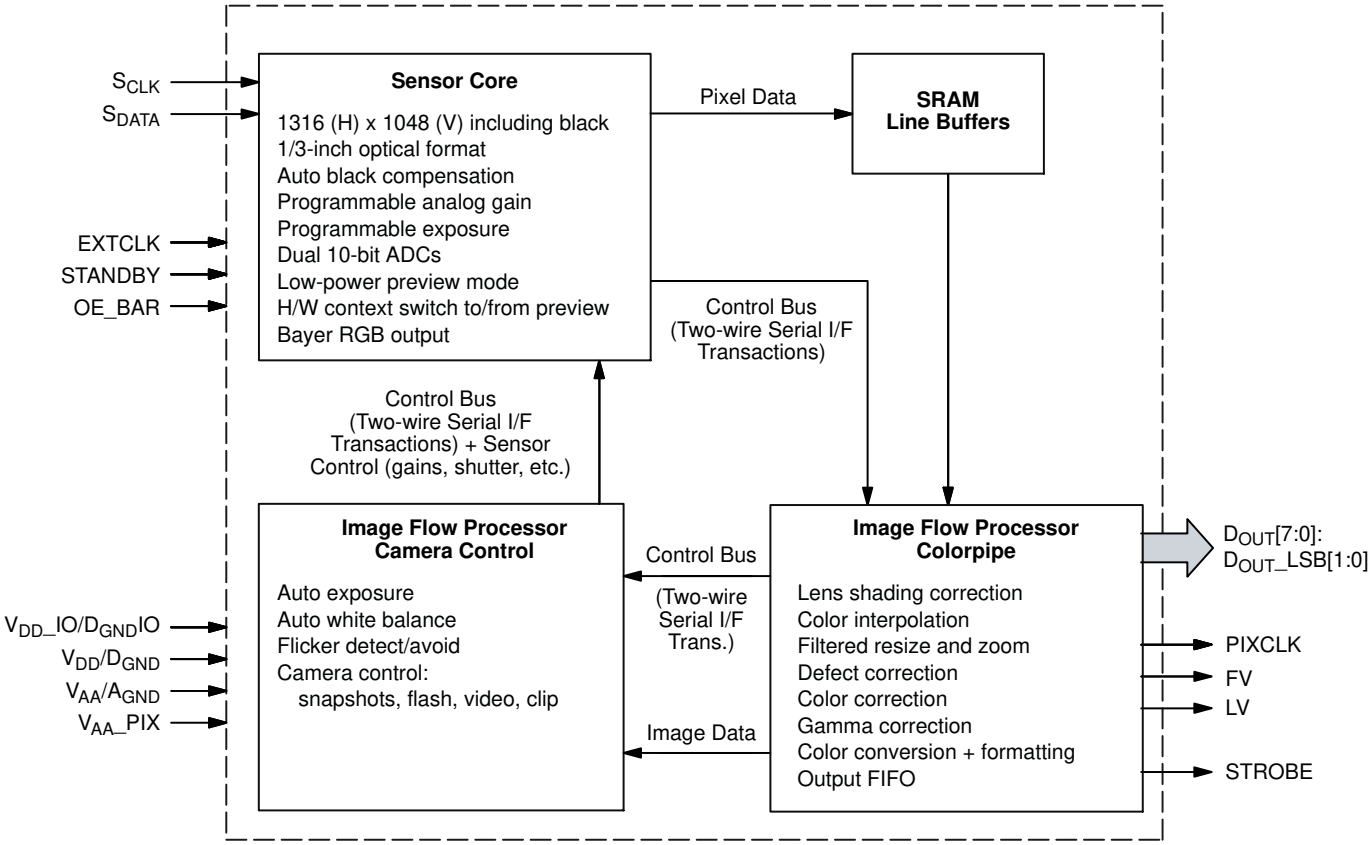



**Figure 1. Functional Block Diagram**

The output pixel clock is used to latch data, while FV and LV signals indicate the active video. The MT9M131 internal registers are configured using a two-wire serial interface.

The device can be put in low-power sleep mode by asserting STANDBY and shutting down the clock. Output pins can be tri-stated by de-asserting the OE_BAR. Both tri-stating output pins and entry in standby mode also can be achieved by two-wire serial interface register writes.

The MT9M131 accepts input clocks up to 54 MHz, delivering up to 15 fps for SXGA resolution images, and up to 30 fps for QSXGA (full field-of-view [FOV], sensor pixel skipping) images. The device also supports a low-power preview configuration that delivers SXGA images at 7.5 fps and QSXGA images at 30 fps. The device can be programmed to slow the frame rate in low light conditions to achieve longer exposures and better image quality.

### Internal Architecture

Internally, the MT9M131 consists of a sensor core and an IFP. The IFP is divided in two sections: the colorpipe (CP), and the camera controller (CC). The sensor core captures raw Bayer-encoded images that are then input in the IFP. The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance, and to support snapshot modes. The sensor core, CP, and CC registers are grouped in three separate address spaces, as shown in Figure 2.

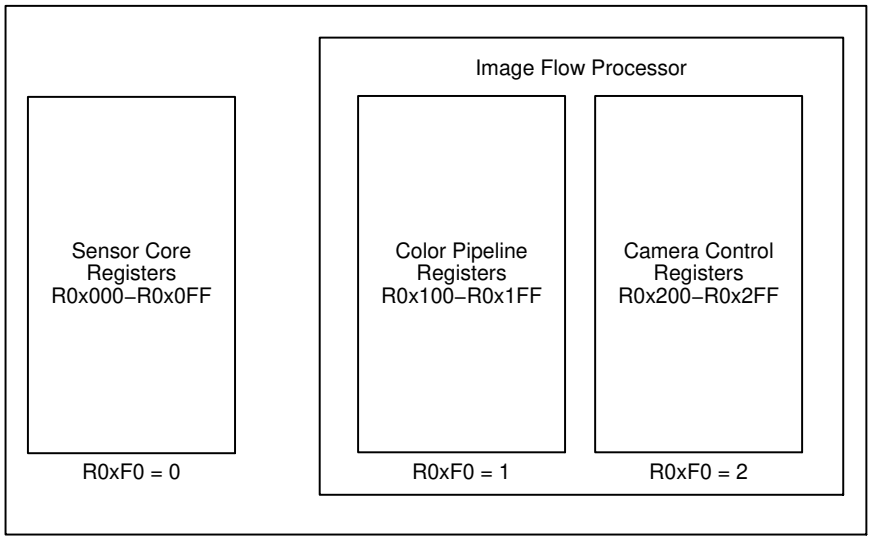



**Figure 2. Internal Registers Grouping**

NOTE: Internal registers are grouped in three address spaces. Register R0xF0 in each page selects the desired address space.

When accessing internal registers through the two-wire serial interface, select the desired address space by programming the R0xF0 shared register.

The MT9M131 accelerates mode switching with hardware-assisted context switching and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9M131 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

- Standard FV/LV video interface with gated pixel clocks
- Standard video interface with uniform clocking
- Progressive ITU−R BT.656 marker-embedded video interface with either gated or uniform pixel clocking

## REGISTER OPERATIONS

This data sheet refers to various registers that the user reads from or writes to for altering the MT9M131 operation. Hardware registers appear as follows and may be read from or written to by sending the address and data information over the two-wire serial interface.

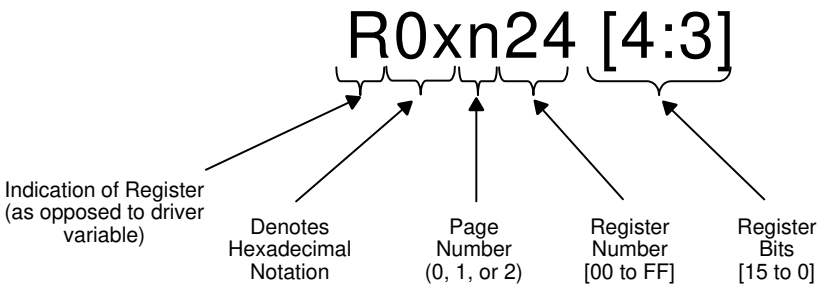



**Figure 3. Register Legend**

The MT9M131 was designed to facilitate customizations to optimize image quality processing. Multiple parameters are allowed to be adjusted at various stages of the image processing pipeline to tune the quality of the output image.

The MT9M131 contains three register pages: sensor, colorpipe, and camera control. The register page must be set prior to writing to a register in the page.

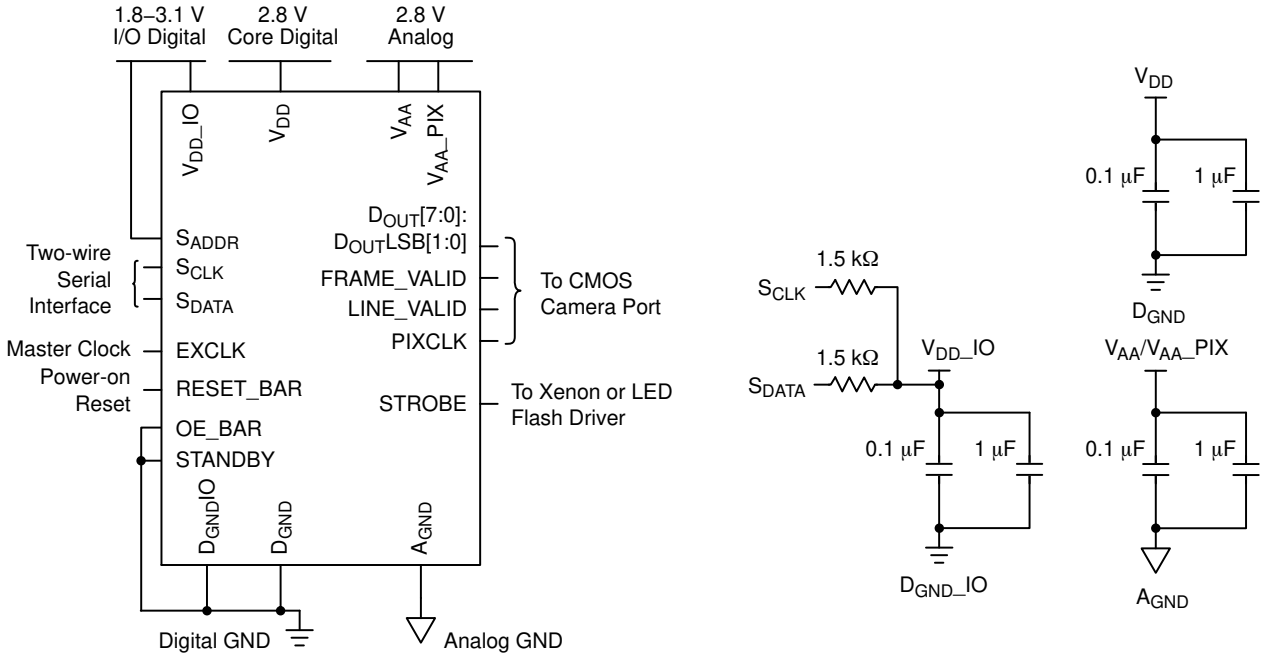
For example, to write to register R0x106 (register 6 in page 1):

- Write the value of “1” to the page map register (0xF0)
- Write the desired value to register R0x06

The sensor maintains the page number once set. The page map register is located at address 0xF0 for all three register pages.

## TYPICAL CONNECTION

Figure 4 shows typical MT9M131 device connections.




Notes:
1. For two-wire serial interface, ON Semiconductor recommends a 1.5 kΩ resistor; however, larger values may be used for slower two-wire speed.
2. $V_{DD}$, $V_{AA}$, $V_{AA}$_PIX must all be at the same potential, though if connected, care must be taken to avoid excessive noise injection in the $V_{AA}$/$V_{AA}$_PIX power domains.
3. Logic levels of all input pins, that is, $S_{ADDR}$, EXTCLK, $S_{CLK}$, $S_{DATA}$, OE_BAR, STANDBY, and RESET_BAR must be equal to $V_{DD}$_IO.

**Figure 4. Typical Configuration (Connection)**

For low-noise operation, the MT9M131 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using ceramic capacitors. The use of inductance filters is not recommended.

The MT9M131 also supports different digital core ($V_{DD}$/$D_{GND}$) and I/O power ($V_{DD}$_IO/$D_{GND}$IO) power domains that can be at different voltages.

### Pin/Ball Assignment

The MT9M131 is available in the CLCC package configuration. Figure 5 shows the 48-pin CLCC assignment.

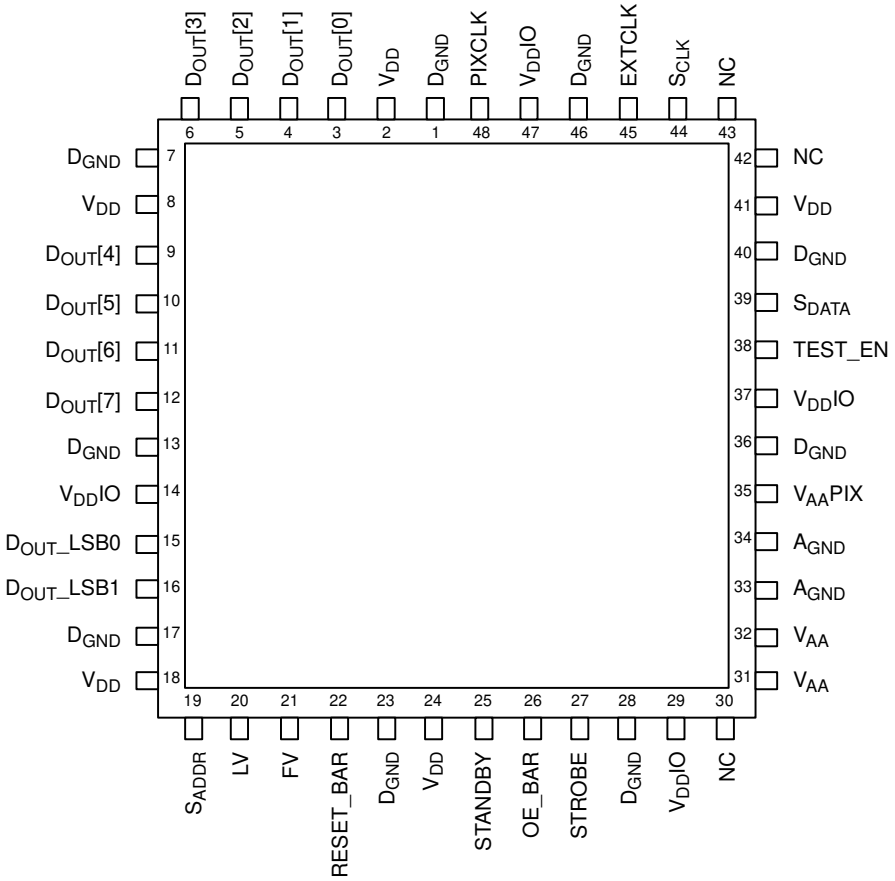



**Figure 5. 48-Pin CLCC Assignment**

**Table 3. PIN/BALL DESCRIPTIONS**

| Signal | Type | Default Operation | Description |
|---|---|---|---|
| EXTCLK | I/O | Input | Master clock in sensor |
| OE_BAR | I/O | Input | Active LOW: output enable for $D_{OUT}$[7:0] |
| RESET_BAR | I/O | Input | Active LOW: asynchronous reset |
| $S_{ADDR}$ | I/O | Input | Two-wire serial interface DeviceID selection 1:0xBA, 0:0x90 |
| $S_{CLK}$ | I/O | Input | Two-wire serial interface clock |
| STANDBY | I/O | Input | Active HIGH: disables imager |
| $S_{DATA}$ | I/O | Input | Two-wire serial interface data I/O |
| TEST_EN | I/O | Input | Tie to $D_{GND}$ for normal operation (manufacturing use only) |
| $D_{OUT}$0 | I/O | Output | |
| $D_{OUT}$1 | I/O | Output | |
| $D_{OUT}$2 | I/O | Output | |
| $D_{OUT}$3 | I/O | Output | |
| $D_{OUT}$4 | I/O | Output | |
| $D_{OUT}$5 | I/O | Output | |
| $D_{OUT}$6 | I/O | Output | |
| $D_{OUT}$70 | I/O | Output | |
| $D_{OUT}$_LSB0 | I/O | Output | Sensor bypass mode output 0 – typically left unconnected for normal SOC operation |
| $D_{OUT}$_LSB1 | I/O | Output | Sensor bypass mode output 1 – typically left unconnected for normal SOC operation |
| FRAME_VALID(FV) | I/O | Output | Active HIGH: FV; indicates active frame |
| LINE_VALID (LV) | I/O | Output | Active HIGH: LV, DATA_VALID; indicates active pixel |
| PIXCLK | I/O | Output | Pixel clock output |
| STROBE | I/O | Output | Active HIGH: strobe (Xenon) or turn on (LED) flash |
| $A_{GND}$ | Supply | | Analog ground |
| $D_{GND}$ | Supply | | Core digital ground |
| $D_{GND}$IO | Supply | | I/O digital ground |
| $V_{AA}$ | Supply | | Analog power (2.5–3.1 V) |
| $V_{AA}$PIX | Supply | | Pixel array analog power supply (2.5–3.1 V) |
| $V_{DD}$ | Supply | | Core digital power (2.5–3.1 V) |
| $V_{DD}$IO | Supply | | I/O digital power (1.8–3.1 V) |
| NC | – | | No connect |

1. All inputs and outputs are implemented with bidirectional buffers. Care must be taken to ensure that all inputs are driven and all outputs are driven if tri-stated.

## OUTPUT DATA ORDERING

**Table 4. DATA ORDERING IN YCbCr MODE**

| Mode | Byte | | | |
|---|---|---|---|---|
| Default | $Cb_i$ | $Y_i$ | $Cr_i$ | $Y_{i+1}$ |
| Swap CrCb | $Cr_i$ | $Y_i$ | $Cb_i$ | $Y_{i+1}$ |
| Swap YC | $Y_i$ | $Cb_i$ | $Y_{i+1}$ | $Cr_i$ |
| Swap CrCb, SwapYC | $Y_i$ | $Cr_i$ | $Y_{i+1}$ | $Cb_i$ |

**Table 5. OUTPUT DATA ORDERING IN PROCESSED BAYER MODE**

| Mode | Line | Byte | | | |
|---|---|---|---|---|---|
| Default | First | $G_i$ | $R_{i+1}$ | $G_{i+2}$ | $R_{i+3}$ |
| | Second | $B_i$ | $G_{i+1}$ | $B_{i+2}$ | $G_{i+3}$ |
| Flip Bayer Col | First | $R_i$ | $G_{i+1}$ | $R_{i+2}$ | $G_{i+3}$ |
| | Second | $G_i$ | $B_{i+1}$ | $G_{i+2}$ | $B_{i+3}$ |
| Flip Bayer Row | First | $B_i$ | $G_{i+1}$ | $B_{i+2}$ | $G_{i+3}$ |
| | Second | $G_i$ | $R_{i+1}$ | $G_{i+2}$ | $R_{i+3}$ |
| Flip Bayer Col, Flip Bayer Row | First | $G_i$ | $B_{i+1}$ | $G_{i+2}$ | $B_{i+3}$ |
| | Second | $R_i$ | $G_{i+1}$ | $R_{i+2}$ | $G_{i+3}$ |

**Table 6. OUTPUT DATA ORDERING IN RGB MODE**

| Mode (Swap Disabled) | Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 565RGB | First | R7 | R6 | R5 | R4 | R3 | G7 | G6 | G5 |
| | Second | G4 | G3 | G2 | B7 | B6 | B5 | B4 | B3 |
| 555RGB | First | 0 | R7 | R6 | R5 | R4 | R3 | G7 | G6 |
| | Second | G5 | G4 | G3 | B7 | B6 | B5 | B4 | B3 |
| 444xRGB | First | R7 | R6 | R5 | R4 | G7 | G6 | G5 | G4 |
| | Second | B7 | B6 | B5 | B4 | 0 | 0 | 0 | 0 |
| x444RGB | First | 0 | 0 | 0 | 0 | R7 | R6 | R5 | R4 |
| | Second | G7 | G6 | G5 | G4 | B7 | B6 | B5 | B4 |

**Table 7. OUTPUT DATA ORDERING IN (8+2) BYPASS MODE**

| Mode | Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 8 + 2 Bypass | First | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 |
| | Second | 0 | 0 | 0 | 0 | 0 | 0 | B1 | B0 |

## IFP REGISTER LIST

**Table 8. COLORPIPE REGISTERS (ADDRESS PAGE 1)**

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R5 (R0x105) | Aperture Correction | 0000 0000 0000 dddd | 3 (0003) | Interp |
| R6 (R0x106) | Operating Mode Control | dddd dddd 0ddd dddd | 28686 (700E) | Cfg |
| R8 (R0x108) | Output Format Control | 0000 0ddd dddd dddd | 128 (0080) | Cfg |
| R16 (R0x110) | Reserved | – | 61437 (EFFD) | – |
| R17 (R0x111) | Reserved | – | 64831 (FD3F) | – |
| R18 (R0x112) | Reserved | – | 16367 (3FEF) | – |
| R19 (R0x113) | Reserved | – | N/A | – |
| R20 (R0x114) | Reserved | – | N/A | – |
| R21 (R0x115) | Reserved | – | N/A | – |
| R27 (R0x11B) | Reserved | – | 0 (0000) | – |
| R28 (R0x11C) | Reserved | – | 0 (0000) | – |
| R29 (R0x11D) | Reserved | – | N/A | – |
| R30 (R0x11E) | Reserved | – | 512 (0200) | – |
| R37 (R0x125) | Color Saturation Control | 0000 0000 00dd dddd | 5 (0005) | rgb2yuv |
| R52 (R0x134) | Luma Offset | dddd dddd dddd dddd | 16 (0010) | CamInt |
| R53 (R0x135) | Luma Clip | dddd dddd dddd dddd | 61456 (F010) | CamInt |
| R58 (R0x13A) | Output Format Control 2 – Context A | 0ddd dddd dddd dddd | 512 (0200) | CamInt |
| R59 (R0x13B) | | | 1066 (042A) | LensCorr |
| R60 (R0x13C) | | | 1024 (0400) | LensCorr |
| R71 (R0x147) | | | 24 (0018) | |
| R72 (R0x148) | Test Pattern Generator Control | 0000 0000 d000 0ddd | 0 (0000) | FifoInt |
| R76 (R0x14C) | Defect Correction Context A | 0000 0000 0000 0ddd | 0 (0000) | DfctCorr |
| R77 (R0x14D) | Defect Correction Context B | 0000 0000 0000 0ddd | 0 (0000) | DfctCorr |
| R78 (R0x14E) | Reserved | – | 10 (000A) | – |
| R80 (R0x150) | | | N/A | |
| R82 (R0x152) | Reserved | – | 0 (0000) | – |
| R83 (R0x153) | | | 7700 (1E14) | GmaCorr |
| R84 (R0x154) | | | 17966 (462E) | GmaCorr |
| R85 (R0x155) | | | 34666 (876A) | GmaCorr |
| R86 (R0x156) | | | 47008 (B7A0) | GmaCorr |
| R87 (R0x157) | | | 57548 (E0CC) | GmaCorr |
| R88 (R0x158) | | | 0 (0000) | GmaCorr |
| R104 (R0x168) | Reserved | – | 17 (0011) | – |
| R128 (R0x180) | | | 7 (0007) | LensCorr |
| R129 (R0x181) | | | 56588 (DD0C) | LensCorr |
| R130 (R0x182) | | | 62696 (F4E8) | LensCorr |
| R131 (R0x183) | | | 1276 (04FC) | LensCorr |
| R132 (R0x184) | | | 57868 (E20C) | LensCorr |
| R133 (R0x185) | | | 63212 (F6EC) | LensCorr |
| R134 (R0x186) | | | 764 (02FC) | LensCorr |
| R135 (R0x187) | | | 56588 (DD0C) | LensCorr |
| R136 (R0x188) | | | 62696 (F4E8) | LensCorr |
| R137 (R0x189) | | | 250 (00FA) | LensCorr |

**Table 8. COLORPIPE REGISTERS (ADDRESS PAGE 1)** (continued)

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R138 (R0x18A) | | | 34866 (8832) | LensCorr |
| R139 (R0x18B) | | | 56754 (DDB2) | LensCorr |
| R140 (R0x18C) | | | 63466 (F7EA) | LensCorr |
| R141 (R0x18D) | | | 2 (0002) | LensCorr |
| R142 (R0x18E) | | | 47646 (BA1E) | LensCorr |
| R143 (R0x18F) | | | 60627 (ECD3) | LensCorr |
| R144 (R0x190) | | | 63473 (F7F1) | LensCorr |
| R145 (R0x191) | | | 255 (00FF) | LensCorr |
| R146 (R0x192) | | | 48926 (BF1E) | LensCorr |
| R147 (R0x193) | | | 61142 (EED6) | LensCorr |
| R148 (R0x194) | | | 63474 (F7F2) | LensCorr |
| R149 (R0x195) | | | 3 (0003) | LensCorr |
| R153 (R0x199) | Line Counter | ???? ???? ???? ???? | N/A | CamInt |
| R154 (R0x19A) | Frame Counter | ???? ???? ???? ???? | N/A | CamInt |
| R155 (R0x19B) | Output Format Control 2 – Context B | 0ddd dddd dddd dddd | 512 (0200) | CamInt |
| R157 (R0x19D) | Reserved | – | 9390 (24AE) | – |
| R158 (R0x19E) | Reserved | – | N/A | – |
| R159 (R0x19F) | Reducer Gorizontal Pan – Context B | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| R160 (R0x1A0) | Reducer Horizontal Zoom – Context B | 0000 0ddd dddd dddd | 1280 (0500) | Interp |
| R161 (R0x1A1) | Reducer Horizontal Size – Context B | 0000 0ddd dddd dddd | 1280 (0500) | Interp |
| R162 (R0x1A2) | Reducer Vertical Pan – Context B | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| R163 (R0x1A3) | Reducer Vertical Zoom – Context B | 0000 0ddd dddd dddd | 1024 (0400) | Interp |
| R164 (R0x1A4) | Reducer Vertical Size – Context B | 0000 0ddd dddd dddd | 1024 (0400) | Interp |
| R165 (R0x1A5) | Reducer Horizontal Pan – Context A | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| R166 (R0x1A6) | Reducer Horizontal Zoom – Context A | 0000 0ddd dddd dddd | 1280 (0500) | Interp |
| R167 (R0x1A7) | Reducer Horizontal Size – Context A | 0000 0ddd dddd dddd | 640 (0280) | Interp |
| R168 (R0x1A8) | Reducer Vertical Pan – Context A | 0d00 0ddd dddd dddd | 0 (0000) | Interp |
| R169 (R0x1A9) | Reducer Vertical Zoom – Context A | 0000 0ddd dddd dddd | 1024 (0400) | Interp |
| R170 (R0x1AA) | Reducer Vertical Size – Context A | 0000 0ddd dddd dddd | 512 (0200) | Interp |
| R171 (R0x1AB) | Reducer Current Zoom Horizontal | ???? 0??? ???? ???? | N/A | Interp |
| R172 (R0x1AC) | Reducer Current Zoom Vertical | ???? 0??? ???? ???? | N/A | Interp |
| R174 (R0x1AE) | Reducer Zoom Step Size | dddd dddd dddd dddd | 1284 (0504) | Interp |
| R175 (R0x1AF) | Reducer Zoom Control | 0000 00dd 0ddd dddd | 16 (0010) | Interp |
| R179 (R0x1B3) | Global Clock Control | 0000 0000 0000 00dd | 2 (0002) | ClockRst |
| R180 (R0x1B4) | | | 32 (0020) | |
| R181 (R0x1B5) | | | 257 (0101) | |
| R182 (R0x1B6) | | | 4363 (110B) | LensCorr |
| R183 (R0x1B7) | | | 15399 (3C27) | LensCorr |
| R184 (R0x1B8) | | | 4362 (110A) | LensCorr |
| R185 (R0x1B9) | | | 12834 (3222) | LensCorr |
| R186 (R0x1BA) | | | 5643 (160B) | LensCorr |
| R187 (R0x1BB) | | | 12836 (3224) | LensCorr |
| R188 (R0x1BC) | | | 9228 (240C) | LensCorr |
| R189 (R0x1BD) | | | 24124 (5E3C) | LensCorr |
| R190 (R0x1BE) | | | 127 (007F) | LensCorr |

**Table 8. COLORPIPE REGISTERS (ADDRESS PAGE 1)** (continued)

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R191 (R0x1BF) | | | 8200 (2008) | LensCorr |
| R192 (R0x1C0) | | | 20023 (4E37) | LensCorr |
| R193 (R0x1C1) | | | 100 (0064) | LensCorr |
| R194 (R0x1C2) | | | 8463 (210F) | LensCorr |
| R195 (R0x1C3) | | | 19250 (4B32) | LensCorr |
| R196 (R0x1C4) | | | 100 (0064) | LensCorr |
| R200 (R0x1C8) | Global Context Control | dddd dddd dddd dddd | 0 (0000) | CntxCtl |
| R201 (R0x1C9) | Reserved | – | N/A | – |
| R202 (R0x1CA) | Reserved | – | N/A | – |
| R203 (R0x1CB) | Reserved | – | N/A | – |
| R204 (R0x1CC) | Reserved | – | N/A | – |
| R205 (R0x1CD) | Reserved | – | N/A | – |
| R206 (R0x1CE) | Reserved | – | N/A | – |
| R207 (R0x1CF) | Reserved | – | N/A | – |
| R208 (R0x1D0) | Reserved | – | N/A | – |
| R220 (R0x1DC) | | | 7700 (1E14) | GmaCorr |
| R221 (R0x1DD) | | | 17966 (462E) | GmaCorr |
| R222 (R0x1DE) | | | 34666 (876A) | GmaCorr |
| R223 (R0x1DF) | | | 47008 (B7A0) | GmaCorr |
| R224 (R0x1E0) | | | 57548 (E0CC) | GmaCorr |
| R225 (R0x1E1) | | | 0 (0000) | GmaCorr |
| R226 (R0x1E2) | Effects Mode | dddd dddd 0000 0ddd | 28672 (7000) | GmaCorr |
| R227 (R0x1E3) | Effects Sepia | dddd dddd dddd dddd | 45091 (B023) | GmaCorr |
| R240 (R0x1F0) | Page Map | 0000 0000 0000 0ddd | 0 (0000) | Cfg |
| R241 (R0x1F1) | Byte-wise Address | – | Reserved | – |

**Table 9. CAMERA CONTROL REGISTERS (ADDRESS PAGE 2)**

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R2 (R0x202) | | | 110 (006E) | ColorCorr |
| R3 (R0x203) | | | 10531 (2923) | ColorCorr |
| R4 (R0x204) | | | 1316 (0524) | ColorCorr |
| R9 (R0x209) | | | 146 (0092) | ColorCorr |
| R10 (R0x20A) | | | 22 (0016) | ColorCorr |
| R11 (R0x20B) | | | 8 (0008) | ColorCorr |
| R12 (R0x20C) | | | 171 (00AB) | ColorCorr |
| R13 (R0x20D) | | | 147 (0093) | ColorCorr |
| R14 (R0x20E) | | | 88 (0058) | ColorCorr |
| R15 (R0x20F) | | | 77 (004D) | ColorCorr |
| R16 (R0x210) | | | 169 (00A9) | ColorCorr |
| R17 (R0x211) | | | 160 (00A0) | ColorCorr |
| R18 (R0x212) | | | N/A | ColorCorr |
| R19 (R0x213) | | | N/A | ColorCorr |
| R20 (R0x214) | | | N/A | ColorCorr |
| R21 (R0x215) | | | 373 (0175) | ColorCorr |
| R22 (R0x216) | | | 22 (0016) | ColorCorr |
| R23 (R0x217) | | | 67 (0043) | ColorCorr |
| R24 (R0x218) | | | 12 (000C) | ColorCorr |
| R25 (R0x219) | | | 0 (0000) | ColorCorr |
| R26 (R0x21A) | | | 21 (0015) | ColorCorr |
| R27 (R0x21B) | | | 31 (001F) | ColorCorr |
| R28 (R0x21C) | | | 22 (0016) | ColorCorr |
| R29 (R0x21D) | | | 152 (0098) | ColorCorr |
| R30 (R0x21E) | | | 76 (004C) | ColorCorr |
| R31 (R0x21F) | | | 160 (00A0) | AWB |
| R32 (R0x220) | | | 51220 (C814) | AWB |
| R33 (R0x221) | | | 32896 (8080) | AWB |
| R34 (R0x222) | | | 55648 (D960) | AWB |
| R35 (R0x223) | | | 55648 (D960) | AWB |
| R36 (R0x224) | | | 32512 (7F00) | AWB |
| R38 (R0x226) | Auto Exposure Window Horizontal Boundaries | dddd dddd dddd dddd | 32768 (8000) | AutoExp |
| R39 (R0x227) | Auto Exposure Window Vertical Boundaries | dddd dddd dddd dddd | 32776 (8008) | AutoExp |
| R40 (R0x228) | | | 61188 (EF04) | AWB |
| R41 (R0x229) | | | 36211 (8D73) | AWB |
| R42 (R0x22A) | | | 208 (00D0) | AWB |
| R43 (R0x22B) | Auto Exposure Center Horizontal Window Boundaries | dddd dddd dddd dddd | 24608 (6020) | AutoExp |
| R44 (R0x22C) | Auto Exposure Center Vertical Window Boundaries | dddd dddd dddd dddd | 24608 (6020) | AutoExp |
| R45 (R0x22D) | AWB Window Boundaries | dddd dddd dddd dddd | 61600 (F0A0) | AWB |
| R46 (R0x22E) | Auto Exposure Target and Precision Control | dddd dddd dddd dddd | 3146 (0C4A) | AutoExp |

**Table 9. CAMERA CONTROL REGISTERS (ADDRESS PAGE 2)** (continued)

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R47 (R0x22F) | Auto Exposure Speed and Sensitivity Control – Context A | dddd dddd dddd dddd | 57120 (DF20) | AutoExp |
| R48 (R0x230) | | | N/A | AWB |
| R49 (R0x231) | | | N/A | AWB |
| R50 (R0x232) | | | N/A | AWB |
| R51 (R0x233) | | | 5230 (146E) | AutoExp |
| R54 (R0x236) | | | 30736 (7810) | AutoExp |
| R55 (R0x237) | | | 768 (0300) | AutoExp |
| R56 (R0x238) | | | 1088 (0440) | AutoExp |
| R57 (R0x239) | | | 1676 (068C) | AutoExp |
| R58 (R0x23A) | | | 1676 (068C) | AutoExp |
| R59 (R0x23B) | | | 1676 (068C) | AutoExp |
| R60 (R0x23C) | | | 1676 (068C) | AutoExp |
| R61 (R0x23D) | | | 6105 (17D9) | AutoExp |
| R62 (R0x23E) | | | 7423 (1CFF) | AWB |
| R63 (R0x23F) | | | N/A | AutoExp |
| R70 (R0x246) | | | 55552 (D900) | AutoExp |
| R75 (R0x24B) | Reserved | – | 0 (0000) | – |
| R76 (R0x24C) | | | N/A | AutoExp |
| R77 (R0x24D) | | | N/A | AutoExp |
| R79 (R0x24F) | Reserved | – | N/A | – |
| R87 (R0x257) | | | 537 (0219) | AutoExp |
| R88 (R0x258) | | | 644 (0284) | AutoExp |
| R89 (R0x259) | | | 537 (0219) | AutoExp |
| R90 (R0x25A) | | | 644 (0284) | AutoExp |
| R91 (R0x25B) | Flicker Control 0 | ?000 0000 0000 0ddd | 2 (0002) | FD |
| R92 (R0x25C) | | | 4620 (120C) | |
| R93 (R0x25D) | | | 5394 (1512) | |
| R94 (R0x25E) | | | 26684 (683C) | ColorCorr |
| R95 (R0x25F) | | | 12296 (3008) | ColorCorr |
| R96 (R0x260) | | | 2 (0002) | ColorCorr |
| R97 (R0x261) | | | 32896 (8080) | |
| R98 (R0x262) | Auto Exposure Digital Gains Monitor | ???? ???? ???? ???? | N/A | AutoExp |
| R99 (R0x263) | Reserved | – | N/A | – |
| R100 (R0x264) | Reserved | – | 23036 (59FC) | – |
| R101 (R0x265) | | | 0 (0000) | AutoExp |
| R103 (R0x267) | Auto Exposure Digital Gain Limits | dddd dddd dddd dddd | 16400 (4010) | AutoExp |
| R104 (R0x268) | Reserved | – | 17 (0011) | – |
| R106 (R0x26A) | Reserved | – | N/A | – |
| R107 (R0x26B) | Reserved | – | N/A | – |
| R108 (R0x26C) | Reserved | – | N/A | – |
| R109 (R0x26D) | Reserved | – | N/A | – |
| R110 (R0x26E) | Reserved | – | N/A | – |
| R111 (R0x26F) | Reserved | – | N/A | – |
| R112 (R0x270) | Reserved | – | N/A | – |

**Table 9. CAMERA CONTROL REGISTERS (ADDRESS PAGE 2)** (continued)

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R113 (R0x271) | Reserved | – | N/A | – |
| R114 (R0x272) | Reserved | – | N/A | – |
| R115 (R0x273) | Reserved | – | N/A | – |
| R116 (R0x274) | Reserved | – | N/A | – |
| R117 (R0x275) | Reserved | – | N/A | – |
| R118 (R0x276) | Reserved | – | N/A | – |
| R119 (R0x277) | Reserved | – | N/A | – |
| R120 (R0x278) | Reserved | – | N/A | – |
| R121 (R0x279) | Reserved | – | N/A | – |
| R122 (R0x27A) | Reserved | – | N/A | – |
| R123 (R0x27B) | Reserved | – | N/A | – |
| R124 (R0x27C) | Reserved | – | N/A | – |
| R125 (R0x27D) | Reserved | – | N/A | – |
| R130 (R0x282) | | | 1020 (03FC) | AutoExp |
| R131 (R0x283) | | | 769 (0301) | AutoExp |
| R132 (R0x284) | | | 193 (00C1) | AutoExp |
| R133 (R0x285) | | | 929 (03A1) | AutoExp |
| R134 (R0x286) | | | 980 (03D4) | AutoExp |
| R135 (R0x287) | | | 983 (03D7) | AutoExp |
| R136 (R0x288) | | | 921 (0399) | AutoExp |
| R137 (R0x289) | | | 1016 (03F8) | AutoExp |
| R138 (R0x28A) | | | 28 (001C) | AutoExp |
| R139 (R0x28B) | | | 957 (03BD) | AutoExp |
| R140 (R0x28C) | | | 987 (03DB) | AutoExp |
| R141 (R0x28D) | | | 957 (03BD) | AutoExp |
| R142 (R0x28E) | | | 1020 (03FC) | AutoExp |
| R143 (R0x28F) | | | 990 (03DE) | AutoExp |
| R144 (R0x290) | | | 990 (03DE) | AutoExp |
| R145 (R0x291) | | | 990 (03DE) | AutoExp |
| R146 (R0x292) | | | 990 (03DE) | AutoExp |
| R147 (R0x293) | | | 31 (001F) | AutoExp |
| R148 (R0x294) | | | 65 (0041) | AutoExp |
| R149 (R0x295) | | | 867 (0363) | AutoExp |
| R150 (R0x296) | Reserved | – | 0 (0000) | – |
| R151 (R0x297) | Reserved | – | N/A | – |
| R152 (R0x298) | Reserved | – | 255 (00FF) | – |
| R153 (R0x299) | Reserved | – | 1 (0001) | – |
| R156 (R0x29C) | Auto Exposure Speed and Sensitivity Control – Context B | dddd dddd dddd dddd | 57120 (DF20) | AutoExp |
| R180 (R0x2B4) | Reserved | – | 32 (0020) | – |
| R181 (R0x2B5) | Reserved | – | N/A | – |
| R198 (R0x2C6) | Reserved | – | 0 (0000) | – |
| R199 (R0x2C7) | Reserved | – | N/A | – |
| R200 (R0x2C8) | Global Context Control | dddd dddd dddd dddd | 0 (0000) | CntxCtl |
| R201 (R0x2C9) | | | N/A | CamCtl |

**Table 9. CAMERA CONTROL REGISTERS (ADDRESS PAGE 2)** (continued)

| Register Number Dec (Hex) | Register Name | Data Format (Binary) | Default Value Dec (Hex) | Module |
|---|---|---|---|---|
| R202 (R0x2CA) | | | N/A | CamCtl |
| R203 (R0x2CB) | | | 0 (0000) | CamCtl |
| R204 (R0x2CC) | | | 0 (0000) | CamCtl |
| R205 (R0x2CD) | | | 8608 (21A0) | CamCtl |
| R206 (R0x2CE) | | | 7835 (1E9B) | CamCtl |
| R207 (R0x2CF) | | | 19018 (4A4A) | CamCtl |
| R208 (R0x2D0) | | | 5773 (168D) | CamCtl |
| R209 (R0x2D1) | | | 77 (004D) | CamCtl |
| R210 (R0x2D2) | | | 0 (0000) | CamCtl |
| R211 (R0x2D3) | | | 0 (0000) | CntxCtl |
| R212 (R0x2D4) | | | 520 (0208) | CamCtl |
| R213 (R0x2D5) | | | 0 (0000) | CamCtl |
| R239 (R0x2EF) | | | 8 (0008) | AWB |
| R240 (R0x2F0) | Page Map | 0000 0000 0000 0ddd | 0 (0000) | Cfg |
| R241 (R0x2F1) | Byte-wise Address | – | Reserved | – |
| R242 (R0x2F2) | | | 0 (0000) | AWB |
| R243 (R0x2F3) | Reserved | – | 0 (0000) | – |
| R244 (R0x2F4) | | | 110 (006E) | ColorCorr |
| R245 (R0x2F5) | | | 135 (0087) | ColorCorr |
| R246 (R0x2F6) | | | 54 (0036) | ColorCorr |
| R247 (R0x2F7) | | | 13 (000D) | ColorCorr |
| R248 (R0x2F8) | | | 171 (00AB) | ColorCorr |
| R249 (R0x2F9) | | | 136 (0088) | ColorCorr |
| R250 (R0x2FA) | | | 72 (0048) | ColorCorr |
| R251 (R0x2FB) | | | 87 (0057) | ColorCorr |
| R252 (R0x2FC) | | | 94 (005E) | ColorCorr |
| R253 (R0x2FD) | | | 122 (007A) | ColorCorr |
| R254 (R0x2FE) | | | 20543 (503F) | ColorCorr |
| R255 (R0x2FF) | | | 43136 (A880) | ColorCorr |

NOTE: Data Format Key:
0 = “Don’t Care” bit. The exceptions: R0x200 and R0x2FF, which are hardwired
R/O binary values
d = R/W bit
? = R/O bit

## IFP REGISTER DESCRIPTION

### Configuration

The vast majority of IFP registers associate naturally to one of the IFP modules. These modules are identified in Table 9. Detailed register descriptions follow in Table 10. A few registers create effects across a number of module functions. These include R0xF0 page map register (R/W); R0x106 operating mode control register (R/W); R0x108 output format control register (R/W); the R0x23E gain types and CCM threshold register – the gain threshold for CCM adjustment (R/W).

### Colorpipe Registers

Unless noted otherwise in this document, colorpipe registers take effect immediately. This can result in one or more distorted output frames. These registers should be adjusted during FV LOW or the resulting image should be hidden for one or two frames.

Colorpipe resize registers are updated shortly after FV goes HIGH. They are not examined again until the next frame.

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1**

| Register Number Dec – Hex | Description |
|---|---|
| **R5:1 – R0x105 – Aperture Correction** | |
| Default | 0x0003 |
| Description | Aperture correction scale factor, used for sharpening |
| Bit 3 | Enables automatic sharpness reduction control (see R0x233) |
| Bits 2:0 | Sharpening factor:<br>“000” – No sharpening<br>“001” – 25% sharpening<br>“010” – 50% sharpening<br>“011” – 75% sharpening<br>“100” – 100% sharpening<br>“101” – 125% sharpening<br>“110” – 150% sharpening<br>“111” – 200% sharpening |
| **R6:1 – R0x106 – Operating Mode Control (R/W)** | |
| Default | 0x700E |
| Description | This register specifies the operating mode of the IFP |
| Bit 15 | Enables manual white balance. User can set the base matrix and color channel gains. This bit must be asserted and de-asserted with a frame in between to force new color correction settings to take effect |
| Bit 14 | Enables auto exposure |
| Bit 13 | Enables on-the-fly defect correction |
| Bit 12 | Clips aperture corrections. Small aperture corrections (< 8) are attenuated to reduce noise amplification |
| Bit 11 | Load color correction matrix<br>1: In manual white balance mode, triggers the loading of a new base matrix in color correction and the loading of new base sensor gain ratios<br>0: Enables the matrix to be changed “offline” |
| Bit 10 | Enables lens shading correction<br>1: Enables lens shading correction |
| Bit 9 | Reserved |
| Bit 8 | Reserved |
| Bit 7 | Enables flicker detection<br>1: Enables automatic flicker detection |
| Bit 6 | Reserved for future expansion |
| Bit 5 | Reserved |
| Bit 4 | Bypasses color correction matrix<br>1: Outputs raw color, bypassing color correction<br>0: Normal color processing |
| Bits 3:2 | Auto exposure back light compensation control<br>“00” – Auto exposure sampling window is specified by R0x226 and R0x227 (“large window”)<br>“01” – Auto exposure sampling window is specified by R0x22B and R0x22C (“small window”)<br>“1X” – Auto exposure sampling window is specified by the weighted sum of the large window and the small window, with the small window weighted four times more heavily |

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| Bit 1 | Enables AWB<br>1: Enables auto white balance<br>0: Freezes white balance at current values |
| Bit 0 | Reserved for future expansion. |
| **R8:1 – R0x108 – Output Format Control (R/W)** | |
| Default | 0x0080 |
| Description | This register specifies the output timing and format in conjunction with R0x13A or R0x19B (depending on the context) |
| Bits 15:10 | Reserved for future expansion |
| Bit 9 | Flip Bayer columns in processed Bayer output mode<br>0: Column order is green, red and blue, green.<br>1: Column order is red, green and green, blue. |
| Bit 8 | Flip Bayer row in processed Bayer output mode<br>0: First row contains green and red; the second row contains blue and green<br>1: First row contains blue and green; the second row contains green and red |
| Bit 7 | Controls the values used for the protection bits in Rec. ITU−R BT.656 codes<br>0: Use zeros for the protection bits<br>1: Use the correct values |
| Bit 5 | Multiplexes Y (in YCbCr mode) or green (in RGB mode) channel on all channels (monochrome)<br>1: Forces Y/G onto all channels |
| Bit 4 | Disables Cab color output channel (Cb = 128) in YCbCr mode and disables the blue color output channel (B = 0) in RGB mode<br>1: Forces Cab to 128 or B to 0 |
| Bit 3 | Disables Y color output channel (Y = 128) in YCbCr and disables the green color output channel (G = 0) in RGB mode<br>1: Forces Y to 128 or G to 0 |
| Bit 2 | Disables Cr color output channel (Cr = 128) in YCbCr mode and disables the red color output channel (R = 0) in RGB mode<br>1: Forces Cr to 128 or R to 0 |
| Bit 1 | Toggles the assumptions about Bayer vertical CFA shift<br>0: Row containing red comes first<br>1: Row containing blue comes first |
| Bit 0 | Toggles the assumptions about Bayer horizontal CFA shift<br>0: Green comes first<br>1: Red or blue comes first |
| **R37:1 – R0x125 – Color Saturation Control (R/W)** | |
| Default | 0x0005 |
| Description | This register specifies the color saturation control settings. |
| Bit 5:3 | Specify overall attenuation of the color saturation<br>“000” – Full color saturation<br>“001” – 75% of full saturation<br>“010” – 50% of full saturation<br>“011” – 37.5% of full saturation<br>“100” – 25% of full saturation<br>“101” – 150% of full saturation<br>“110” – black and white |
| Bit 2:0 | Specify color saturation attenuation at high luminance (linearly increasing attenuation from no attenuation to monochrome at luminance of 224).<br>“000” – No attenuation<br>“001” – Attenuation starts at luminance of 216<br>“010” – Attenuation starts at luminance of 208<br>“011” – Attenuation starts at luminance of 192<br>“100” – Attenuation starts at luminance of 160<br>“101” – Attenuation starts at luminance of 96 |

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| **R52:1 – R0x134 – Luma Offset (R/W)** | |
| Default | 0x0010 |
| Description | Offset added to the luminance prior to output |
| Bits 15:8 | Y Offset in YCbCr mode |
| Bits 7:0 | Offset in RGB mode |
| **R53:1 – R0x135 – Luma Clip (R/W)** | |
| Default | 0xF010 |
| Description | Clipping limits for output luminance |
| Bits 15:8 | Highest value of output luminance |
| Bits 7:0 | Lowest value of output luminance |
| **R58:1 – R0x13A – Output Format Control 2 – Context A (R/W)** | |
| Default | 0x0200 |
| Description | Output format control 2A |
| Bit 14 | Output processed Bayer data |
| Bit 13 | Reserved |
| Bit 12 | |
| Bit 11 | Enables embedding Rec. ITU−R BT.656 synchronization codes in the output data. See R0x19B |
| Bit 10 | Entire image processing is bypassed and raw bayer is output directly.<br>In YCbCr or RGB mode:<br>0: Normal operation, sensor core data flows through IFP.<br>1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; that is, 8 + 2. Data rate is effectively the same as default 16-bit/per pixel modes. Auto exposure/AWB, etc. still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R0x19B |
| Bit 9 | Invert output pixel clock. Inverts output pixel clock. By default, this bit is asserted.<br>0: Output data transitions on the rising edge of PIXCLK for capture by the receiver on the falling edge.<br>1: Output data transitions on the falling edge of PIXCLK for capture by the receiver on the rising edge. |
| Bit 8 | Enables RGB output.<br>0: Output YCbCr data.<br>1: Output RGB format data as defined by R0x13A[7:6]. |
| Bits 7:6 | RGB output format:<br>“00” – 16-bit 565RGB<br>“01” – 15-bit 555RGB<br>“10” – 12-bit 444xRGB<br>“11” – 12-bit x444RGB |
| Bits 5:4 | Test ramp output:<br>“00” – Off<br>“01” – By column<br>“10” – By row<br>“11” – By frame |
| Bit 3 | Outputs RGB or YCbCr values are shifted 3 bits up. Use with R0x13A[5:4] to test LCDs with low color depth. |
| Bit 2 | Averages two nearby chrominance bytes. See R0x19B |
| Bit 1 | In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R0x19B |
| Bit 0 | In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R0x19B |
| **R72:1 – 0x148 – Test Pattern Generator Control (R/W)** | |
| Default | 0x0000 |
| Description | This register enables test pattern generation at the input of the image processor. Values greater than “0” turn on the test pattern generator. The brightness of the flat color areas depends on the value programmed (from 6–1) in this register. The value 7 produces the color bar pattern. Value 0 selects the sensor image. |
| Bit 7 | 1: Forces WB digital gains to 1.0.<br>0: Normal operation. |
| Bits 2:0 | Test pattern selection |

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| **R76:1 – 0x14C – Defect Correction – Context A (R/W)** | |
| Default | 0x0000 |
| Description | Context A register with defect correction, mode enables, and calibration bits |
| Bit 2 | Reserved |
| Bit 1 | Reserved |
| Bit 0 | Enables 2D defect correction |
| **R77:1 – 0x14D – Defect Correction – Context B (R/W)** | |
| Default | 0x0000 |
| Description | Context B register with defect correction, mode enables, and calibration bits |
| Bit 2 | Reserved |
| Bit 1 | Reserved |
| Bit 0 | Enables 2D defect correction |
| **R153:1 – 0x199 – Line Counter (R/O)** | |
| Default | N/A |
| Description | Use line counter to determine the number of the line currently being output |
| Bits 12:0 | Line count |
| **R154:1 – 0x19A – Frame Counter (R/O)** | |
| Default | N/A |
| Description | Use frame counter to determine the index of the frame currently being output |
| Bits 15:0 | Frame count |
| **R155:1 – 0x19B – Output Format Control 2 — Context B (R/W)** | |
| Default | 0x0200 |
| Description | Output format control 2B |
| Bit 14 | Output processed Bayer data |
| Bit 13 | Reserved |
| Bit 12 | |
| Bit 11 | Enables embedding Rec. ITU–R BT.656 synchronization codes to the output data. See R0x13A |
| Bit 10 | Entire image processing is bypassed and raw bayer is output directly.<br>In YCbCr or RGB mode:<br>0: Normal operation, sensor core data flows through IFP.<br>1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to 2 output bytes through the camera interface; that is, 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. AE/AWB, and so on, still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R0x13A. |
| Bit 9 | Invert output pixel clock. Inverts output pixel clock. By default, this bit is asserted.<br>0: Output data transitions on the rising edge of PIXCLK for capture by the receiver on the falling edge.<br>1: Output data transitions on the falling edge of PIXCLK for capture by the receiver on the rising edge. |
| Bit 8 | Enables RGB output.<br>0: Output YCbCr data.<br>1: Output RGB format data as defined by R0x19B[7:6]. See R0x13A. |
| Bits 7:6 | RGB output format:<br>“00” – 16-bit 565RGB<br>“01” – 15-bit 555RGB<br>“10” – 12-bit 444xRGB<br>“11” – 12-bit x444RGB |
| Bits 5:4 | Test Ramp output:<br>“00” – Off<br>“01” – By column<br>“10” – By row<br>“11” – By frame |
| Bit 3 | Output RGB or YCbCr values are shifted 3 bits up. Use with R0x13A[5:4] to test LCDs with low color depth |

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| Bit 2 | Averages two nearby chrominance bytes. See R0x13A |
| Bit 1 | In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R0x13A |
| Bit 0 | In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R0x13A |
| **R159:1 – 0x19F – Reducer Horizontal Pan – Context B (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer horizontal pan in context B |
| Bit 14 | 0: MT9V111-compatible origin at X = 0.<br>1: Centered origin at 640 for more convenient zoom and resize. |
| Bits 10:0 | X pan: Unsigned offset from x = 0 (Bit 14 = 0), or two's complement from X = 640 (Bit 14 = 1) |
| **R160:1 – 0x1A0 – Reducer Horizontal Zoom – Context B (R/W)** | |
| Default | 0x0500 |
| Description | Controls reducer horizontal width of zoom window for FOV in context B |
| Bits 10:0 | X zoom B. Must be ≥ X size B |
| **R161:1 – 0x1A1 – Reducer Horizontal Output Size – Context B (R/W)** | |
| Default | 0x0500 |
| Description | Controls reducer horizontal output size in context B |
| Bits 10:0 | X size B. Must be ≤ X zoom B |
| **R162:1 – 0x1A2 – Reducer Vertical Pan – Context B (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer vertical pan in context B |
| Bit 14 | 0: MT9V111-compatible origin at Y = 0.<br>1: Centered origin at Y = 512 for more convenient zoom and resize. |
| Bits 10:0 | Y pan: unsigned offset from Y = 0 (Bit 14 = 0), or two's complement from Y = 512 (Bit 14 = 1) |
| **R163:1 – 0x1A3 – Reducer Vertical Zoom – Context B (R/W)** | |
| Default | 0x0400 |
| Description | Controls reducer vertical height of zoom window for FOV in context B |
| Bits 10:0 | Y zoom B. Must be ≥ Y size B |
| **R164:1 – 0x1A4 – Reducer Vertical Output Size – Context B (R/W)** | |
| Default | 0x0400 |
| Description | Controls reducer vertical output size in context B |
| Bits 10:0 | Y size B. Must be ≤ Y zoom B |
| **R165:1 – 0x1A5 – Reducer Horizontal Pan – Context A (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer horizontal pan in context A |
| Bit 14 | 0: MT9V111-compatible offset from X = 0.<br>1: Centered origin at 640 for more convenient zoom and resize. |
| Bits 10:0 | X pan: Unsigned offset from X = 0 (Bit 14 = 0), or two's complement from X = 640 (Bit 14 = 1) |
| **R166:1 – 0x1A6 – Reducer Horizontal Zoom – Context A (R/W)** | |
| Default | 0x0500 |
| Description | Controls reducer horizontal width of zoom window for FOV in context A |
| Bits 10:0 | X zoom A. Must be ≥ X size A |
| **R167:1 – 0x1A7 – Reducer Horizontal Output Size – Context A (R/W)** | |
| Default | 0x0280 |
| Description | Controls reducer horizontal output size in context A |
| Bits 10:0 | X size A. Must be ≤ X zoom A |

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| **R168:1 – 0x1A8 – Reducer Vertical Pan – Context A (R/W)** | |
| Default | 0x0000 |
| Description | Controls reducer vertical pan in context A |
| Bit 14 | 0: MT9V111-compatible origin at Y = 0.<br>1: Centered origin at Y = 512 for more convenient zoom and resize. |
| Bits 10:0 | Y pan: unsigned offset from y = 0 (Bit 14 = 0), or two□s complement from Y = 512 (Bit 14 = 1) |
| **R169:1 – 0x1A9 – Reducer Vertical Zoom – Context A (R/W)** | |
| Default | 0x0400 |
| Description | Controls reducer vertical height of zoom window for FOV in context A |
| Bits 10:0 | Y zoom A. Must be ≥ Y size A |
| **R170:1 – 0x1AA – Reducer Vertical Output Size — Context A (R/W)** | |
| Default | 0x0200 |
| Description | Controls reducer vertical output size in context A |
| Bits 10:0 | Y size A. Must be ≤ Y zoom A |
| **R171:1 – 0x1AB – Reducer Current Horizontal Zoom (R/O)** | |
| Default | N/A |
| Description | Current horizontal zoom |
| Bits 10:0 | Current zoom Window Width. After automatic zoom (R0x1AF), copy R0x1AB to the snapshot X zoom register R0x1A6 (context A) or R0x1A0 (context B) so the snapshot has the same FOV as preview. Also copy to snapshot X size register R0x1A7 (context A) or R0x1A1 (context B) for largest snapshot. |
| Bits 15:12 | Reserved. Mask off these bits before performing the above copy operation |
| **R172:1 – 0x1AC – Reducer Current Vertical Zoom (R/O)** | |
| Default | N/A |
| Description | Current vertical zoom |
| Bits 10:0 | Current zoom Window Height. After automatic zoom (R0x1AF), copy R0x1AC to the snapshot Y zoom register R0x1A9 (context A) or R0x1A3 (context B) so the snapshot will have the same FOV as preview. Also copy to snapshot X size register R0x1AA (context A) or R0x1A4 (context B) for largest snapshot. |
| Bits 15:12 | Reserved. Mask off these bits before performing the above copy operation |
| **R174:1 – 0x1AE – Reducer Zoom Step Size (R/W)** | |
| Default | 0x0504 |
| Description | Zoom step sizes. Should be a multiple of the aspect ratio 5:4 for SXGA or 4:3 VGA or 11:9 for CIF |
| Bits 15:8 | Zoom step size in X |
| Bits 7:0 | Zoom step size in Y |
| **R175:1 – 0x1AF – Reducer Zoom Control (R/W)** | |
| Default | 0x0010 |
| Description | Resize interpolation and zoom control |
| Bit 9 | Starts automatic “zoom out” in step sizes defined in R0x1AE |
| Bit 8 | Starts automatic “zoom in” in step sizes defined in R0x1AE |
| Bit 6 | |
| Bit 5 | |
| Bit 4 | |
| Bit 3 | Auto switch to classic interpolation at full resolution |
| Bit 1 | Reserved |
| Bit 0 | Reserved |

**Table 10. COLORPIPE REGISTER DESCRIPTION ADDRESS PAGE 1** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| **R179:1 – 0x1B3 – Global Clock Control (R/W)** | |
| Default | 0x0002 |
| Description | Configures assorted aspects of the clock controller |
| Bits 15:2 | Not used |
| Bit 1 | Tri-states signals in standby mode |
| Bit 0 | |
| **R200:1 – 0x1C8 – Global Context Control (R/W)** | |
| Default | 0x0000 |
| Description | Defines sensor and colorpipe context for current frame. Registers R0x0C8, R0x1C8, and R0x2C8 are shadows of each other. See description in R0x2C8. It is recommended that all updates to R0xnC8 are handled by means of a write to R0x2C8 |
| Bit 15:0 | See R0x2C8[15:0] |
| **R226:1 – 0x1E2 – Effects Mode (R/W)** | |
| Default | 0x7000 |
| Description | This register specifies which of several special effects to apply to each pixel passing through the pixel pipe |
| Bits 15:8 | Solarization threshold |
| Bits 2:0 | Specification of the effects mode.<br>“000” – No effect (pixels pass through unchanged)<br>“001” – Monochrome (chromas set to 0)<br>“010” – Sepia (chromas set to the value in the Effects Sepia register)<br>“011” – Negative (all color channels inverted)<br>“100” – Solarize (luma conditionally inverted)<br>“101” – Solarize2 (luma conditionally inverted, chromas inverted when luma inverted) |
| **R227:1 – 0x1E3 – Effects Sepia (R/W)** | |
| Default | 0xB023 |
| Description | This register specifies the chroma values for the sepia effect. In sepia mode, the chroma values of each pixel are set to this value. By default, this register contains a brownish color, but it can be set to an arbitrary color |
| Bit 15 | Sign of Cb |
| Bits 14:8 | Magnitude of Cb in 0.7 fixed point |
| Bit 7 | Sign of Cr |
| Bits 6:0 | Magnitude of Cr in 0.7 fixed point |
| **R240:1 – 0x1F0 – Page Map (R/W)** | |
| Default | 0x0000 |
| Description | This register specifies the register address page for the two-wire interface protocol |
| Bits 2:0 | Page Address:<br>“000” – Sensor address page<br>“001” – Colorpipe address page<br>“010” – Camera control address page |
| **R241:1 – 0x1F1 – Byte-Wise Address (R/W)** | |
| Default | N/A |
| Description | Special address to perform 8-bit reads and writes to the sensor. For additional information, see “Two-Wire Serial Interface Sample” and “Appendix A – Serial Bus Description”. |

## CAMERA CONTROL REGISTERS

Register WRITEs reach the camera control registers immediately. For non-AE/AWB/CCM registers, register writes take effect immediately.

For AE/AWB and CCM registers, the effects of register writes are dependent on the state of the AE and AWB engines. It may take from zero to many frames for the changes to take effect. Monitor AWB/CCM changes by watching for stable settings in R0x212 (current CCM position), in R0x213 (current AWB red channel), and in R0x214 (current AWB blue channel). Monitor AE changes by watching register R0x24C (AE current luma exposure), and register R0x262 (AE digital gains monitor).

**Table 11. CAMERA CONTROL REGISTER DESCRIPTION**

| Register Number Dec – Hex | Description |
|---|---|
| **R38:2 – 0x226 – Auto Exposure Window Horizontal Boundaries (R/W)** | |
| Default | 0x8000 |
| Description | This register specifies the left and right boundaries of the window used by the AE measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame. |
| Bits 15:8 | Right window boundary |
| Bits 7:0 | Left window boundary |
| **R39:2 – 0x227 – Auto Exposure Window Vertical Boundaries (R/W)** | |
| Default | 0x8008 |
| Description | This register specifies the top and bottom boundaries of the window used by the AE measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the top edge of the frame. |
| Bits 15:8 | Bottom window boundary |
| Bits 7:0 | Top window boundary |
| **R43:2 – 0x22B – Auto Exposure Center Window Horizontal Boundaries (R/W)** | |
| Default | 0x6020 |
| Description | This register specifies the left and right boundaries of the window used by the AE measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame. |
| Bits 15:8 | Right window boundary |
| Bits 7:0 | Left window boundary |
| **R44:2 – 0x22C – Auto Exposure Center Window Vertical Boundaries (R/W)** | |
| Default | 0x6020 |
| Description | This register specifies the top and bottom boundaries of the window used by the AE measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the top edge of the frame. |
| Bits 15:8 | Bottom window boundary |
| Bits 7:0 | Top window boundary |
| **R45:2 – 0x22D – AWB Window Boundaries (R/W)** | |
| Default | 0xF0A0 |
| Description | This register specifies the boundaries of the window used by the AWB measurement engine. Essentially, it describes the AWB measurement window in terms relative to the size of the image – horizontally, in units of 1/10ths of the width of the image; vertically, in units of 1/16 of the height of the image. So although the positioning is highly quantized, the window remains roughly in place as the resolution changes. |
| Bits 15:12 | Bottom window boundary (in units of 1 block) |
| Bits 11:8 | Top window boundary (in units of 1 block) |
| Bits 7:4 | Right window boundary (in units of 2 blocks) |
| Bits 3:0 | Left window boundary (in units of 2 blocks) |

**Table 11. CAMERA CONTROL REGISTER DESCRIPTION** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| **R46:2 – 0x22E – Auto Exposure Target and Precision Control (R/W)** | |
| Default | 0x0C4A |
| Description | This register specifies the luma target of the AE algorithm and the size of the window/range around the target in which no AE adjustment is made. This window is centered on target, but the value programmed in the register is 1/2 of the window size. |
| Bits 15:8 | Half-size of the AE stability window/range |
| Bits 7:0 | Luma value of the AE target |
| **R47:2 – 0x22F – Auto Exposure Speed and Sensitivity Control – Context A (R/W)** | |
| Default | 0xDF20 |
| Description | This register specifies the speed and sensitivity to changes of AE in context A |
| Bit 15 | Reserved |
| Bit 14 | |
| Bits 13:12 | |
| Bit 11 | Reserved |
| Bit 10 | Reserved |
| Bit 9 | Reserved |
| Bits 8:6 | Factor of reduction of the difference between current luma and target luma. In one adjustment AE advances from current luma to target as follows:<br>“000” – 1/4 way going down, 1/8 going up<br>“001” – 1/4 way in both directions<br>“010” – 1/2 way in both directions<br>“011” – 1/2 way going down, 1/4 going up<br>“100” – All the way in both directions (fast adaptation!)<br>“101” – 3/4 way in both directions<br>“110” – 7/8 way in both directions<br>“111” – Reserved. Currently the same as “100” |
| Bit 5 | Reserved |
| Bits 4:3 | Auto exposure luma is updated every N frames, where N is given by this field |
| Bits 2:0 | Hysteresis control through time−averaged smoothing of luma data. Luma measurements for AE are time-averaged as follows:<br>“000” – Auto exposure luma = current luma<br>“001” – Auto exposure luma = 1/2 current luma + 1/2 buffered value<br>“010” – Auto exposure luma = 1/4 current luma + 3/4 buffered value<br>“011” – Auto exposure luma = 1/8 current luma + 7/8 buffered value<br>“100” – Auto exposure luma = 1/16 current luma + 15/16 buffered value<br>“101” – Auto exposure luma = 1/32 current luma + 31/32 buffered value<br>“110” – Auto exposure luma = 1/64 current luma + 63/64 buffered value<br>“111” – Auto exposure luma = 1/128 current luma + 127/128 buffered value |
| **R91:2 – 0x25B – Flicker Control (R/W)** | |
| Default | 0x0002 |
| Description | Primary flicker control register |
| Bit 15 | (Read only) 50 Hz/60 Hz detected<br>0: 50 Hz detected<br>1: 60 Hz detected |
| Bit 2 | |
| Bit 1 | When in “manual” flicker mode (R0x25B[0] = 1), defines which flicker frequency to avoid<br>0: Forces 50 Hz detection<br>1: Forces 60 Hz detection |
| Bit 0 | 0: Auto flicker detection<br>1: Manual mode |

**Table 11. CAMERA CONTROL REGISTER DESCRIPTION** (continued)

| Register Number Dec – Hex | Description |
|---|---|
| **R98:2 – 0x262 – Auto Exposure Digital Gains Monitor (R/W*)** | |
| Default | N/A |
| Description | These digital gains are applied within the IFP; they are independent of the Imager gains |
| Bits 15:8 | Post-lens-correction digital gain (*writable if AE is disabled) |
| Bits 7:0 | Pre-lens-correction digital gain (*writable if AE is disabled) |
| **R103:2 – 0x267 – Auto Exposure Digital Gain Limits (R/W)** | |
| Default | 0x4010 |
| Description | This register specifies the upper limits of the digital gains used by the AE algorithm. The values programmed to this register are 16 times the absolute gain values. The value of 16 represents the gain 1.0. |
| Bits 15:8 | Maximum limit on post-lens-correction digital gain |
| Bits 7:0 | Maximum limit on pre-lens-correction digital gain |
| **R156:2 – 0x29C – Auto Exposure Speed and Sensitivity Control – Context B (R/W)** | |
| Default | 0xDF20 |
| Description | This register specifies the speed and sensitivity to AE changes in context B |
| Bit 15 | Reserved |
| Bit 14 | |
| Bits 13:12 | |
| Bit 11 | Reserved |
| Bit 10 | Reserved |
| Bit 9 | Reserved |
| Bits 8:6 | Factor of reduction of the difference between current luma and target luma. In one adjustment, AE advances from current luma to target as follows:<br>“000” – 1/4 way going down, 1/8 going up<br>“001” – 1/4 way in both directions<br>“010” – 1/2 way in both directions<br>“011” – 1/2 way going down, 1/4 going up<br>“100” – All the way in both directions (fast adaptation!)<br>“101” – 3/4 way in both directions<br>“110” – 7/8 way in both directions<br>“111” – Reserved. Currently the same as “100” |
| Bit 5 | Reserved |
| Bits 4:3 | Auto exposure luma is updated every N frames, where N is given by this field |
| Bits 2:0 | Hysteresis control through time-averaged smoothing of luma data. Luma measurements for AE are time-averaged as follows:<br>“000” – Auto exposure luma = current luma<br>“001” – Auto exposure luma = 1/2 current luma + 1/2 buffered value<br>“010” – Auto exposure luma = 1/4 current luma + 3/4 buffered value<br>“011” – Auto exposure luma = 1/8 current luma + 7/8 buffered value<br>“100” – Auto exposure luma = 1/16 current luma + 15/16 buffered value<br>“101” – Auto exposure luma = 1/32 current luma + 31/32 buffered value<br>“110” – Auto exposure luma = 1/64 current luma + 63/64 buffered value<br>“111” – Auto exposure luma = 1/128 current luma + 127/128 buffered value |
| **R200:2 – 0x2C8 – Global Context Control (R/W)** | |
| Default | 0x0000 |
| Description | Defines sensor and colorpipe context for current frame. Context A is typically used to define preview or viewfinder mode, while context B is typically used for snapshots. The bits of this register *directly* control the respective functions, so care must be taken when writing to this register if a bad frame is to be avoided during the context switch. |
| Bit 15 | Controls assertion of sensor restart on update of global context control register. This helps ensure that the very next frame is generated with the new context (a problem with regard to exposure due to the rolling shutter). This bit is automatically cleared once the restart has occurred.<br>0: Do not restart sensor<br>1: Restart sensor |
| Bit 14 | Reserved |