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1/4-Inch 5 Mp System-On-A-Chip (SOC) CMOS Digital Image Sensor

MT9P111 Datasheet, Rev. G

For the latest datasheet, please visit www.onsemi.com

Features

- Superior low-light performance
- Ultra-low-power, low-cost
- Anti-shake support
- One time programmable memory (OTPM) for automatic positional gain adjustments and other uses
- Parallel data output and serial mobile industry processor interface (MIPI) data output
- Integrated real-time JPEG encoder
- Flexible support for external auto focus
- Internal master clock generated by on-chip phase-locked loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement
- Selectable output data format: YCbCr, 565RGB, 555RGB, 444RGB, JPEG 4:2:2, processed Bayer, RAW8- and RAW10-bit
- Output FIFO for data rate equalization
- Programmable I/O slew rate
- Xenon and LED flash support with fast exposure adaptation
- Configurable gamma correction based on scene brightness
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory, additional serial interface under user control
- Includes internal VCM driver and access to internal A/D converter

Applications

- Cellular phones
- PC cameras
- PDAs

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/4-inch
Full resolution		2592 x 1944 pixels
Pixel size		1.4 µm x 1.4 µm
Dynamic range		62 dB
SNR MAX		35.2 dB
Responsivity		0.68 V/lux-sec
Chief ray angle		25.11° MAX at 80% image height
Color filter array		RGB Bayer pattern
Active pixel array area		3.62 mm x 2.72 mm
Shutter type		Electronic rolling shutter (ERS) and Global reset release (GRR)
Input clock frequency		10–48 MHz
Maximum frame rate		15 fps at full resolution (JPEG), 30 fps in preview mode (VGA bin2 skip2)
Maximum pixel data output		MIPI: 768 Mb/s MAX Parallel: 96 Mp/s
Maximum pixel clock frequency		96 MHz
Supply voltage	Analog	2.5–3.1 V
	Digital	1.7–1.95 V
	I/O	1.7-1.9V or 2.5–3.1 V
	PLL	2.5–3.1 V
	MIPI	2.5–3.1 V
ADC resolution		12-bit, on-die
Power consumption		550 mW at 30 fps, 1280 x 720 video mode
		401 mW at 30 fps, HP preview mode
		230 mW at 23 fps, preview LP mode
Current consumption		10 µA, shutdown, at +70°C
Operating temperature (at junction)		–30°C to +70°C

Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
MT9P111D00STCK28AC1-200	5 MP 1/4" SOC	Die Sales, 200μm Thickness

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MT9P111 Overview

The MT9P111 has a color image sensor with a Bayer color filter arrangement and a 5Mp active-pixel array with electronic rolling shutter (ERS). The sensor core readout is 12-bit, supports skipping and binning, and can be flipped and/or mirrored. The sensor core also supports separate analog and digital gain for all four color channels (R, Gr, Gb, B).

The MT9P111 also has an embedded phase-locked loop oscillator (PLL) that can generate the internal sensor clock from the common clock signals available in typical mobile phone systems. When in use, the PLL adjusts the incoming clock frequency up, allowing the MT9P111 to run at almost any desired resolution and frame rate within the sensor's capabilities. The PLL can be bypassed and powered down to reduce power consumption.

The MT9P111 has numerous power-conserving features including a soft standby mode and a hard standby mode. In standby mode, the sensor can be configured to consume less power than normal operation, with the option of retaining a limited amount of the internal configuration settings. By default, entering standby disables the internal V_{DD} power rail. In addition, there is a SHUTDOWN mode that will disable the power supplies in order to achieve the lowest power consumption possible.

The MT9P111 can be used with either a serial MIPI interface or the parallel data output interface, which has a programmable I/O slew rate to minimize EMI and an output FIFO to eliminate output data bursts. JPEG format can be output in both the MIPI and the parallel data output interfaces. EXIF, MIPI data type support is also included, along with Scalado support.

The advanced image flow processor (IFP) and flexible programmability of the MT9P111 provide a variety of ways to enhance and optimize the image sensor performance. Built-in optimization algorithms enable the MT9P111 to operate at factory settings as a fully automatic, highly adaptable camera; however, most of its settings are user-programmable.

These algorithms include black level conditioning, shading correction, defect correction, noise reduction, color interpolation, color correction, aperture correction, and image formatting such as cropping and scaling.

The MT9P111 also includes a sequencer that coordinates all events triggered by the user. The sequencer manages auto focus, auto white balance, flicker detection, anti-shake, and auto exposure for the different operating modes, which include preview, still capture, video, and snapshot with flash.

All modes of operation are individually configurable and are organized as two contexts. A context is defined by sensor image size, frame rate, resolution, and other associated parameters. The user can switch between the two contexts by sending a command through the two-wire serial interface.

A two-wire serial register interface bus enables read/write access to control registers, variables, and special function registers within the MT9P111. The hardware registers include sensor core controls, color pipeline controls, and output controls.

The general purpose VGPIO can be configured to allow the user extended platform functionality or achieve a 10-bit parallel Bayer output.

Signal Description

Table 3 provides the signal descriptions for the MT9P111.

Table 3: Signal Descriptions

Name	Type	Description	Notes
STANDBY	Input	Controls sensor's standby mode, active HIGH.	
RESET_BAR	Input	Master reset signal, active LOW (can be left floating if not used).	
SHUTDOWN	Input	Complete shutdown function for lowest power state (Must be tied to DGND if not used)	
EXTCLK	Input	Input clock signal 10–48 MHz. For low leakage, do not overdrive input signal.	
VPP	Input	High voltage programming pin for one-time programmable (OTP) memory (must be left floating for normal operation).	
SCLK	Input	Slave two-wire serial interface clock from the host processor.	
SADDR	Input	Selects device address for the slave two-wire serial interface. The address is 0x78 when SADDR is tied LOW, 0x7A if tied HIGH.	
SDATA	I/O	Slave two-wire serial interface data to and from the host processor.	
S_SCL	Output	Master two-wire serial interface clock to peripheral devices like AF mechanics.	
S_SDA	I/O	Master two-wire serial interface data to peripheral devices like AF mechanics.	
VGPIO[7:0]	I/O	General purpose digital I/O, used for auto focus function (can be left floating if not used).	
DOUT[7:0]	Output	8-bit image data output or most significant bits (MSB) of 10-bit SOC bypass mode. If 10-bit Bayer is desired, VGIO[1:0] can be configured to output two least significant bits (LSB).	
PIXCLK	Output	Pixel clock. Used for sampling DOUT, FRAME_VALID, and LINE_VALID.	
LINE_VALID	Output	Identifies pixels in the active line.	
FRAME_VALID	Output	Identifies rows in the active image.	
DOUT_N	Output	Differential MIPI data (sub-LVDS, negative) (must be left floating if not used).	
DOUT_P	Output	Differential MIPI data (sub-LVDS, positive) (must be left floating if not used).	
CLK_N	Output	Differential MIPI clock (sub-LVDS, negative) (must be left floating if not used).	
CLK_P	Output	Differential MIPI clock (sub-LVDS, positive) (must be left floating if not used).	
VCM_OUT	I/O	VCM actuator driver pad.	
VCM_GND	I/O	Ground pad for VCM_OUT.	
ATEST0	I/O	Internal ADC access (leave floating if not used).	
ATEST1	I/O	Internal ADC access (leave floating if not used).	
TEST_EN	Input	Test enable (Must be tied to DGND).	
VDD	Supply	Digital power (1.8V typical).	
VAA_PIX	Supply	Pixel array power (2.8V typical).	
VAA	Supply	Analog power (2.8V typical).	
VDD_PLL	Supply	PLL power (2.8V typical).	
VDD_IO	Supply	I/O power supply (1.8V or 2.8V typical).	
GND_IO	Supply	I/O ground.	
DGND	Supply	Digital ground.	1
AGND	Supply	Analog ground.	1
VDDIO_TX	Supply	I/O power supply for the MIPI output interface, 2.8V typical, Can be disconnected if the interface is not used.	
GNDIO_TX	Supply	I/O ground supply for the MIPI output interface. Can be disconnected if the interface is not used).	

Table 3: Signal Descriptions

Name	Type	Description	Notes
VDD_VGPIO	Supply	I/O power supply for VGPIO[7:0] signals. Can be either 1.8 V or 2.8 V typical. Must be connected even if not used.	
GND_VGPIO	Supply	I/O ground for VGPIO[7:0]. Must be connected even if not used.	

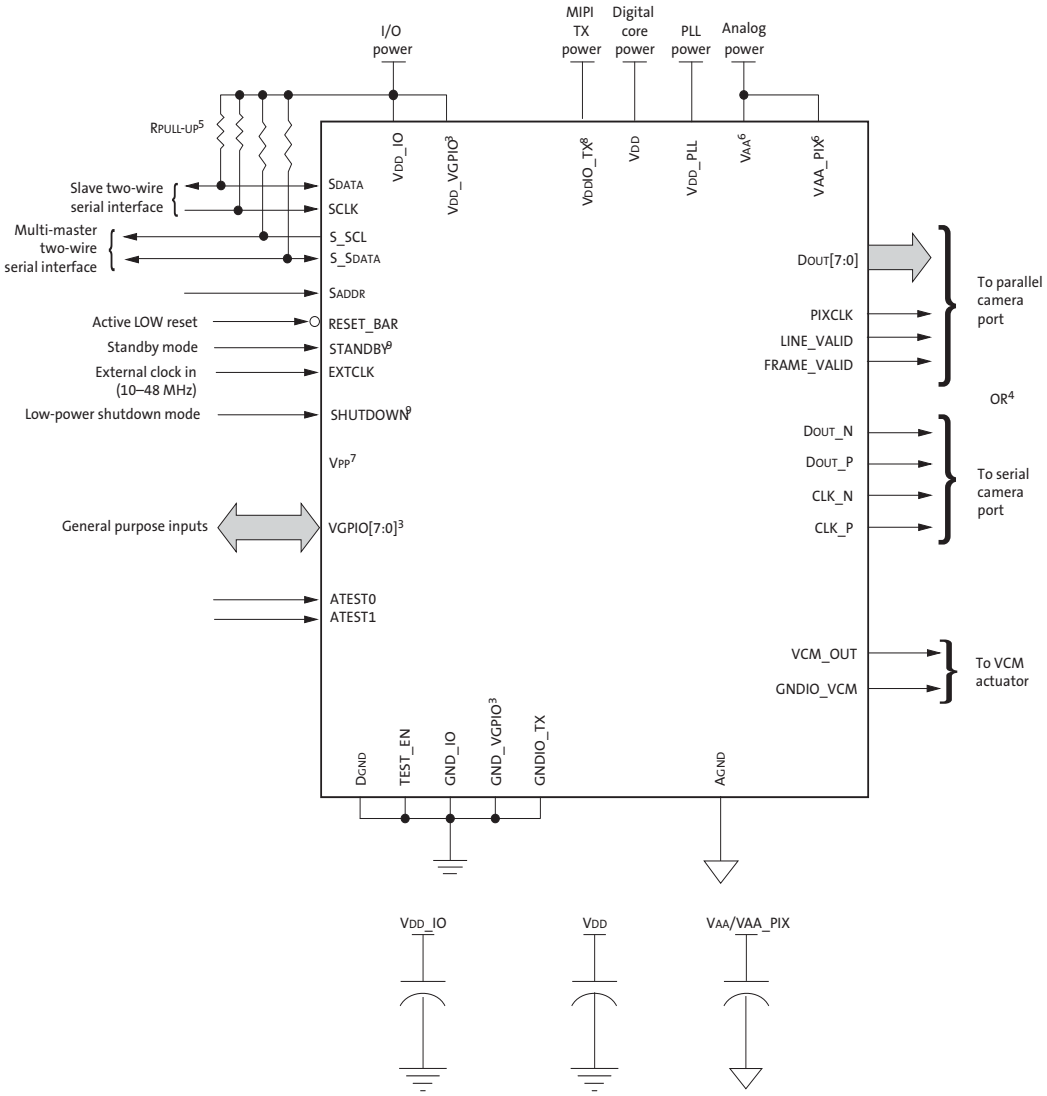
Note: AGND and DGND are not connected internally (inside the chip).

Typical Connections

Figure 1 on page 9 shows typical MT9P111 device connections. For low-noise operation, the MT9P111 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled from ground using capacitors as close as possible to the die. ON Semiconductor does not recommend the use of inductance filters on the power supplies or output signals.

The MT9P111 supports different digital core (VDD/DGND), MIPI output (VDDIO_TX/GNDIO_TX), and I/O (VDD_IO/GND_IO) power domains that can be at different voltages. The PLL requires a clean power source (VDD_PLL).

Figure 1: Typical Configuration (connection)



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor. The minimum recommended decoupling configuration is 0.1µF per supply on module and 10µF off module.
2. If a MIPI interface is not required, the following pads must be left floating: DOUT_P, DOUT_N, CLK_P, and CLK_N.
3. The VGPIO pads can serve multiple features that can be reconfigured. The function and direction will vary by applications. If VGPIO pads are not required, the VDD_VGPIO, GND_VGPIO, and VGPIO[7:0] pads can be left floating.
4. Only one of the output modes (serial or parallel) can be used at any time.
5. ON Semiconductor recommends a resistor value of 1.5KΩ to VDD_IO for the two-wire serial interface Rpull-up; however, greater values may be used for slower transmission speeds.
6. VAA and VAA_PIX must be tied together.
7. VPP is the one-time programmable (OTP) memory programming voltage and should be left floating during normal operation.
8. VDDIO_TX can be connected to VDD_IO if VDD_IO = 2.8V. If the MIPI output is not used, VDDIO_TX can be tied to the VAA supply if an ON Semiconductor-recommended decoupling capacitor is used. VDDIO_TX must be connected to a 2.8V supply.

9. If STANDBY and SHUTDOWN pins are not used, they must be connected to DGND.

Decoupling Capacitor Recommendations

The minimum decoupling capacitor recommendation is 0.1 µF per supply in the module.

It is important to provide clean, well regulated power to each power supply. The ON Semiconductor recommendation for capacitor placement and values are based on our internal demo camera design and verified in hardware.

Note: Since hardware design is influenced by many factors, such as layout, operating conditions, and component selection, the customer is ultimately responsible to ensure that clean power is provided for their own designs.

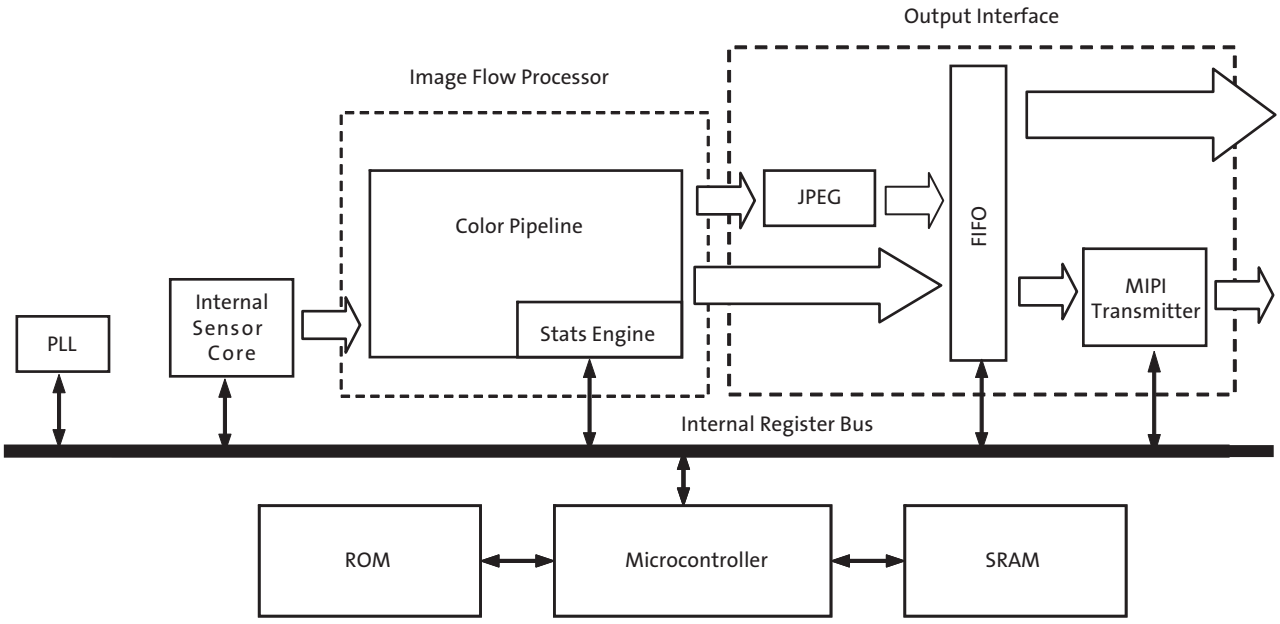
In order of preference, ON Semiconductor recommends:

1. Mount 0.1µF and 1µF decoupling capacitors for each power supply as close as possible to the pad and place a 10 µF capacitor nearby off-module.
2. If module limitations allow for only six decoupling capacitors for a three-regulator design (VDD_PLL tied to VAA), use a 0.1µF and 1µF capacitor for each of the three regulated supplies. ON Semiconductor also recommends placing a 10µF capacitor for each supply off-module, but close to each supply.
3. If module limitations allow for only three decoupling capacitors, a 1µF capacitor for each of the three regulated supplies is preferred. ON Semiconductor recommends placing a 10µF capacitor for each supply off-module but closed to each supply.
4. If module limitations allow for only three decoupling capacitors, a 0.1µF capacitor for each of the three regulated supplies is preferred. ON Semiconductor recommends placing a 10µF capacitor for each supply off-module but close to each supply.
5. Priority should be given to the VAA supply for additional decoupling capacitors.
6. Inductive filtering components are not recommended.
7. Follow best practices when performing physical layout. Refer to technical notes TN-09-131 and TN-09-214.

Architecture Overview

The MT9P111 combines a 5Mp sensor core with an image flow processor (IFP) to form a stand-alone solution that includes both image acquisition and processing. Both the sensor core and the IFP have internal registers that can be controlled by the user. In normal operation though, an integrated microcontroller autonomously controls most aspects of operation. The processed image data is transmitted to the host system either through a parallel bus or a serial data interface through the output interface.

Figure 2: SOC Block Diagram



Sensor Core Description

The sensor core of the MT9P111 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate, qualified by LINE_VALID (LV) and FRAME_VALID (FV). The maximum pixel rate is 96 Mp/s, corresponding to a pixel clock rate of 96 MHz. Figure 3 shows a block diagram of the sensor core. It includes a 5Mp active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 12-bit value compressed to a 10-bit value for each pixel in the array.

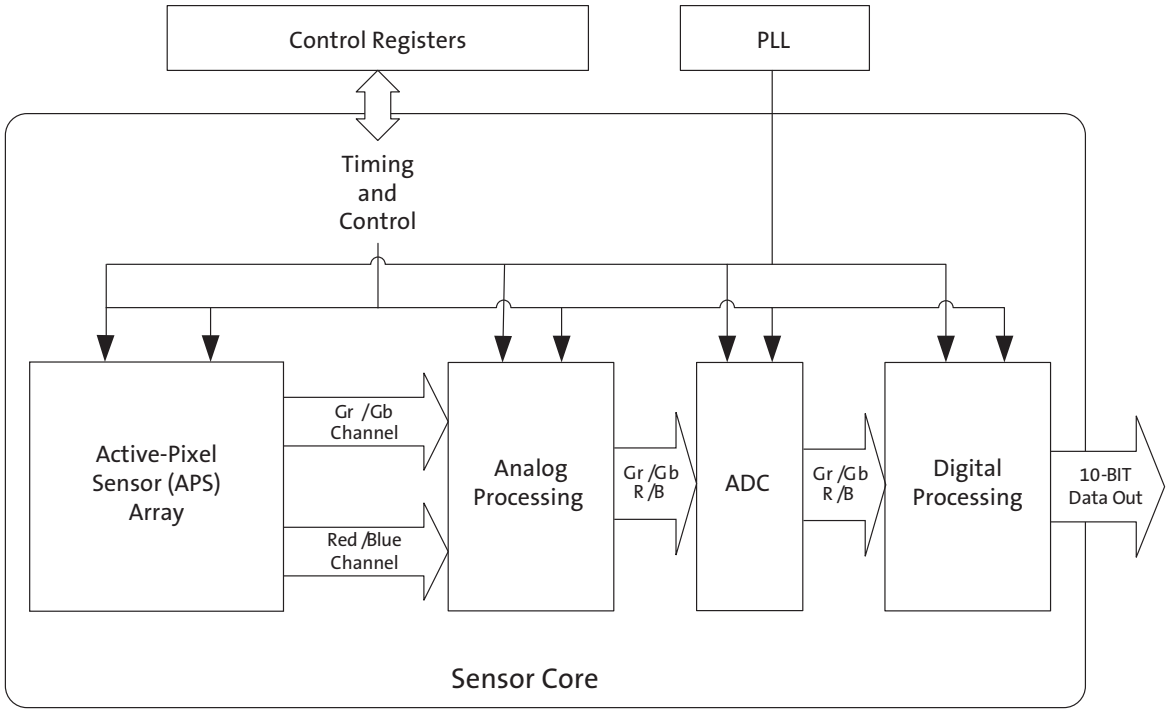
The pixel array contains optically active and light-shielded (dark) pixels. The dark pixels are used to provide data for the offset-correction algorithms (black level control).

The sensor core contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers are controlled by the SOC firmware and can be accessed through a two-wire serial interface. Register values written to the sensor core maybe overwritten by firmware.

The output from the core is a Bayer pattern; alternate rows are a sequence of either green and red pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

A flash strobe output signal is provided to allow an external xenon or LED light source to synchronize with the sensor exposure time. Additional I/O signals support the provision of an external mechanical shutter.

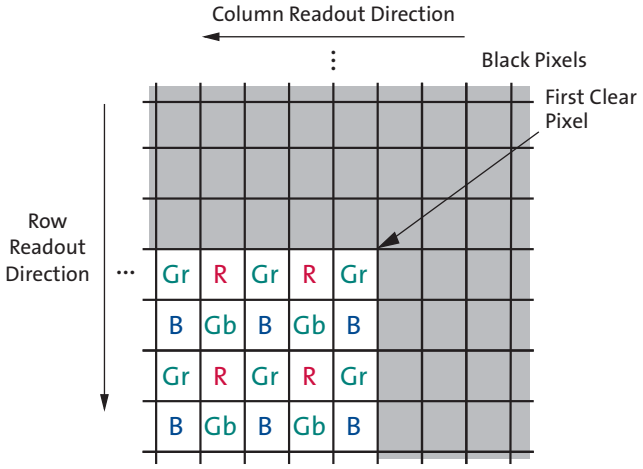
Figure 3: Sensor Core Block Diagram



Pixel Array

The sensor core uses a Bayer color pattern, as shown in Figure 4.

Figure 4: Pixel Color Pattern Detail (Top Right Corner)

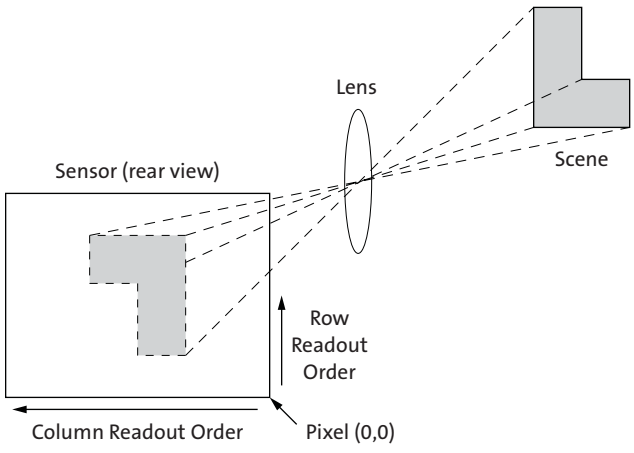


Default Readout Order

When the sensor is operating in a system, the active surface of the sensor faces the scene as shown in Figure 5.

When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced. By convention, data from the sensor is shown with the first pixel read out in the case of the sensor core in the top left corner.

Figure 5: Imaging a Scene



PLL

PLL-Generated Clocks

The PLL can generate a pixel clock signal whose frequency is up to 96 MHz, using a EXTCLK input of 10 through 48 MHz.

PLL Setup

Because the input clock frequency is unknown, the sensor starts up with the PLL disabled. The PLL takes time to power up. The behavior of its output clock signal during lock phase is not guaranteed. Another limitation is that the pll_bypass cannot be turned off until after the analog core is powered up. Failure to do so may make the clocking inoperable.

Digital Processing

Readout Options

The sensor core supports different readout options to modify the image before it is sent to the IFP. The readout can be limited to a specific window of the original pixel array.

For preview modes, the sensor core supports both skipping and binning in x and y directions.

By changing the readout direction the image can be flipped in the vertical and/or mirrored in the horizontal.

Window Size

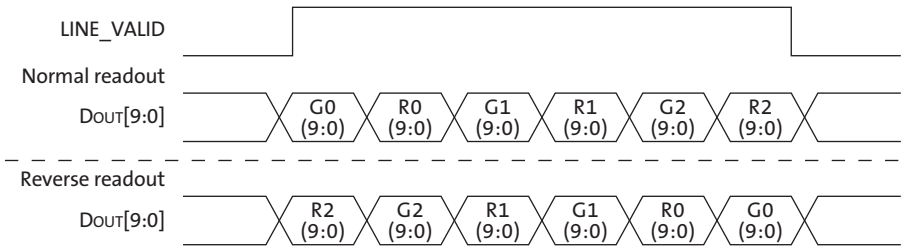
The image output size is set using firmware variables. The edge pixels in the array are present to avoid edge defects and should not be included in the visible window. Binning or skipping will change the image output size.

Readout Modes

Horizontal Mirror

When the sensor is configured to mirror the image horizontally, the order of pixel readout within a row is reversed. Figure 6 shows a sequence of 6 pixels being read out with normal readout and reverse readout.

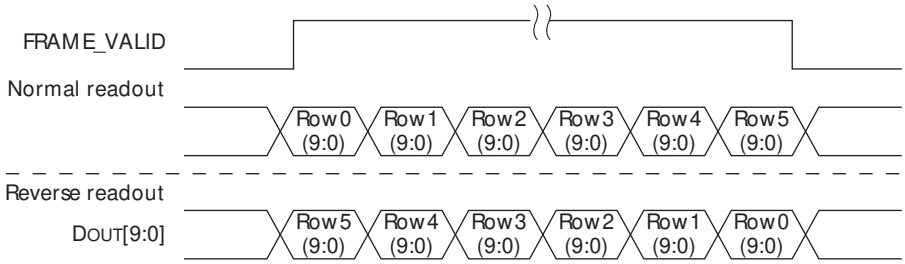
Figure 6: 6 Pixels in Normal and Column Mirror Readout Modes



Vertical Flip

When the sensor is configured to flip the image vertically, the order in which pixel rows are read out is reversed. Figure 7 shows a sequence of 6 rows being read out with normal readout and reverse readout.

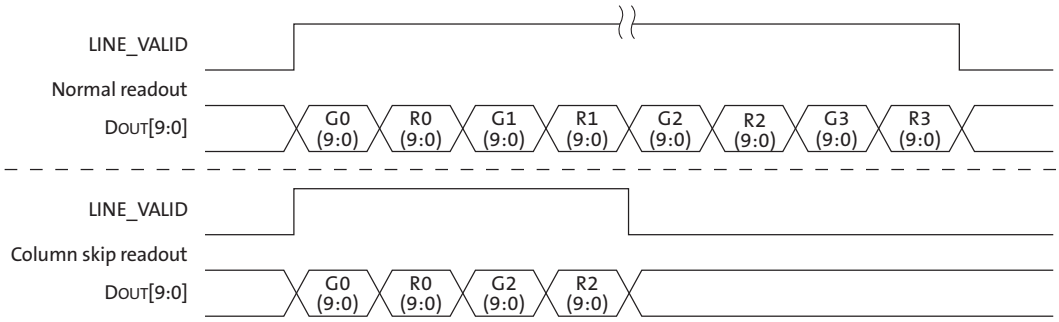
Figure 7: Six Rows in Normal and Row Mirror Readout Modes



Column and Row Skip

The sensor core supports subsampling. Subsampling reduces the amount of data processed by the analog signal chain in the sensor and thereby allows the frame rate to be increased. This reduces the amount of row and column data processed and is equivalent to the skip2 readout mode provided by earlier ON Semiconductor imaging sensors. When enabling subsampling, the proper image output and crop sizes must be updated beforehand.

Figure 8: 8 Pixels in Normal and Column Skip 2X Readout Modes



Pixel Readouts

The following diagrams show a sequence of data being read out with no skipping. The effect of the different subsampling on the pixel array readout is shown in Figures 9 through 13.

Figure 9: Pixel Readout (no skipping)

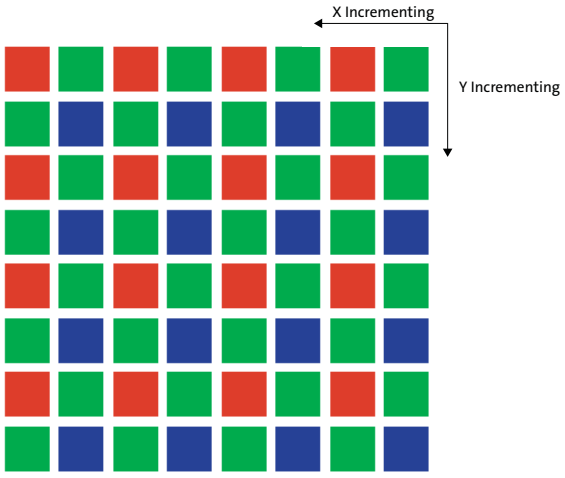


Figure 10: Pixel Readout (column skipping)

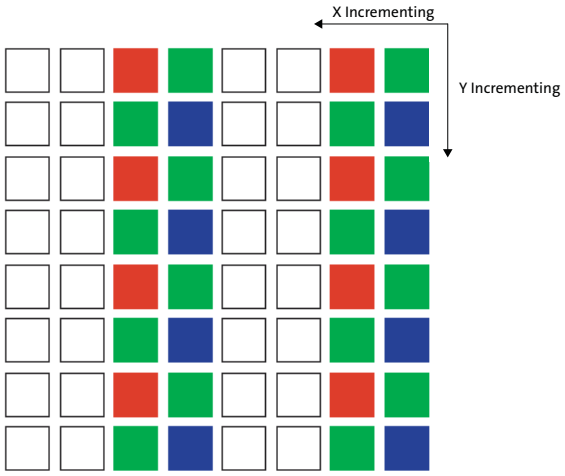


Figure 11: Pixel Readout (row skipping)

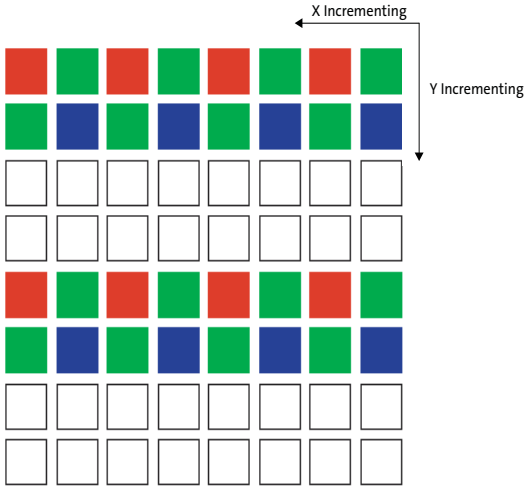


Figure 12: Pixel Readout (column and row skipping)

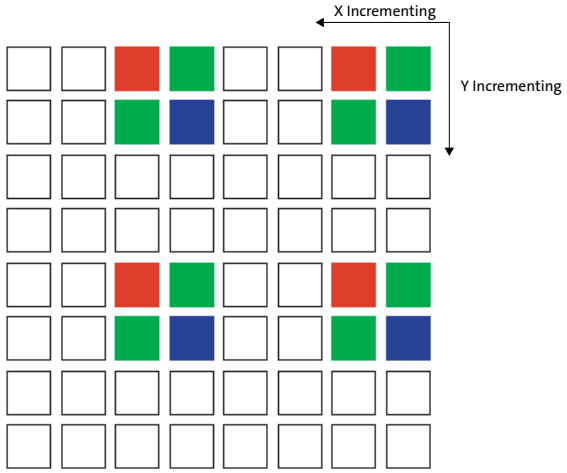


Table 4: Row Address Sequencing (Sampling)

Normal	Subsampled Sequence 1	Subsampled Sequence 2
0	0	No data
1	1	No data
2	No data	2
3	No data	3
4	4	No data
5	5	No data
6	No data	6
7	No data	7

Binning

The MT9P111 sensor core supports 2 x 1, 2 x 2, and Bin2-Skip4 analog binning (column binning, also called x-binning and row/column binning, also called xy-binning). Binning has many of the same characteristics as subsampling but because it gathers image data from all pixels in the active window (rather than a subset of them), it achieves superior image quality and avoids the aliasing artifacts that can be a characteristic side effect of subsampling.

Binning is enabled by selecting the appropriate subsampling settings. Subsampling may require sensor window size adjustment when binning is enabled.

The effect of the different subsampling settings is shown in Figure 13 and Figure 14 on page 19.

Figure 13: Pixel Readout (column binning)

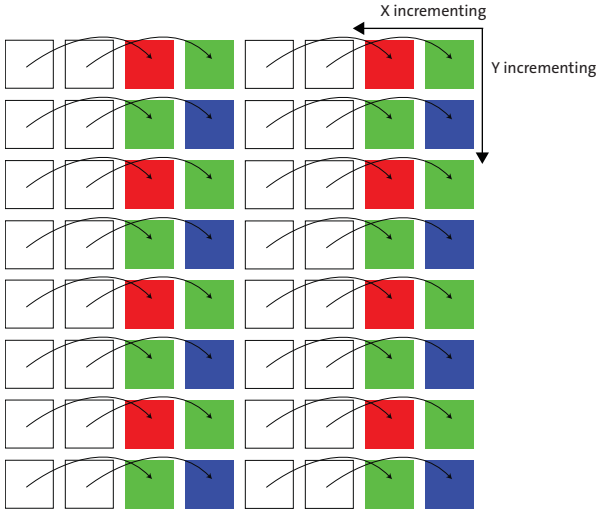
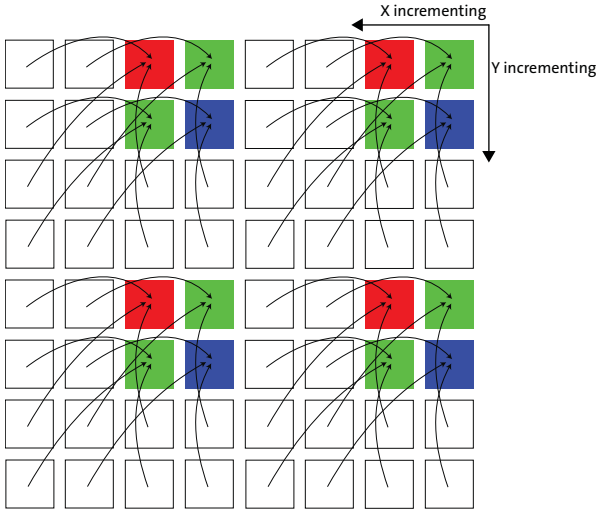


Figure 14: Pixel Readout (column and row binning)



Binning Limitations

The sensor must be taken out of streaming mode before switching between binned and non-binned operation. Binning requires different sequencing of the pixel array and imposes different timing limits on the operation of the sensor. In particular, xy-binning requires two read operations from the pixel array for each line of output data, which has the effect of increasing the minimum line blanking time.

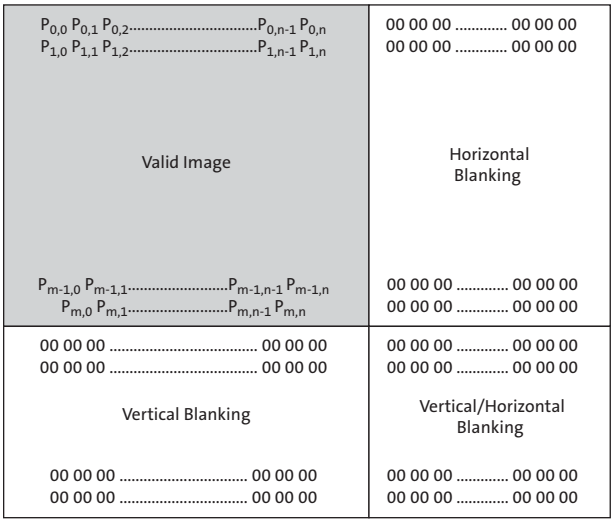
Table 5: Row Address Sequencing (Binning)

Normal	Binning Sequence 1	Binning Sequence 2
0	0,2	No data
1	1,3	No data
2	No data	2,4
3	No data	3,5
4	4,6	No data
5	5,7	No data
6	No data	6,8
7	No data	7,9

Raw Data Format

The sensor core image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 15 on page 20. The amount of horizontal blanking and vertical blanking is programmable. LV is HIGH during the shaded region of the figure.

Figure 15: Valid Image Data

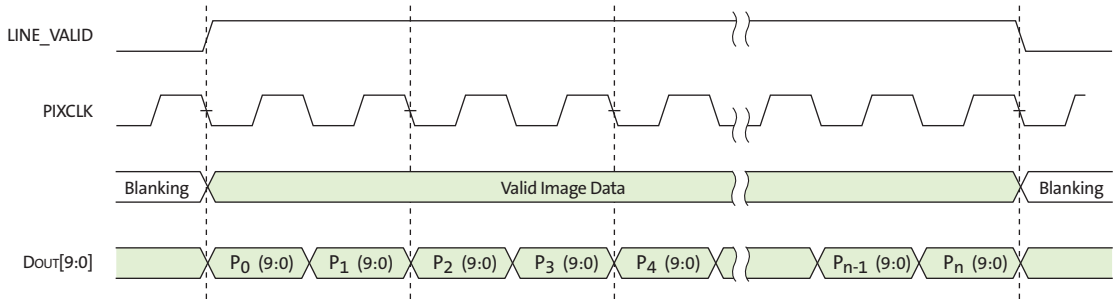


Raw Data Timing

DOUT[9:0]is synchronized with the PIXCLK output. When LV is HIGH, one pixel's data is output on the 10-bit DOUT output bus every PIXCLK period. By default, the PIXCLK signal runs at the same frequency as the master clock, and its rising edges occur one-half

of a master clock period after transitions on LV, FV, and DOUT (see Figure 16). This allows PIXCLK to be used as a clock to sample the data. PIXCLK is continuously enabled by default (but is configurable), even during the blanking period.

Figure 16: Pixel Data Timing Example



Power Reduction Modes

Low Power Mode

The MT9P111 supports low power operation during preview mode by reducing the pixel clock frequency. When the MT9P111 enters preview mode with low power mode enabled (Sensor core register 0x3040[9] = 1), the sensor clock will be reduced by half. Internal logic will disable the pixel clock and re-program the divider value. Internal delay will be applied during this change to avoid any clock glitches.

Dynamic Power Mode

Dynamic Power Mode setting can also be used to significantly reduce the power levels in the sensor. Dynamic power mode will turn off power to the analog portions of the sensor that are not being utilized.

The following registers need to be asserted to enter dynamic power modes:

REG = 0x3170[11] = 1, Enable dynamic power modes

REG = 0x3EDA[6] = 1

REG = 0x3EDA[14] = 1

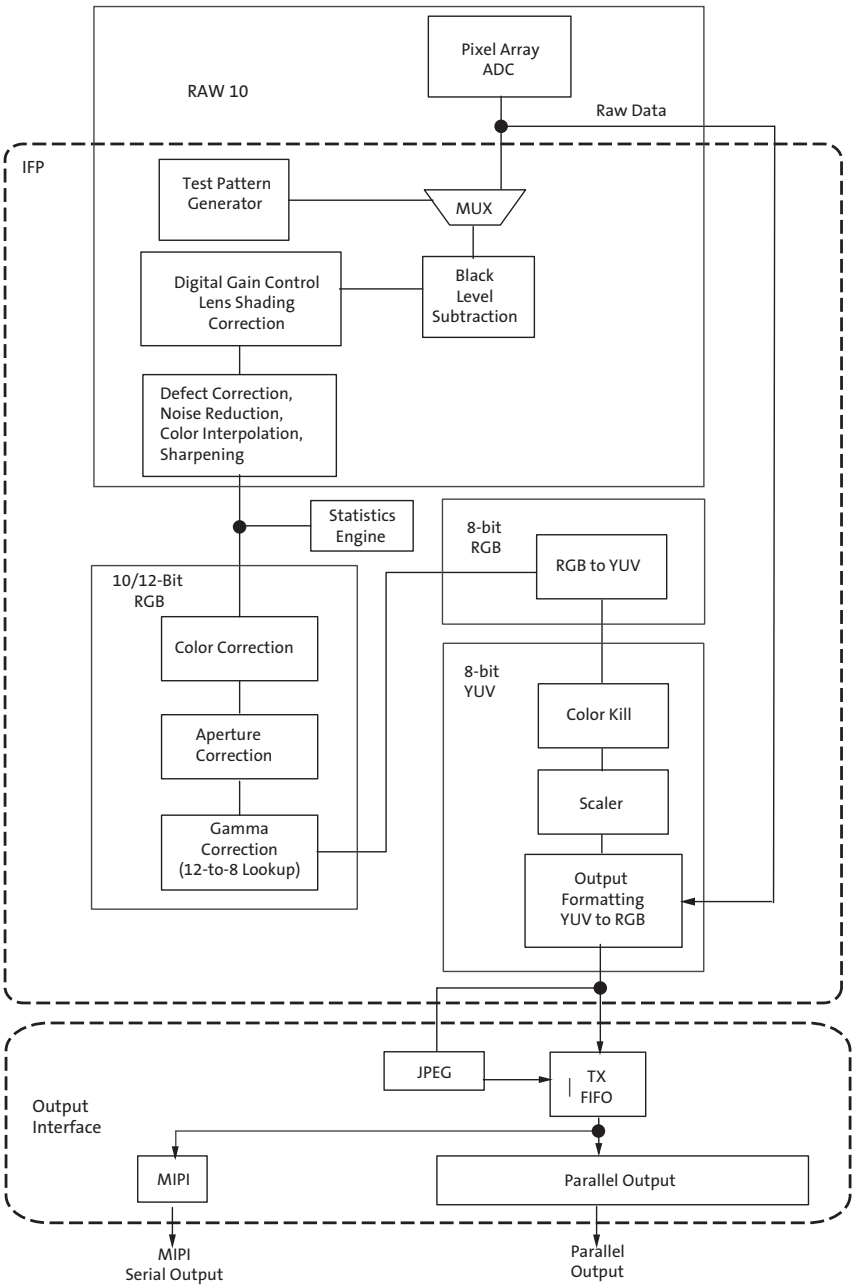
REG = 0x3EDA[15] = 1

SOC Description

Image Flow Processor

Image and color processing in the MT9P111 are implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operation parameters. The IFP is broken down into different sections, as outlined in Figure 17.

Figure 17: Color Pipeline

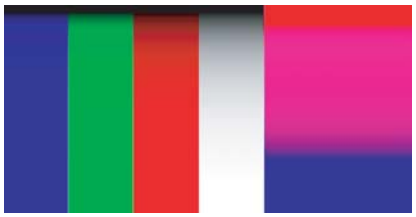


Test Patterns

During normal operation of the MT9P111, a stream of raw image data from the sensor core is continuously fed into the color pipeline. For test purposes, this stream can be replaced with a fixed image generated by a special test module in the pipeline. The module provides a selection of test patterns sufficient for basic testing of the pipeline.

Test patterns are accessible by programming a register and are shown in Figure 18. Disabling the MCU is recommended before enabling test patterns.

Figure 18: Color Bar Test Pattern

Test Pattern	Example
Flat Field	
Vertical Ramp	
Color Bar	
Vertical Stripes	
Pseudo-Random	

Black Level Subtraction and Digital Gain

Image stream processing starts with black level subtraction and multiplication of all pixel values by a programmable digital gain. Both operations can be independently set to separate values for each color channel (R, Gr, Gb, B). Independent color channel digital gain can be adjusted with registers. Independent color channel black level adjustments can also be made. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to "0."

Automatic Positional Gain Adjustments (APGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The MT9P111 has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

In some cases, different lighting conditions can introduce different color shading response. To compensate for the dependency of the lens shading to the illuminant that can result, different settings of lens shading correction (LC) coefficients can be used. The MT9P111 provides up to three settings to be stored. Each PGA setting should be optimized at a particular color temperature. In the MT9P111, color temperature is detected, stored in the firmware variable ccmPosition, and an appropriate PGA setting is applied.

The variable (ccmPosition) has a range from 0 through 255 and reflects the current color temperature, 0 corresponding to lowest color temperature, 255 the highest. The host specifies a range of ccmPosition values for a particular PGA setting. The ranges should overlap to provide hysteresis and prevent thrashing between PGA settings.

The Correction Function

For each illuminant, color-dependent solutions are calibrated using the sensor, lens system, and an image of an evenly illuminated, featureless gray calibration field. From the resulting image, the color correction functions can be derived.

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row,col) = P_{sensor}(row,col) * f(row,col) \quad \text{(EQ 1)}$$

where P are the pixel values and f is the color dependent correction functions for each color channel.

One-Time Programmable Memory

The MT9P111 contains 5Kb of OTP memory, suitable for storing three separate lens shading correction settings, color calibration, external mechanisms, initialization settings, and module identification that can be programmed during the module manufacturing process. Programming the OTP memory requires the use of a high voltage at the VPP pin. During normal operation, the VPP pin should be left floating. The OTP memory can be accessed through the two-wire serial interface. Refer to the MT9P111 Developer Guide for programming procedures.

There is a one-time programmable memory timing calculator available for customer use. Please contact ON Semiconductor engineering support.

Defect Correction and Noise Reduction

The IFP performs continuous defect correction that can mask pixel array defects such as high dark-current (hot) pixels and pixels that are darker or brighter than their neighbors due to photoresponse nonuniformity. The module is edge-aware with exposure that is based on configurable thresholds. The thresholds are changed continuously based on the brightness of the current scene. Noise reduction can be enabled and disabled and thresholds can be set through register settings.

Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10-bit integer number, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one-color-per-pixel nature of the data stream, but after the defect correction it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10-bit numbers. Since such sums can have up to 12 significant bits, the bit width of the image data stream is widened to 12-bits per color (36 bits per pixel). The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color-corrected image data. The gain and threshold for 2D correction can be defined through register settings.