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MT9P401

MT9P401 1/2.5-Inch 5 Mp CMOS Digital Image Sensor

Table 1. KEY PERFORMANCE PARAMETERS

Parameter		Value
Optical Format		1/2.5−inch (4:3)
Active Imager Size		5.70 mm (H) x 4.28 mm (V) 7.13 mm Diagonal
Active Pixels		2592 (H) x 1944 (V)
Pixel Size		2.2 x 2.2 μm
Color Filter Array		RGB Bayer Pattern
Shutter Type		Global Reset Release (GRR), Snapshot Only Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		96 Mp/s at 96 MHz (2.8 V I/O) 48 Mp/s at 48 MHz (1.8 V I/O)
Frame Rate	Full Resolution	Programmable up to fps
	HDTV (1280 x 720)	Programmable up to 60 fps
ADC Resolution		12−bit, On−chip
Responsivity		1.4 V/lux−sec (550 nm)
Pixel Dynamic Range		70.1 dB
SNR_{MAX}		38.1 dB
Supply Voltage	I/O	1.7−3.1 V
	Digital	1.7−1.9 V (1.8 V Nominal)
	Analog	2.6−3.1 V (2.8 V Nominal)
Power Consumption		381 mW at 15 fps Full Resolution
Operating Temperature		−30°C to +70°C
Packaging		48−pin iLCC, Die

Features

- High Frame Rate
- Superior Low−light Performance
- Low Dark Current
- Global Reset Release, which Starts the Exposure of all Rows Simultaneously
- Bulb Exposure Mode, for Arbitrary Exposure Times
- Snapshot Mode to Take Frames on Demand
- Horizontal and Vertical Mirror Image
- Column and Row Skip Modes to Reduce Image Size without Reducing Field−of−view (FOV)
- Column and Row Binning Modes to Improve Image Quality when Resizing

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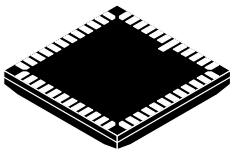

ILCC48 10x10
CASE 847AA

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features (continued)

- Simple Two−wire Serial Interface
- Programmable Controls: Gain, Frame Rate, Frame Size, Exposure
- Automatic Black Level Calibration
- On−chip Phase−locked Loop (PLL)
- 720p HDTV Video at 60 fps

Applications

- Digital Still Cameras
- Digital Video Cameras
- PC Cameras
- Converged DSCs/camcorders
- Cellular Phones
- PDAs

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9P401D00C18B−N3001−200	VGA 1/3” GS CIS	Die Sales, 200 μm Thickness
MT9P401I12STC−DP	5 MP 1/2.5” CIS	Dry Pack with Protective Film
MT9P401I12STC−DR	5 MP 1/2.5” CIS	Dry Pack without Protective Film

GENERAL DESCRIPTION

The ON Semiconductor MT9P401 is a 1/2.5−inch CMOS active−pixel digital image sensor with an active imaging pixel array of 2592 (H) × 1944 (V). It incorporates sophisticated camera functions on−chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two−wire serial interface.

The 5 Mp CMOS image sensor features ON Semiconductor’s breakthrough low−noise CMOS imaging technology that achieves CCD image quality (based on signal−to−noise ratio and low−light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The MT9P401 sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a full resolution image at 15 frames per second (fps).

An on−chip analog−to−digital converter (ADC) provides 12 bits per pixel. FRAME_VALID (FV) and LINE_VALID (LV) signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

TheMT9P401 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous HDTV video and single frames makes it the perfect choice for a wide range of consumer and

FUNCTIONAL OVERVIEW

The MT9P401 is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum pixel rate is 96 Mp/s, corresponding to a clock rate of 96 MHz. Figure 1 illustrates a block diagram of the sensor.

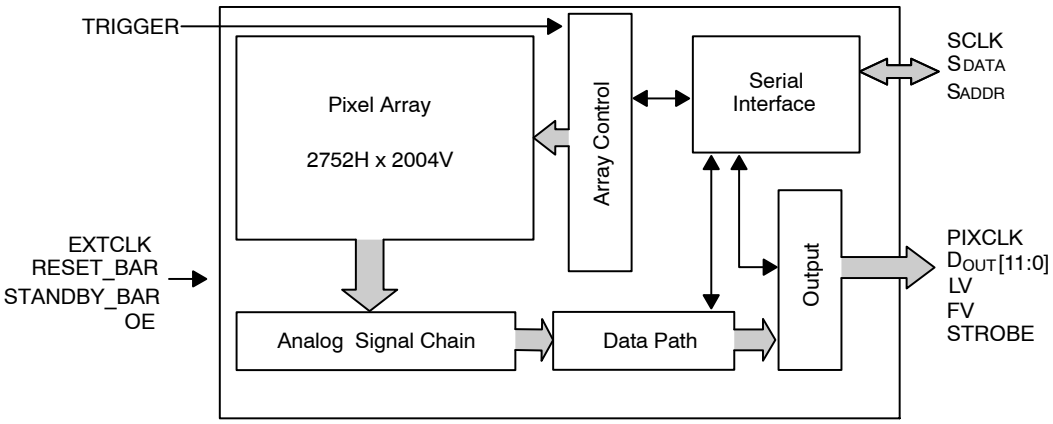

Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 5 Mp active−pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 96 Mp/s, in addition to frame and line synchronization signals.

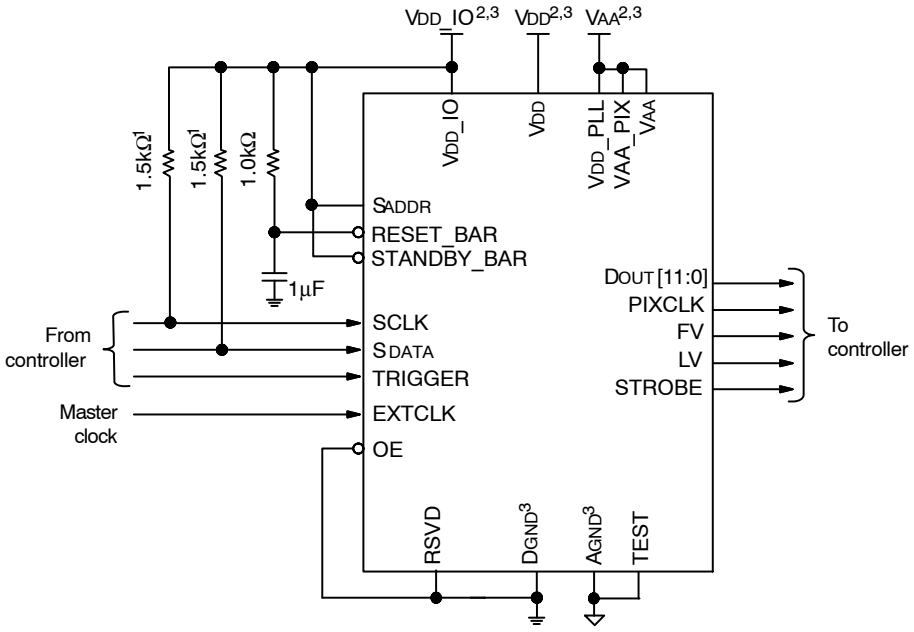

Figure 2. Typical Configuration (Connection)

NOTE:
1. A resistor value of 1.5 kΩ is recommended, but may be greater for slower two-wire speed.
2. All power supplies should be adequately decoupled.
3. All DGND pins must be tied together, as must all AGND pins, all VDD_IO pins, and all VDD pins.

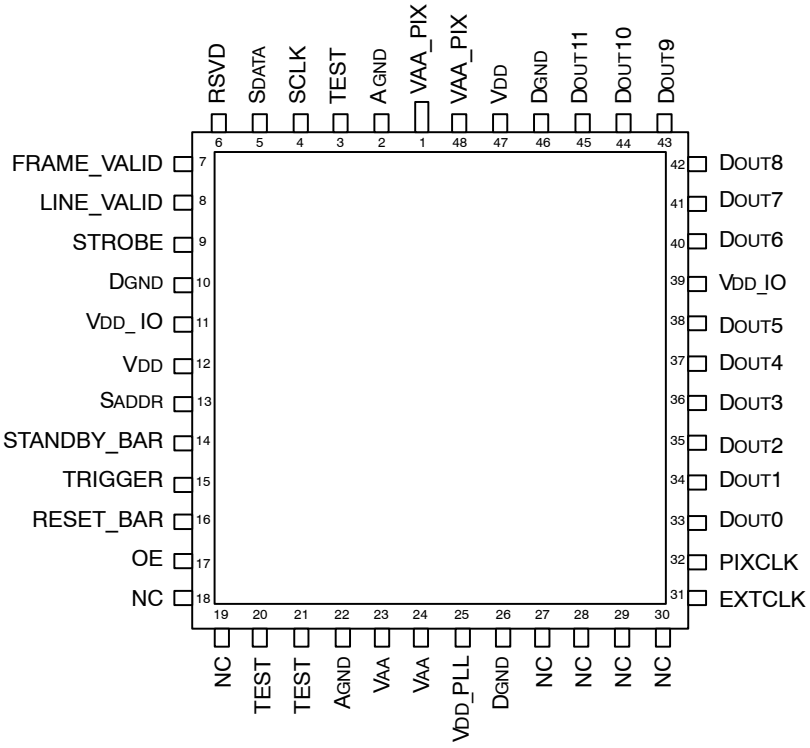

Figure 3. 48-Pin iLCC 10 x 10 Package Pinout Diagram (Top View)

Table 3. PIN DESCRIPTION

Name	Type	Description
RESET_BAR	Input	When LOW, the MT9P401 asynchronously resets. When driven HIGH, it resumes normal operation with all configuration registers set to factory defaults
EXTCLK	Input	External input clock
SCLK	Input	Serial clock. Pull to V_{DD}_IO with a 1.5 kΩ resistor
OE	Input	When HIGH, the PIXCLK, DOUT, FV, LV, and STROBE outputs enter a High−Z. When driven LOW, normal operation resumes
STANDBY_BAR	Input	Standby. When LOW, the chip enters a low−power standby mode. It resumes normal operation when the pin is driven HIGH
TRIGGER	Input	Snapshot trigger. Used to trigger one frame of output in snapshot modes, and to indicate the end of exposure in bulb exposure modes
SADDR	Input	Serial address. When HIGH, the MT9P401 responds to device ID $(BA)_H$. When LOW, it responds to serial device ID $(90)_H$
SDATA	I/O	Serial data. Pull to V_{DD}_IO with a 1.5 kΩ resistor
PIXCLK	Output	Pixel clock. The DOUT, FV, LV, and STROBE outputs should be captured on the falling edge of this signal
DOUT[11:0]	Output	Pixel data. Pixel data is 12−bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK
FRAME_VALID	Output	Frame valid. Driven HIGH during active pixels and horizontal blanking of each frame and LOW during vertical blanking
LINE_VALID	Output	Line valid. Driven HIGH with active pixels of each line and LOW during blanking periods
STROBE	Output	Snapshot strobe. Driven HIGH when all pixels are exposing in snapshot modes
V_{DD}	Supply	Digital supply voltage. Nominally 1.8 V
V_{DD}_IO	Supply	IO supply voltage. Nominally 1.8 or 2.8 V
DGND	Supply	Digital ground
V_{AA}	Supply	Analog supply voltage. Nominally 2.8 V
VAA_PIX	Supply	Pixel supply voltage. Nominally 2.8 V, connected externally to V_{AA}
AGND	Supply	Analog ground
V_{DD}_PLL	Supply	PLL supply voltage. Nominally 2.8 V, connected externally to V_{AA}
TEST	—	Tie to AGND for normal device operation (factory use only)
RSVD	—	Tie to DGND for normal device operation (factory use only)
NC	—	No connect

PIXEL DATA FORMAT

Pixel Array Structure

The MT9P401 pixel array consists of a 2752−column by 2004−row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper−right corner of the entire array, looking at the sensor, as shown in Figure 4.

The array consists of a 2592−column by 1944−row active region in the center representing the default output image, surrounded by a boundary region (also active), surrounded by a border of dark pixels (see Table 4 and Table 5). The boundary region can be used to avoid edge effects when doing color processing to achieve a 2592 × 1944 result image, while the optically black column and rows can be used to monitor the black level.

Pixels are output in a Bayer pattern format consisting of four “colors”−GreenR, GreenB, Red, and Blue (Gr, Gb, R, B)−representing three filter colors. When no mirror modes are enabled, the first row output alternates between Gr and R pixels, and the second row output alternates between B and Gb pixels. The Gr and Gb pixels have the same color filter, but they are treated as separate colors by the data path and analog signal chain.

Table 4. PIXEL TYPE BY COLUMN

Column	Pixel Type
0–9	Dark (10)
10–15	Active boundary (6)
16–2607	Active image (2592)
2608–2617	Active boundary (10)
2618–2751	Dark (134)

Table 5. PIXEL TYPE BY ROW

Column	Pixel Type
0–49	Dark (50)
50–53	Active boundary (4)
54–1997	Active image (1944)
1998–2001	Active boundary (3)
2002–2003	Dark (2)

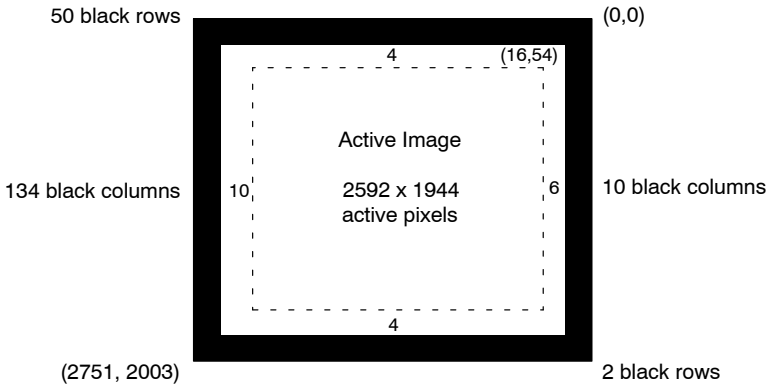

Figure 4. Pixel Array Description

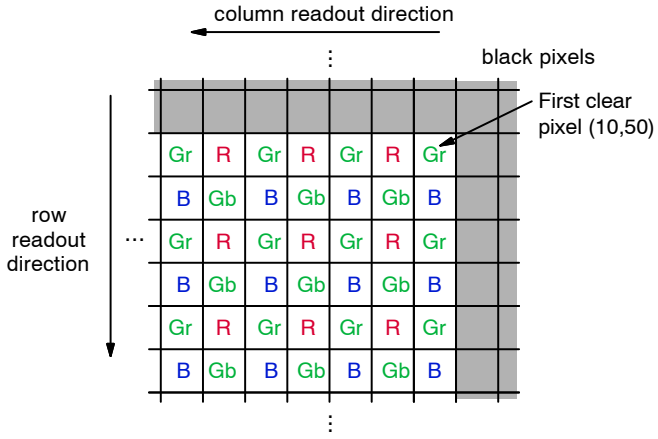

Figure 5. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 4). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (16, 54).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 5. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

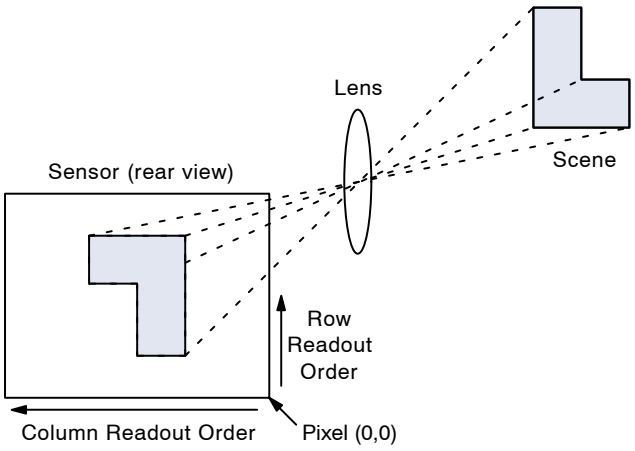

Figure 6. Imaging a Scene

Output Data Format (Default Mode)

The MT9P401 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 7. LV is HIGH during the shaded region of the figure. FV timing is described in “Output Data Timing”.

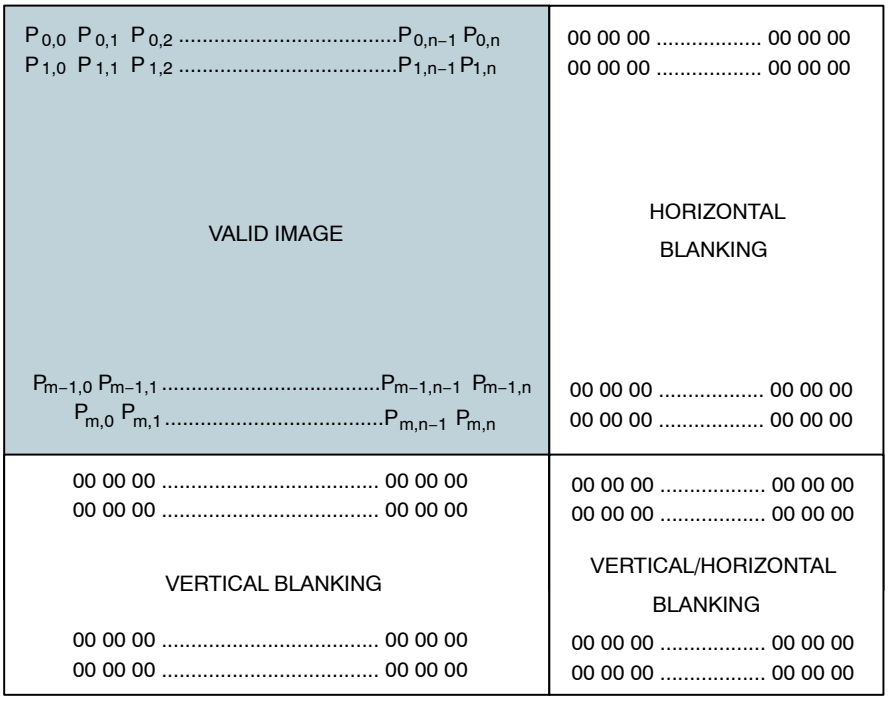

Figure 7. Spatial Illustration of Image Readout

Readout Sequence

Typically, the readout window is set to a region including only active pixels. The user has the option of reading out dark regions of the array, but if this is done, consideration must be given to how the sensor reads the dark regions for its own purposes.

1. Dark rows:
   If Show_Dark_Rows is set, or if Manual_BLC is clear, dark rows on the top of the array are read out. The set of rows sampled are adjusted based on the Row_Bin setting such that there are 8 rows after binning, as shown in the Table 6.
   The Row_Skip setting is ignored for the dark row region.
   If Show_Dark_Rows is clear and Manual_BLC is set, no dark rows are read from the array as part of this step, allowing all rows to be part of the active image. This does not change the frame time, as H_{DR} is included in the vertical blank period.
2. Active image:
   The rows defined by the row start, row size, bin, skip, and row mirror settings are read out. If this set of rows includes rows read out above, those rows are resampled, meaning that the data is invalid.

Table 6. DARK ROWS SAMPLED AS A FUNCTION OF ROW_BIN

Row_Bin	H_{DR} (Dark Rows After Binning)
0	8
1	8
3	8

Columns are read out in the following order:

1. Dark columns:
   If either Show_Dark_Columns or Row_BLC is set, dark columns on the left side of the image are read out followed by those on the right side. The set of columns read is shown in Table 7.
   The Column_Skip setting is ignored for the dark columns.
   If neither Show_Dark_Columns nor Row_BLC is set, no dark columns are read, allowing all columns to be part of the active image. This does not change the row time, as W_{DC} is included in the vertical blank period.
2. Active image:
   The columns defined by column start, column size, bin, skip, and column mirror settings are read out. If this set of columns includes the columns read out above, these columns are resampled, meaning the data is invalid.

Table 7. DARK COLUMNS SAMPLED AS A FUNCTION OF COLUMN_BIN

Column_Bin	W_{DC} (Dark Columns After Binning)
0	80
1	40
3	20

OUTPUT DATA TIMING

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 1944 rows of 2592 columns each. The FV and LV signals indicate the boundaries between frames and lines, respectively. PIXCLK can be used as a clock to latch the data. For each PIXCLK cycle, one 12−bit pixel datum outputs on the DOUT pins. When both FV and LV are asserted, the pixel is valid. PIXCLK cycles that occur when FV is negated are called vertical blanking. PIXCLK cycles that occur when only LV is negated are called horizontal blanking.

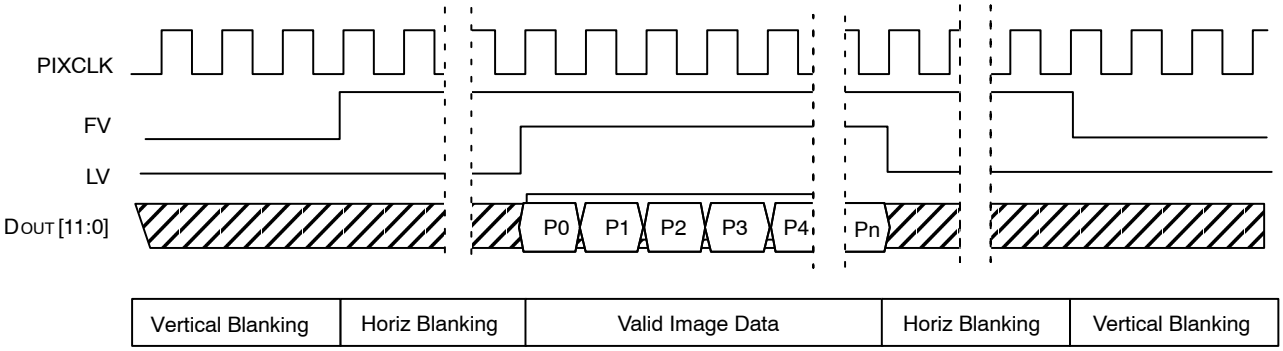

Figure 8. Default Pixel Output Timing

LV and FV

The timing of the FV and LV outputs is closely related to the row time and the frame time.

FV will be asserted for an integral number of row times, which will normally be equal to the height of the output image. If Show_Dark_Rows is set, the dark sample rows will be output before the active image, and FV will be extended to include them. In this case, FV's leading edge happens at time 0.

LV will be asserted during the valid pixels of each row. The leading edge of LV will be offset from the leading edge of FV by 609 PIXCLKs. If Show_Dark_Columns is set, the dark columns will be output before the image pixels, and LV will be extended back to include them; in this case, the first pixel of the active image still occurs at the same position relative to the leading edge of FV. Normally, LV will only be asserted if FV is asserted; this is configurable as described below.

LV Format Options

The default situation is for LV to be negated when FV is negated. The other option available is shown in Figure 9. If Continuous_LV is set, LV is asserted even when FV is not, with the same period and duty cycle. If XOR_Line_Valid is set, but not Continuous_Line_Valid, the resulting LV will be the XOR of FV and the continuous LV.

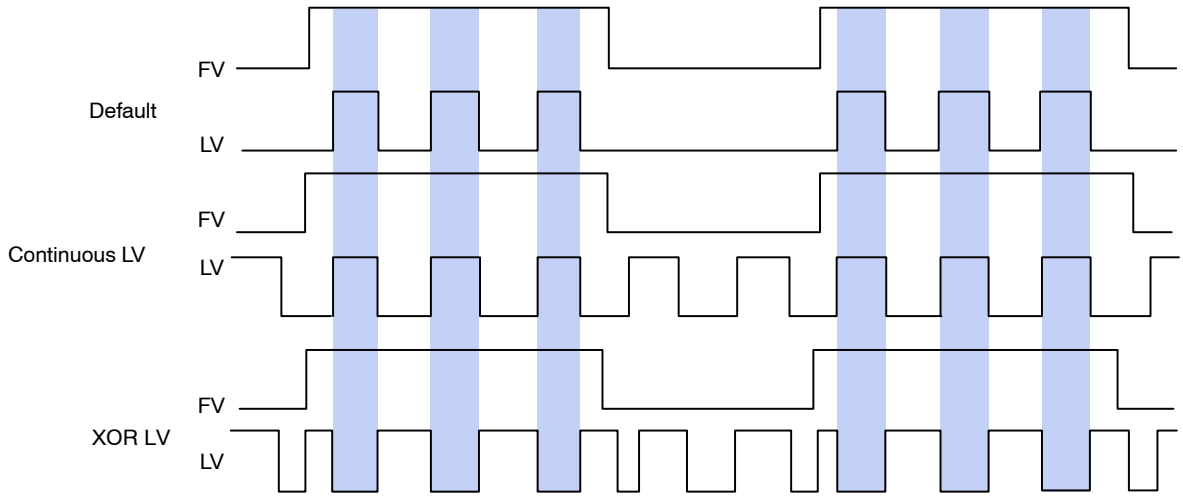

Figure 9. LV Format Options

The timing of an entire frame is shown in Figure 10.

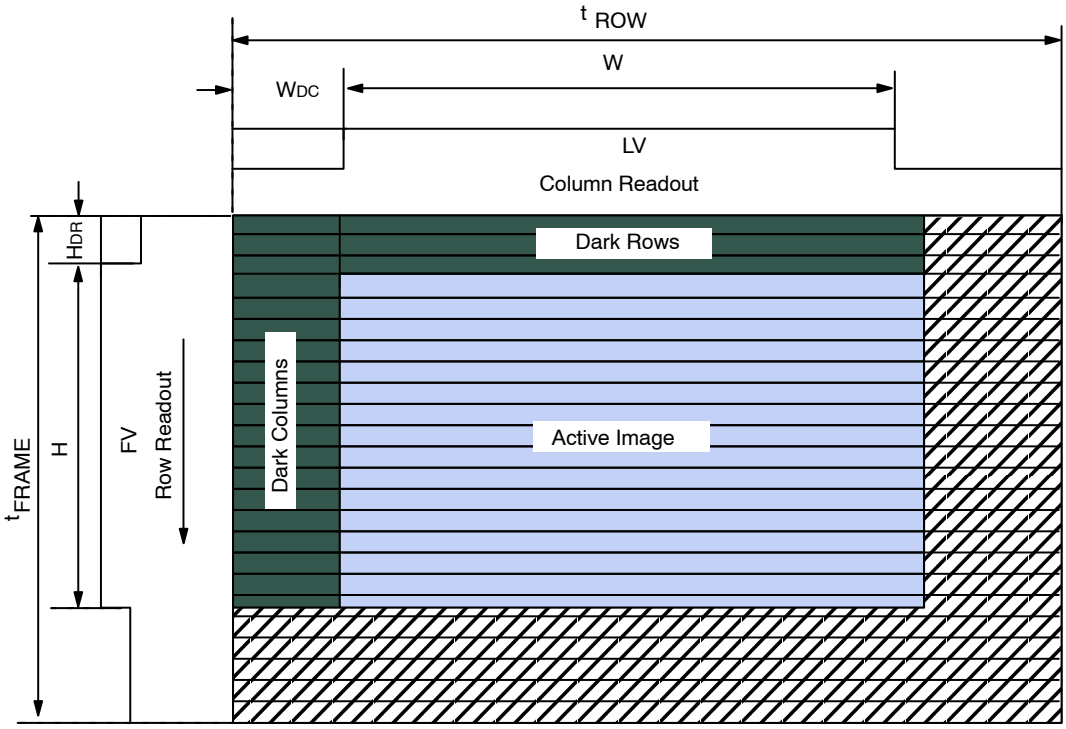

Figure 10. Frame Timing

Frame Time

The pixel clock (PIXCLK) represents the time needed to sample 1 pixel from the array, and is typically equal to 1 EXTCLK period. The sensor outputs data at the maximum rate of 1 pixel per PIXCLK. One row time (^{t}ROW) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 8.

Table 8. FRAME TIME

Parameters	Name	Equation	Default Timing at EXTCLK = 96 MHz
fps	Frame Rate	1/^{t}FRAME	14
^{t}FRAME	Frame Time	(H + max(VB, VB$_{MIN}$)) × ^{t}ROW	71.66 ms
^{t}ROW	Row Time	2 × ^{t}PIXCLK × max(((W/2) + max(HB, HB$_{MIN}$)), (41 + 346 × (Row_Bin+1) + 99))	36.38 µs
^{t}ROW_Default	Row Time	2 × ^{t}PIXCLK × max(((W/2) + max(HB, HB$_{MIN}$)), (41 + 346 × (Row_Bin+1) + 99))	36.38 µs
^{t}ROW_HDTV	Row Time	2 × ^{t}PIXCLK × max(((W/2) + max(HB, HB$_{MIN}$)), (41 + 186 × (Row_Bin+1) + 99))	24.4 µs
W	Output Image Width	2 × ceil((Column_Size + 1) / (2 × (Column_Skip + 1)))	2592 PIXCLK
H	Output Image Height	2 × ceil((Row_Size + 1) / (2 × (Row_Skip + 1)))	1944 rows
SW	Shutter Width	max (1, (2 16 × Shutter_Width_Upper) + Shutter_Width_Lower)	1943 rows
HB	Horizontal Blanking	Horizontal_Blank + 1	1 PIXCLK
VB	Vertical Blanking	Vertical_Blank + 1	26 rows
HB$_{MIN}$	Minimum Horizontal Blanking	346 × (Row_Bin + 1) + 64 + (W$_{DC}$ / 2)	450 PIXCLK
VB$_{MIN}$	Minimum Vertical Blanking	max (8, SW – H) + 1	9 rows
^{t}PIXCLK	Pixclk Period	1/^{f}PIXCLK	10.42 ns

The minimum horizontal blanking (HBMIN) values for various Row_Bin and Column_Bin settings are shown in Table 9.

Table 9. HB_{MIN} VALUES FOR ROW_BIN VS. COLUMN_BIN SETTINGS

	Column_bin (W_{DC})			
Row_bin		0	1	3
	0	450	430	420
	1	796	776	766
	3	1488	1468	1458

Frame Rates at Common Resolutions

Table 10 and Table 11 show examples of register settings to achieve common resolutions and their frame rates. Frame rates are shown both with subsampling enabled and disabled.

Table 10. STANDARD RESOLUTIONS

Resolution	Frame Rate	Sub–sampling Mode	Column_ Size (R0x04)	Row_ Size (R0x03)	Shutter_ Width_ Lower (R0x09)	Row_ Bin (R0x22 [5:4])	Row_ Skip (R0x22 [2:0])	Column_ Bin (R0x23 [5:4])	Column_ Skip (R0x23 [2:0])
2592 x 1944 (Full Resolution)	14	N/A	2591	1943	<1943	0	0	0	0
2048 x 1536 QXGA	21	N/A	2047	1535	<1535	0	0	0	0
1600 x 1200 UXGA	31	N/A	1599	1199	<1199	0	0	0	0
1280 x 1024 SXGA	42	N/A	1279	1023	<1023	0	0	0	0
1024 x 768 XGA	63	N/A	1023	767	<767	0	0	0	0
	63	Skipping	2047	1535		0	1	0	1
	47	Binning	2047	1535		1	1	1	1
800 x 600 SVGA	90	N/A	799	599	<599	0	0	0	0
	90	Skipping	1599	1199		0	1	0	1
	65	Binning	1599	1199		1	1	1	1
640 x 480 VGA	123	N/A	639	479	<479	0	0	0	0
	123	Skipping	2559	1919		0	3	0	3
	53	Binning	2559	1919		3	3	3	3

Table 11. WIDE SCREEN (16:9) RESOLUTIONS

Resolution	Frame Rate	Sub–sampling Mode	Column_ Size (R0x04)	Row_ Size (R0x03)	Shutter_ Width_ Lower (R0x09)	Row_ Bin (R0x22 [5:4])	Row_ Skip (R0x22 [2:0])	Column_ Bin (R0x23 [5:4])	Column_ Skip (R0x23 [2:0])
1920 x 1080 HDTV	31	N/A	1919	1079	<1079	0	0	0	0
1280 x 720 HDTV	60	Binning	2559	1439	<719	1	1	1	1

1. It is assumed that the minimum horizontal blanking and the minimum vertical blanking conditions are met, and that all other registers are set to default values. Please refer to TN09111 for instructions on how to configure 720p HDTV.

SERIAL BUS DESCRIPTION

Registers are written to and read from the MT9P401 through the two−wire serial interface bus. The MT9P401 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9P401 through the serial data (SDATA) line. The SDATA line is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can pull the SDATA line LOW—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial defines several different transmission codes, as follows:

1. a start bit
2. the slave device 8-bit address
3. an (a no) acknowledge bit
4. an 8-bit message
5. a stop bit

Sequence

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8−bit address. The last bit of the address determines if the request is a READ or a WRITE, where a "0" indicates a WRITE and a "1" indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request is a WRITE, the master then transfers the 8−bit register address to which a WRITE should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9P401 uses 16−bit data for its internal registers, thus requiring two 8−bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write−mode slave address and 8−bit register address, just as in the WRITE request. The master then sends a start bit and the read−mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is automatically−incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH−to−LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW−to−HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8−bit address of a two−wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB (least significant bit) of the address indicates write mode (0xBA), and a "1" indicates read mode (0xBB).

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two−wire serial interface clock−it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no−acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no−acknowledge bit is used to terminate a read sequence.

TWO-WIRE SERIAL INTERFACE SAMPLE WRITE AND READ SEQUENCES

16-Bit WRITE Sequence

A typical WRITE sequence for writing 16 bits to a register is shown in Figure 11. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16−bit data. After each 8−bit transfer, the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

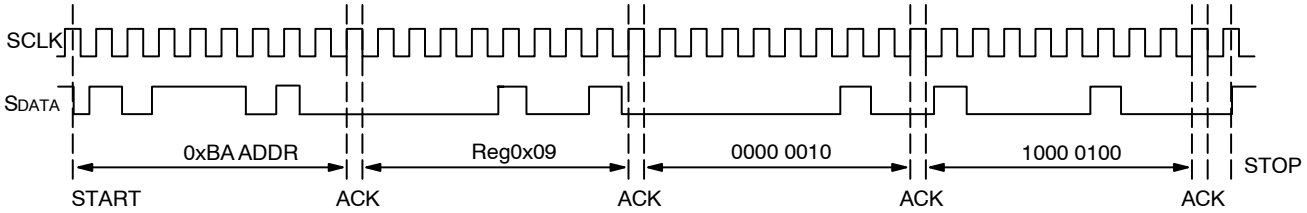

Figure 11. Timing Diagram Showing a WRITE to Reg0x09 with the Value 0x0284

16-Bit READ Sequence

A typical READ sequence is shown in Figure 12. First the master has to write the register address, as in a WRITE sequence. Then a start bit and the read address specify that a READ is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

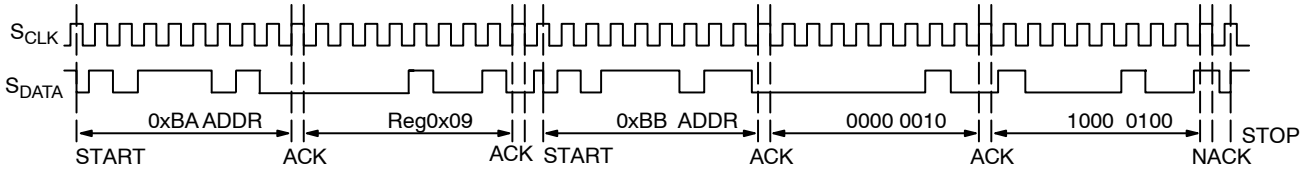

Figure 12. Timing Diagram Showing a READ to Reg0x09 with the Value 0x0284

REGISTERS

Register List

Table 12 lists sensor registers and their default values.

Table 12. REGISTER LIST AND DEFAULT VALUES

(1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic)

Register # Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R0:0(R0x000)	Chip Version	???? ???? ???? ????	6145 (0x1801)
R1:0(R0x001)	Row Start	0000 0ddd dddd dddd	54 (0x0036)
R2:0(R0x002)	Column Start	0000 dddd dddd dddd	16 (0x0010)
R3:0(R0x003)	Row Size	0000 0ddd dddd dddd	1943 (0x0797)
R4:0(R0x004)	Column Size	0000 dddd dddd dddd	2591 (0x0A1F)
R5:0(R0x005)	Horizontal Blank	0000 dddd dddd dddd	0 (0x0000)
R6:0(R0x006)	Vertical Blank	0000 0ddd dddd dddd	25 (0x0019)
R7:0(R0x007)	Output Control	0d0d dddd dddd dddd	8066 (0x1F82)
R8:0(R0x008)	Shutter Width Upper	0000 0000 0000 dddd	0 (0x0000)
R9:0(R0x009)	Shutter Width Lower	dddd dddd dddd dddd	1943 (0x0797)
R10:0(R0x00A)	Pixel Clock Control	d000 0ddd 0ddd dddd	0 (0x0000)
R11:0(R0x00B)	Restart	0000 0000 0000 0ddd	0 (0x0000)
R12:0(R0x00C)	Shutter Delay	000d dddd dddd dddd	0 (0x0000)
R13:0(R0x00D)	Reset	0000 0000 0000 000d	0 (0x0000)
R15:0(R0x00F)	Reserved	–	0 (0x0000)
R16:0(R0x010)	PLL Control	ddd0 000d dddd 00dd	80 (0x0050)
R17:0(R0x011)	PLL Config 1	dddd dddd 00dd dddd	25604 (0x6404)
R18:0(R0x012)	PLL Config 2	000d dddd 000d dddd	0 (0x0000)
R20:0(R0x014)	Reserved	–	54 (0x0036)
R21:0(R0x015)	Reserved	–	16 (0x0010)
R30:0(R0x01E)	Read Mode 1	0ddd dddd dddd dddd	16390 (0x4006)
R32:0(R0x020)	Read Mode 2	dddd d000 0ddd 00d0	64 (0x0040)
R34:0(R0x022)	Row Address Mode	0ddd 0ddd 00dd 0ddd	0 (0x0000)
R35:0(R0x023)	Column Address Mode	0000 0ddd 00dd 0ddd	0 (0x0000)
R36:0(R0x024)	Reserved	–	2 (0x0002)
R39:0(R0x027)	Reserved	–	11 (0x000B)
R41:0(R0x029)	Reserved	–	1153 (0x0481)
R42:0(R0x02A)	Reserved	–	4230 (0x1086)
R43:0(R0x02B)	Green1 Gain	0ddd dddd dddd dddd	8 (0x0008)
R44:0(R0x02C)	Blue Gain	0ddd dddd dddd dddd	8 (0x0008)
R45:0(R0x02D)	Red Gain	0ddd dddd dddd dddd	8 (0x0008)
R46:0(R0x02E)	Green2 Gain	0ddd dddd dddd dddd	8 (0x0008)
R48:0(R0x030)	Reserved	–	0 (0x0000)
R50:0(R0x032)	Reserved	–	0 (0x0000)
R53:0(R0x035)	Global Gain	dddd dddd dddd dddd	8 (0x0008)
R60:0(R0x03C)	Reserved	–	4112 (0x1010)
R61:0(R0x03D)	Reserved	–	5 (0x0005)

Table 12. REGISTER LIST AND DEFAULT VALUES (continued)
(1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic)

Register # Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R62:0(R0x03E)	Reserved	–	64 (0x80C7)
R63:0(R0x03F)	Reserved	–	4 (0x0004)
R64:0(R0x040)	Reserved	–	7 (0x0007)
R65:0(R0x041)	Reserved	–	3 (0x0000)
R66:0(R0x042)	Reserved	–	5 (0x0003)
R67:0(R0x043)	Reserved	–	1 (0x0003)
R68:0(R0x044)	Reserved	–	515 (0x0203)
R69:0(R0x045)	Reserved	–	4112 (0x1010)
R70:0(R0x046)	Reserved	–	4112 (0x1010)
R71:0(R0x047)	Reserved	–	4112 (0x1010)
R72:0(R0x048)	Reserved	–	16 (0x0010)
R73:0(R0x049)	Reserved	–	168 (0x00A8)
R74:0(R0x04A)	Reserved	–	16 (0x0010)
R75:0(R0x04B)	Reserved	–	40 (0x0028)
R76:0(R0x04C)	Reserved	–	16 (0x0010)
R77:0(R0x04D)	Reserved	–	8224 (0x2020)
R78:0(R0x04E)	Reserved	–	4112 (0x1010)
R79:0(R0x04F)	Reserved	–	23 (0x0014)
R80:0(R0x050)	Reserved	–	32768 (0x8000)
R81:0(R0x051)	Reserved	–	7 (0x0007)
R82:0(R0x052)	Reserved	–	32768 (0x8000)
R83:0(R0x053)	Reserved	–	7 (0x0007)
R84:0(R0x054)	Reserved	–	8 (0x0008)
R86:0(R0x056)	Reserved	–	32 (0x0020)
R87:0(R0x057)	Reserved	–	4 (0x0004)
R88:0(R0x058)	Reserved	–	32768 (0x8000)
R89:0(R0x059)	Reserved	–	7 (0x0007)
R90:0(R0x05A)	Reserved	–	4 (0x0004)
R91:0(R0x05B)	Reserved	–	1 (0x0001)
R92:0(R0x05C)	Reserved	–	90 (0x005A)
R93:0(R0x05D)	Reserved	–	11539 (0x2D13)
R94:0(R0x05E)	Reserved	–	16895 (0x41FF)
R95:0(R0x05F)	Reserved	–	8989 (0x231D)
R96:0(R0x060)	Reserved	–	32 (0x0020)
R97:0(R0x061)	Reserved	–	32 (0x0020)
R98:0(R0x062)	Reserved	–	0 (0x0000)
R99:0(R0x063)	Reserved	–	32 (0x0020)
R100:0(R0x064)	Reserved	–	32 (0x0020)
R101:0(R0x065)	Reserved	–	0 (0x0000)
R104:0(R0x068)	Reserved	–	0 (0x0000)
R105:0(R0x069)	Reserved	–	0 (0x0000)

Table 12. REGISTER LIST AND DEFAULT VALUES (continued)
(1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic)

Register # Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R106:0(R0x06A)	Reserved	–	0 (0x0000)
R107:0(R0x06B)	Reserved	–	0 (0x0000)
R108:0(R0x06C)	Reserved	–	0 (0x0000)
R109:0(R0x06D)	Reserved	–	0 (0x0000)
R112:0(R0x070)	Reserved	–	103 (0x00AC)
R113:0(R0x071)	Reserved	–	25604 (0xA700)
R114:0(R0x072)	Reserved	–	25094 (0xA700)
R115:0(R0x073)	Reserved	–	5128 (0x0C00)
R116:0(R0x074)	Reserved	–	5642 (0x0600)
R117:0(R0x075)	Reserved	–	13068 (0x5 617)
R118:0(R0x076)	Reserved	–	18229 (0x6B57)
R119:0(R0x077)	Reserved	–	18743 (0x6B57)
R120:0(R0x078)	Reserved	–	24633 (0xA500)
R121:0(R0x079)	Reserved	–	26114 (0xAB00)
R122:0(R0x07A)	Reserved	–	25604 (0xA904)
R123:0(R0x07B)	Reserved	–	25094 (0xA700)
R124:0(R0x07C)	Reserved	–	25094 (0xA700)
R125:0(R0x07D)	Reserved	–	65280 (0xFF00)
R126:0(R0x07E)	Reserved	–	25608 (0xA900)
R127:0(R0x07F)	Reserved	–	25604 (0x6404)
R128:0(R0x080)	Reserved	–	34 (0x0022)
R129:0(R0x081)	Reserved	–	7940 (0x1F04)
R130:0(R0x082)	Reserved	–	0 (0x0000)
R131:0(R0x083)	Reserved	–	6918 (0x1B06)
R132:0(R0x084)	Reserved	–	7432 (0x1D08)
R134:0(R0x086)	Reserved	–	6150 (0x1806)
R135:0(R0x087)	Reserved	–	6664 (0x1A08)
R144:0(R0x090)	Reserved	–	2000 (0x07D0)
R145:0(R0x091)	Reserved	–	0 (0x0000)
R146:0(R0x092)	Reserved	–	1 (0x0001)
R147:0(R0x093)	Reserved	–	0 (0x0000)
R149:0(R0x095)	Reserved	–	0 (0x0000)
R150:0(R0x096)	Reserved	–	0 (0x0000)
R151:0(R0x097)	Reserved	–	0 (0x0000)
R152:0(R0x098)	Reserved	–	0 (0x0000)
R153:0(R0x099)	Reserved	–	0 (0x0000)
R154:0(R0x09A)	Reserved	–	0 (0x0000)
R155:0(R0x09B)	Reserved	–	0 (0x0000)
R156:0(R0x09C)	Reserved	–	0 (0x0000)
R160:0(R0x0A0)	Test_Pattern_Control	–	0 (0x0000)
R161:0(R0x0A1)	Test_Pattern_Green	–	0 (0x0000)

Table 12. REGISTER LIST AND DEFAULT VALUES (continued)
(1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic)

Register # Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R162:0(R0x0A2)	Test_Pattern_Red	–	0 (0x0000)
R163:0(R0x0A3)	Test_Pattern_Blue	–	0 (0x0000)
R164:0(R0x0A4)	Test_Pattern_Bar_Width	–	0 (0x0000)
R165:0(R0x0A5)	Reserved	–	0 (0x0000)
R166:0(R0x0A6)	Reserved	–	0 (0x0000)
R167:0(R0x0A7)	Reserved	–	0 (0x0000)
R168:0(R0x0A8)	Reserved	–	0 (0x0000)
R169:0(R0x0A9)	Reserved	–	0 (0x0000)
R170:0(R0x0AA)	Reserved	–	0 (0x0000)
R171:0(R0x0AB)	Reserved	–	0 (0x0000)
R172:0(R0x0AC)	Reserved	–	0 (0x0000)
R173:0(R0x0AD)	Reserved	–	0 (0x0000)
R174:0(R0x0AE)	Reserved	–	32 (0x0020)
R175:0(R0x0AF)	Reserved	–	0 (0x0000)
R176:0(R0x0B0)	Reserved	–	0 (0x0000)
R177:0(R0x0B1)	Reserved	–	0 (0x0000)
R178:0(R0x0B2)	Reserved	–	0 (0x0000)
R179:0(R0x0B3)	Reserved	–	0 (0x0000)
R180:0(R0x0B4)	Reserved	–	0 (0x0000)
R181:0(R0x0B5)	Reserved	–	0 (0x0000)
R182:0(R0x0B6)	Reserved	–	0 (0x0000)
R183:0(R0x0B7)	Reserved	–	0 (0x0000)
R184:0(R0x0B8)	Reserved	–	0 (0x0000)
R185:0(R0x0B9)	Reserved	–	0 (0x0000)
R186:0(R0x0BA)	Reserved	–	0 (0x0000)
R187:0(R0x0BB)	Reserved	–	0 (0x0000)
R188:0(R0x0BC)	Reserved	–	0 (0x0000)
R189:0(R0x0BD)	Reserved	–	0 (0x0000)
R190:0(R0x0BE)	Reserved	–	0 (0x0000)
R191:0(R0x0BF)	Reserved	–	0 (0x0000)
R192:0(R0x0C0)	Reserved	–	0 (0x0000)
R193:0(R0x0C1)	Reserved	–	0 (0x0000)
R194:0(R0x0C2)	Reserved	–	0 (0x0000)
R195:0(R0x0C3)	Reserved	–	0 (0x0000)
R196:0(R0x0C4)	Reserved	–	0 (0x0000)
R197:0(R0x0C5)	Reserved	–	0 (0x0000)
R198:0(R0x0C6)	Reserved	–	0 (0x0000)
R199:0(R0x0C7)	Reserved	–	0 (0x0000)
R200:0(R0x0C8)	Reserved	–	0 (0x0000)
R201:0(R0x0C9)	Reserved	–	0 (0x0000)
R202:0(R0x0CA)	Reserved	–	0 (0x0000)

Table 12. REGISTER LIST AND DEFAULT VALUES (continued)
(1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic)

Register # Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R203:0(R0x0CB)	Reserved	–	0 (0x0000)
R204:0(R0x0CC)	Reserved	–	0 (0x0000)
R205:0(R0x0CD)	Reserved	–	0 (0x0000)
R206:0(R0x0CE)	Reserved	–	0 (0x0000)
R207:0(R0x0CF)	Reserved	–	0 (0x0000)
R208:0(R0x0D0)	Reserved	–	0 (0x0000)
R209:0(R0x0D1)	Reserved	–	0 (0x0000)
R210:0(R0x0D2)	Reserved	–	0 (0x0000)
R211:0(R0x0D3)	Reserved	–	0 (0x0000)
R212:0(R0x0D4)	Reserved	–	0 (0x0000)
R213:0(R0x0D5)	Reserved	–	0 (0x0000)
R214:0(R0x0D6)	Reserved	–	0 (0x0000)
R215:0(R0x0D7)	Reserved	–	0 (0x0000)
R216:0(R0x0D8)	Reserved	–	0 (0x0000)
R217:0(R0x0D9)	Reserved	–	0 (0x0000)
R218:0(R0x0DA)	Reserved	–	0 (0x0000)
R219:0(R0x0DB)	Reserved	–	0 (0x0000)
R220:0(R0x0DC)	Reserved	–	0 (0x0000)
R221:0(R0x0DD)	Reserved	–	0 (0x0000)
R222:0(R0x0DE)	Reserved	–	0 (0x0000)
R223:0(R0x0DF)	Reserved	–	0 (0x0000)
R224:0(R0x0E0)	Reserved	–	0 (0x0000)
R225:0(R0x0E1)	Reserved	–	0 (0x0000)
R226:0(R0x0E2)	Reserved	–	0 (0x0000)
R227:0(R0x0E3)	Reserved	–	0 (0x0000)
R228:0(R0x0E4)	Reserved	–	0 (0x0000)
R229:0(R0x0E5)	Reserved	–	0 (0x0000)
R230:0(R0x0E6)	Reserved	–	0 (0x0000)
R231:0(R0x0E7)	Reserved	–	0 (0x0000)
R232:0(R0x0E8)	Reserved	–	0 (0x0000)
R233:0(R0x0E9)	Reserved	–	0 (0x0000)
R234:0(R0x0EA)	Reserved	–	0 (0x0000)
R235:0(R0x0EB)	Reserved	–	0 (0x0000)
R236:0(R0x0EC)	Reserved	–	0 (0x0000)
R237:0(R0x0ED)	Reserved	–	0 (0x0000)
R238:0(R0x0EE)	Reserved	–	0 (0x0000)
R239:0(R0x0EF)	Reserved	–	0 (0x0000)
R240:0(R0x0F0)	Reserved	–	0 (0x0000)
R241:0(R0x0F1)	Reserved	–	0 (0x0000)
R248:0(R0x0F8)	Reserved	–	0 (0x0000)
R250:0(R0x0FA)	Reserved	–	0 (0x0000)

Table 12. REGISTER LIST AND DEFAULT VALUES (continued)
(1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic)

Register # Dec (Hex)	Register Description	Data Format (Binary)	Default Value Dec (Hex)
R251:0(R0x0FB)	Reserved	–	0 (0x0000)
R252:0(R0x0FC)	Reserved	–	0 (0x0000)
R253:0(R0x0FD)	Reserved	–	0 (0x0000)
R255:0(R0x0FF)	Chip_Version_Alt	???? ???? ???? ????	6145 (0x1801)

Register Description

Table 13 lists sensor register descriptions.

Table 13. REGISTER DESCRIPTION

Reg. #	Bits	Default	Name
R0:0 R0x000	**15:0**	**0x1801**	**Chip Version (RO)**
	15:8	RO	Part ID Two−digit BCD value typically derived from the reticle ID code Legal values: [0, 255]
	7:4	RO	Analog Revision Constant value incremented with each mask change for the same Part ID Legal values: [0, 15]
	3:0	RO	Digital Revision Constant value incremented with each digital functionality change for the same Part ID Legal values: [0, 15]
	Chip version		
R1:0 R0x001	**15:0**	**0x0036**	**Row Start (RW)**
	The Y coordinate of the upper−left corner of the FOV. If this register is set to an odd value, the next lower even value will be used. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 2004], even		
R2:0 R0x002	**15:0**	**0x0010**	**Column Start (RW)**
	The X coordinate of the upper−left corner of the FOV. The value will be rounded down to the nearest multiple of 2 times the column bin factor. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Legal values: [0, 2750], even Note: Set Column_Start such that it is in the form shown below, where n is an integer: Mirror_Column = 0 Mirror_Column = 1 no bin 4n 4n + 2 Bin 2x 8n 8n + 4 Bin 4x 16n 16n + 8		
R3:0 R0x003	**15:0**	**0x0797**	**Row Size (RW)**
	The height of the FOV minus one. If this register is set to an even value, the next higher odd value will be used. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes Causes a Bad Frame if written. Legal values: [1, 2005], odd		
R4:0 R0x004	**15:0**	**0x0A1F**	**Column Size (RW)**
	The width of the field of view minus one. If this register is set to an even value, the next higher odd value will be used. In other words, it should be $(2 \times n \times (Column\_Bin + 1) - 1)$ for some integer n. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written Legal values: [1, 2751], odd		
R5:0 R0x005	**15:0**	**0x0000**	**Horizontal Blank (RW)**
	Extra time added to the end of each row, in pixel clocks. Incrementing this register will increase exposure and decrease frame rate. Setting a value less than the minimum will use the minumum horizontal blank. The minimum horizontal blank depends on the mode of the sensor. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 4095]		

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R6:0 R0x006	**15:0**	**0x0019**	**Vertical Blank (RW)**
	Extra time added to the end of each frame in rows minus one. Incrementing this register will decrease frame rate, but not affect exposure. Setting a value less than the minimum will use the minimum vertical blank. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Legal values: [8, 2047]		
R7:0 R0x007	**15:0**	**0x1F82**	**Output Control (RW)**
	15	X	Reserved
	14	0x0000	Reserved
	13	X	Reserved
	12:10	0x0007	Output_Slew_Rate Controls the slew rate on digital output pads except for PIXCLK. Higher values imply faster transition times. Legal values: [0, 7]
	9:7	0x0007	PIXCLK_Slew_Rate Controls the slew rate on the PIXCLK pad. Higher values imply faster transition times Legal values: [0, 7]
	6	0x0000	Reserved
	5:4	X	Reserved
	3	0x0000	Reserved
	2	0x0000	FIFO_Parallel_Data When set, pixels will be sent through the output FIFO before being sent off chip. This allows the output port to be running at a slower speed than f_PIXCLK, because the FIFO allows for pixels to be output during horizontal blank. Use of this mode requires the PLL to be set up properly
	1	0x0001	Chip Enable When clear, sensor readout is stopped and analog circuitry is put in a state which draws minimal power. When set, the chip operates according to the current mode. Writing this bit does not affect the values of any other registers
	0	0x0000	Synchronize Changes When set, changes to certain registers (those with the SC attribute) are delayed until the bit is clear. When cleared, all the delayed writes will happen immediately. Registers with the F attribute will still have the update synchronized to the next frame boundary
R8:0 R0x008	**15:0**	**0x0000**	**Shutter Width Upper (RW)**
	The most significant bits of the shutter width, which are combined with Shutter Width Lower (R9)		
R9:0 R0x009	**15:0**	**0x0797**	**Shutter Width Lower (RW)**
	The least significant bits of the shutter width. This is combined with Shutter_Width_Upper and Shutter_Delay for the effective shutter width. If set to zero, a value of “1” will be used		
R10:0 R0x00A	**15:0**	**0x0000**	**Pixel Clock Control (RW)**
	15	0x0000	Invert Pixel Clock When set, LV, FV, and D_OUT should be captured on the rising edge of PIXCLK. When clear, they should be captured on the falling edge. This is accomplished by inverting the PIXCLK output NOTE: This field is not reset by the soft Reset (R13)
	14:11	X	Reserved
	10:8	0x0000	Shift Pixel Clock Two’s complement value representing how far to shift the PIXCLK output pin relative to DOUT, in EXTCLK cycles. Positive values shift PIXCLK later in time relative to DOUT (and thus relative to the internal array/datapath clock). No effect unless PIXCLK is divided by Divide Pixel Clock NOTE: This field is not reset by the soft Reset (R13) Legal values: [−2, 2]
	7	X	Reserved

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R10:0 R0x00A	6:0	0x0000	Divide Pixel Clock Produces a PIXCLK that is divided by the value times two. The value must be zero or a power of 2. This will slow down the internal clock in the array control and datapath blocks, including pixel readout. It will not affect the two−wire serial interface clock. A value of "0" corresponds to a PIXCLK with the same frequency as EXTCLK. A value of 1 means f_PIXCLK = (f_EXTCLK / 2); 2 means f_PIXCLK = (f_EXTCLK / 4); 64 means f_PIXCLK = (f_EXTCLK / 128); and so on NOTE: This field is not reset by the soft Reset (R13). This field should not be written while in streaming mode. Instead, Pause_Restart should be used to suspend output while the divider is being changed. Legal values: [0, 1, 2, 4, 8, 16, 32, 64]
R11:0 R0x00B	**15:0**	**0x0000**	**Restart (RW)**
	15:3	X	Reserved
	2	0x0000	Trigger Setting this bit in Snapshot mode will cause the next trigger to occur as if the TRIGGER pin were properly asserted/negated. Ineffective if not in Snapshot mode. The sense of this bit is NOT affected by Invert Trigger. When using this bit instead of the TRIGGER pin, make sure that either the trigger pin is continuously asserted, or that the pad is continuously negated and Invert_Trigger is set
	1	0x0000	Pause Restart When set, Restart will not automatically be cleared. Instead, the sensor will pause at row 0 after Restart is set. When Pause_Restart is cleared, the sensor will resume. This allows for a repeatable delay from clearing restart to FV. When clearing this bit, be sure not to clear Restart as well: it will be cleared automatically when the device has restarted
	0	0x0000	Restart Setting this bit will cause the sensor to abandon the current frame and restart from the first row. It will take up to 2 × t_ROW for the restart to take effect. This bit resets to 0 automatically unless Pause_Restart is set. Manually setting this bit to zero will cause undefined behavior Volatile
R12:0 R0x00C	**15:0**	**0x0000**	**Shutter Delay (RW)**
	A negative adjustment to the effective shutter width in ACLKs. See Shutter_Width_Lower. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Legal values: [0, 8191]		
R13:0 R0x00D	**15:0**	**0x0000**	**Reset (RW)**
	Setting this bit will put the sensor into reset mode, which will set the sensor to its default power−up state and cause it to halt. Clearing this bit will resume normal operation. This is equivalent to pulling RESET_BAR LOW, except that the two−wire serial interface remains functional		
R16:0 R0x010	**15:0**	**0x0050**	**PLL Control (RW)**
	15	0x0000	Reserved
	14:13	0x0000	Reserved
	12:9	X	Reserved
	8	0x0000	Reserved
	7:4	0x0005	Reserved
	3:2	X	Reserved
	1	0x0000	Use PLL When set, use the PLL output as the system clock. When clear, use EXTCLK as the system clock
	0	0x0000	Power PLL When set, the PLL is powered. When clear, it is not powered

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R17:0 R0x011	**15:0**	**0x6404**	**PLL Config 1 (RW)**
	15:8	0x0064	PLL m Factor PLL output frequency multiplier Legal values: [16, 255]
	7:6	X	Reserved
	5:0	0x0004	PLL n Divider PLL output frequency divider minus 1 Legal values: [0, 63]
R18:0 R0x012	**15:0**	**0x0000**	**PLL Config 2 (RW)**
	15:13	X	Reserved
	12:8	0x0000	Reserved
	7:5	X	Reserved
	4:0	0x0000	PLL p1 Divider PLL system clock divider minus 1. Use odd numbers. If this is set to an even number, the system clock duty cycle will not be 50:50. In this case, set all bits in R101 or slow down EXTCLK Legal values: [0, 127]
R30:0 R0x01E	**15:0**	**0x4006**	**Read Mode 1 (RW)**
	15	X	Reserved
	14	0x0001	Reserved
	13	0x0000	Reserved
	12	0x0000	Reserved
	11	0x0000	XOR Line Valid When set, produce a LV signal that is the XOR of FV and the normal line_valid. Ineffective if Continuous Line Valid is set. When clear, produce a normal LV
	10	0x0000	Continuous Line Valid When set, produce the LV signal even during the vertical blank period. When clear, produce LV only when active rows are being read out (that is, only when FV is high). Ineffective if FIFO_Parallel_Data is set
	9	0x0000	Invert Trigger When set, the sense of the TRIGGER input pin will be inverted
	8	0x0000	Snapshot When set, the sensor enters snapshot mode, and will wait for a trigger event between frames. When clear, the sensor is in continuous mode. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	7	0x0000	Global Reset When set, the Global Reset Release shutter will be used. When clear, the Electronic Rolling Shutter will be used. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	6	0x0000	Bulb Exposure When set, exposure time will be controlled by an external trigger. When clear, exposure time will be controlled by the Shutter_Width_Lower and Shutter_Width_Upper registers. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	5	0x0000	Invert Strobe When set, the STROBE signal will be active LOW (during exposure). When clear, the STROBE signal is active HIGH
	4	0x0000	Strobe Enable When set, a strobe signal will be generated by the digital logic during integration. When clear, the strobe pin will be set to the value of Invert_Strobe

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R30:0 R0x01E	3:2	0x0001	Strobe Start Determines the timepoint when the strobe is asserted. 0 – first trigger 1 – start of simultaneous exposure 2 – shutter width 3 – second trigger Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	1:0	0x0002	Strobe End Determines the timepoint when the strobe is negated. If this is set equal to or less than Strobe_Start, the width of the strobe pulse will be t_ROW. See Strobe_Start. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
R32:0 R0x020	**15:0**	**0x0040**	**Read Mode 2 (RW)**
	15	0x0000	Mirror Row When set, row readout in the active image occurs in reverse numerical order starting from (Row_Start + Row_Size). When clear, row readout of the active image occurs in numerical order. This has no effect on the readout of the dark rows. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written
	14	0x0000	Mirror Column When set, column readout in the active image occurs in reverse numerical order, starting from (Column_Start + Column_Size). When clear, column readout of the active image occurs in numerical order. This has no effect on the readout of the dark columns. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	13	0x0000	Reserved
	12	0x0000	Show Dark Columns When set, the dark columns will be output to the left of the active image, making the output image wider. This has no effect on integration time or frame rate. When clear, only columns that are part of the active image will be output. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	11	0x0000	Show Dark Rows When set, the dark rows will be output before the active image rows, making the output image taller. This has no effect on integration time or frame rate. When clear, only rows from the active image will be output. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	10:7	X	Reserved
	6	0x0001	Row BLC When set, digitally compensate for differing black levels between rows by adding Dark Target (R73) and subtracting the average value of the 8 same−color dark pixels at the beginning of the row. When clear, digitally add Row Black Default Offset (R75) to the value of each pixel
	5	0x0000	Column Sum When set, column summing will be enabled, and in column bin modes, all sampled capacitors will be enabled for column readout, resulting in an effective gain equal to the column bin factor. When clear, column averaging will be done, and there will be no additional gain related to the column bin factor Writes are synchronized to frame boundaries. Affected by Synchronize_Changes
	4	0x0000	Reserved
	3:0	X	Reserved
R34:0 R0x022	**15:0**	**0x0000**	**Row Address Mode (RW)**
	15	X	Reserved
	14:12	0x0000	Reserved
	11	X	Reserved
	10:8	0x0000	Reserved
	7:6	X	Reserved

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R34:0 R0x022	5:4	0x0000	Row Bin The number of rows to be read and averaged per row output minus one. The rows will be read independently into sampling capacitors, then averaged together before column readout. For normal readout, this should be 0. For Bin 2X, it should be 1; for Bin 4X, it should be 3. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 3]
	3	X	Reserved
	2:0	0x0000	Row Skip The number of row−pairs to skip for every row−pair output. A value of zero means to read every row. For Skip 2X, this should be 1; for Skip 3X, it should be 2, and so on. This value should be no less than Row_Bin. For full binning, Row_Skip should equal Row_Bin Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 7]
R35:0 R0x023	**15:0**	**0x0000**	**Column Address Mode (RW)**
	15:11	X	Reserved
	10:8	0x0000	Reserved
	7:6	X	Reserved
	5:4	0x0000	Column Bin The number of columns to be read and averaged per column output minus one. For normal readout, this should be zero. For Bin 2X, it shoud be 1; for Bin 4X, it should be 3. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: {0, 1, 3}
	3	X	Reserved
	2:0	0x0000	Column Skip The number of column−pairs to skip for every column−pair output. A value of zero means to read every column in the active image. For Skip 2X, this should be 1; for Skip 3X, this should be 2, and so on. This value should be no less than Column_Bin. For full binning, Column_Skip should equal Column_Bin. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Causes a Bad Frame if written. Legal values: [0, 6]
R43:0 R0x02B	**15:0**	**0x0008**	**Green1 Gain (RW)**
	15	X	Reserved
	14:8	0x0000	Green1 Digital Gain Digital Gain for the Green1 channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile Legal values: [0, 120]
	7	X	Reserved
	6	0x0000	Green1 Analog Multiplier Analog gain multiplier for the Green1 channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile
	5:0	0x0008	Green1 Analogl Gain Analog gain setting for the Green1 channel times 8. The effective gain for the channel is (((Green1_Digital_Gain/8) + 1) × (Green1_Analog_Multiplier + 1) × (Green1_Analog_Gain/8)). Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]
R44:0 R0x02C	**15:0**	**0x0008**	**Blue Gain (RW)**
	15	X	Reserved
	14:8	0x0000	Blue Digital Gain Digital Gain for the Blue channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [0, 120]

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R44:0 R0x02C	7	X	Reserved
	6	0x0000	Blue Analog Multiplier Analog gain multiplier for the Blue channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile
	5:0	0x0008	Blue Analog Gain Analog gain setting for the Blue channel times 8. The effective gain for the channel is (((Blue_Digital_Gain/8) + 1) × (Blue_Analog_Multiplier + 1) × (Blue_Analog_Gain/8)). Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile Legal values: [8, 63]
R45:0 R0x02D	**15:0**	**0x0008**	**Red Gain (RW)**
	15	X	Reserved
	14:8	0x0000	Red Digital Gain Digital Gain for the Red channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [0, 120]
	7	X	Reserved
	6	0x0000	Red Analog Multiplier Analog gain multiplier for the Red channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile
	5:0	0x0008	Red Analog Gain Analog gain setting for the Red channel times 8. The effective gain for the channel is (((Red_Digital_Gain/8) + 1) × (Red_Analog_Multiplier + 1) × (Red_Analog_Gain/8)). Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]
R46:0 R0x02E	**15:0**	**0x0008**	**Green2 Gain (RW)**
	15	X	Reserved
	14:8	0x0000	Green2 Digital Gain Digital Gain for the Green2 channel minus 1 times 8. The actual digital gain is (1 + value/8), and can range from 1 (a setting of 0) to 16 (a setting of 120) in increments of 1/8. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile Legal values: [0, 120]
	7	X	Reserved
	6	0x0000	Green2 Analog Multiplier Analog gain multiplier for the Green2 channel minus 1. If 1, an additional analog gain of 2X will be applied. If 0, no additional gain is applied. Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile
	5:0	0x0008	Green2 Analog Gain Analog gain setting for the Green2 channel times 8. The effective gain for the channel is (((Green2_Digital_Gain/8) + 1) × (Green2_Analog_Multiplier + 1) × (Green2_Analog_Gain/8)). Writes are synchronized to frame boundaries. Affected by Synchronize_Changes. Volatile. Legal values: [8, 63]
R53:0 R0x035	**15:0**	**0x0008**	**Global Gain (WO)**
	Writing the Global_Gain sets all four individual gain registers R43−R46 to the value. This register should not be read. See Green1_Gain (R43) for a description of the various fields. Affected by Synchronize_Changes. Duplicate Legal values: special		
R73:0 R0x049	**15:0**	**0x00A8**	**Row Black Target (RW)**
	Reserved		
R75:0 R0x04B	**15:0**	**0x0028**	**Row Black Default Offset (RW)**
	Reserved		

Table 13. REGISTER DESCRIPTION (continued)

Reg. #	Bits	Default	Name
R91:0 R0x05B	**15:0**	**0x0001**	**BLC_Sample_Size (RW)**
	Reserved		
R92:0 R0x05C	**15:0**	**0x005A**	**BLC_Tune_1 (RW)**
	15:12	X	Reserved
	11:8	0x0000	Reserved
	7:0	0x005A	Reserved
R93:0 R0x05D	**15:0**	**0x2D13**	**BLC_Delta_Thresholds (RW)**
	15	X	Reserved
	14:8	0x002D	Reserved
	7	X	Reserved
	6:0	0x0013	Reserved
R94:0 R0x05E	**15:0**	**0x41FF**	**BLC_Tune_2 (RW)**
	15	X	Reserved
	14:12	0x0004	Reserved
	11:9	X	Reserved
	8:0	0x01FF	Reserved
R95:0 R0x05F	**15:0**	**0x231D**	**BLC_Target_Thresholds (RW)**
	15	X	Reserved
	14:8	0x0023	Reserved
	7	X	Reserved
	6:0	0x001D	Reserved
R96:0 R0x060	**15:0**	**0x0020**	**Green1_Offset (RW)**
	Reserved		
R97:0 R0x061	**15:0**	**0x0020**	**Green2_Offset (RW)**
	Reserved		
R98:0 R0x062	**15:0**	**0x0000**	**Black_Level_Calibration (RW)**
	15	0x0000	Reserved
	14	0x0000	Reserved
	13	0x0000	Reserved
	12	0x0000	Reserved
	11	0x0000	Reserved
	10:2	X	Reserved
	1	0x0000	Reserved
	0	0x0000	Reserved
R99:0 R0x063	**15:0**	**0x0020**	**Red_Offset (RW)**
	Reserved		
R100:0 R0x064	**15:0**	**0x0020**	**Blue_Offset (RW)**
	Reserved		