Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

1/3-Inch Wide-VGA CMOS Digital Image Sensor

MT9V022 Datasheet, Rev. L

For the latest datasheet revision, please visit www.onsemi.com

Features

- Array format: Wide-VGA, active 752H x 480V (360,960 pixels)
- Global shutter photodiode pixels; simultaneous integration and readout
- Monochrome or color: Near_IR enhanced performance for use with non-visible NIR illumination
- Readout modes: progressive or interlaced
- Shutter efficiency: >99%
- Simple two-wire serial interface
- Register Lock capability
- Window Size: User programmable to any smaller format (QVGA, CIF, QCIF, etc.). Data rate can be maintained independent of window size
- Binning: 2 x 2 and 4 x 4 of the full resolution
- ADC: On-chip, 10-bit column-parallel (option to operate in 12-bit to 10-bit companding mode)
- Automatic Controls: Auto exposure control (AEC) and auto gain control (AGC); variable regional and variable weight AEC/AGC
- Support for four unique serial control register IDs to control multiple imagers on the same bus
- Data output formats:
  - Single sensor mode:
    10-bit parallel/stand-alone
    8-bit or 10-bit serial LVDS
  - Stereo sensor mode:
    Interspersed 8-bit serial LVDS

Table 1: Key Performance Parameters

Parameter	Value
Optical format	1/3-inch
Active imager size	4.51 mm (H) x 2.88 mm (V) 5.35 mm diagonal
Active pixels	752H x 480V
Pixel size	6.0 µm x 6.0 µm
Color filter array	Monochrome or color RGB Bayer pattern
Shutter type	Global shutter
Maximum data rate/ master clock	26.6 MPS/26.6 MHz
Full resolution	752 x 480
Frame rate	60 fps (at full resolution)
ADC resolution	10-bit column-parallel
Responsivity	4.8 V/lux-sec (550nm)
Dynamic range	>55 dB linear; >80 dB—100 dB in HDR mode
Supply voltage	3.3 V ±0.3 V (all supplies)
Power consumption	<320 mW at maximum data rate; 100 µW standby power
Operating temperature	-40°C to +85°C
Packaging	52-Ball IBGA, automotive-qualified; wafer or die

Applications

- Automotive
- Unattended surveillance
- Stereo vision
- Security
- Smart vision
- Automation
- Video as input
- Machine vision

Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
MT9V022IA7ATC-DP	RGB, 0deg CRA, iBGA Package	Drypack, Protective Film
MT9V022IA7ATC-DR	RGB, 0deg CRA, iBGA Package	Drypack
MT9V022IA7ATM-DP	Mono, 0deg CRA, iBGA Package	Drypack, Protective Film
MT9V022IA7ATM-DR	Mono, 0deg CRA, iBGA Package	Drypack
MT9V022IA7ATM-TP	Mono, 0deg CRA, iBGA Package	Tape & Reel, Protective Film
MT9V022IA7ATM-TR	Mono, 0deg CRA, iBGA Package	Tape & Reel

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

Table of Contents

List of Figures

List of Tables

General Description

The ON Semiconductor MT9V022 is a 1/3-inch wide-VGA format CMOS active-pixel digital image sensor with global shutter and high dynamic range (HDR) operation. The sensor has specifically been designed to support the demanding interior and exterior automotive imaging needs, which makes this part ideal for a wide variety of imaging applications in real-world environments.

This wide-VGA CMOS image sensor features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The active imaging pixel array is 752H x 480V. It incorporates sophisticated camera functions on-chip—such as binning 2 x 2 and 4 x 4, to improve sensitivity when operating in smaller resolutions—as well as windowing, column and row mirroring. It is programmable through a simple two-wire serial interface.

The MT9V022 can be operated in its default mode or be programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide-VGA-size image at 60 frames per second (fps).

An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. A 12-bit resolution companded for 10 bits for small signals can be alternatively enabled, allowing more accurate digitization for darker areas in the image.

In addition to a traditional, parallel logic output the MT9V022 also features a serial low-voltage differential signaling (LVDS) output. The sensor can be operated in a stereo-camera, and the sensor, designated as a stereo-master, is able to merge the data from itself and the stereo-slave sensor into one serial LVDS stream.

The sensor is designed to operate in a wide temperature range (–40°C to +85°C).

Figure 1: Block Diagram

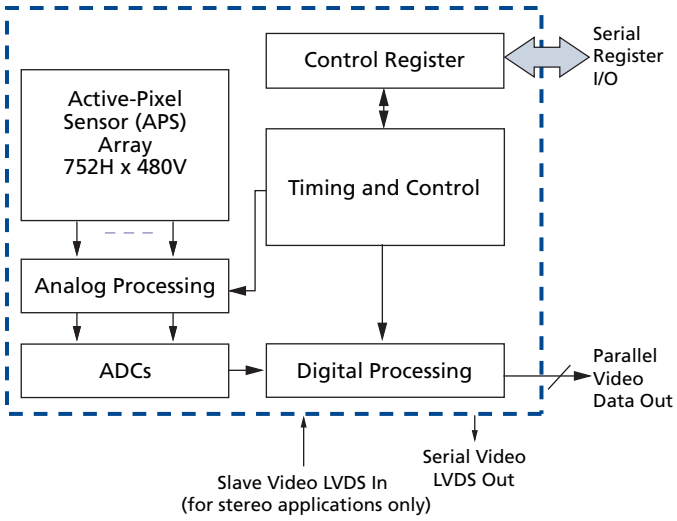
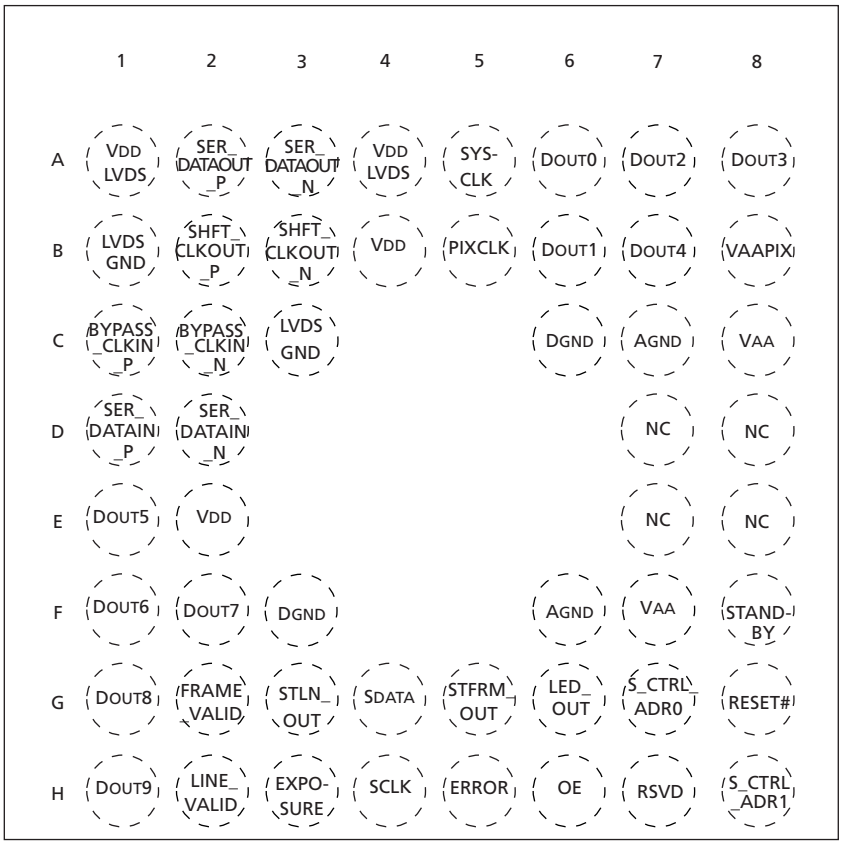


Figure 2: 52-Ball IBGA Package



Top View
(Ball Down)

Ball Descriptions

Table 1: Ball Descriptions
Only pins DOUT0 through DOUT9 may be tri-stated.

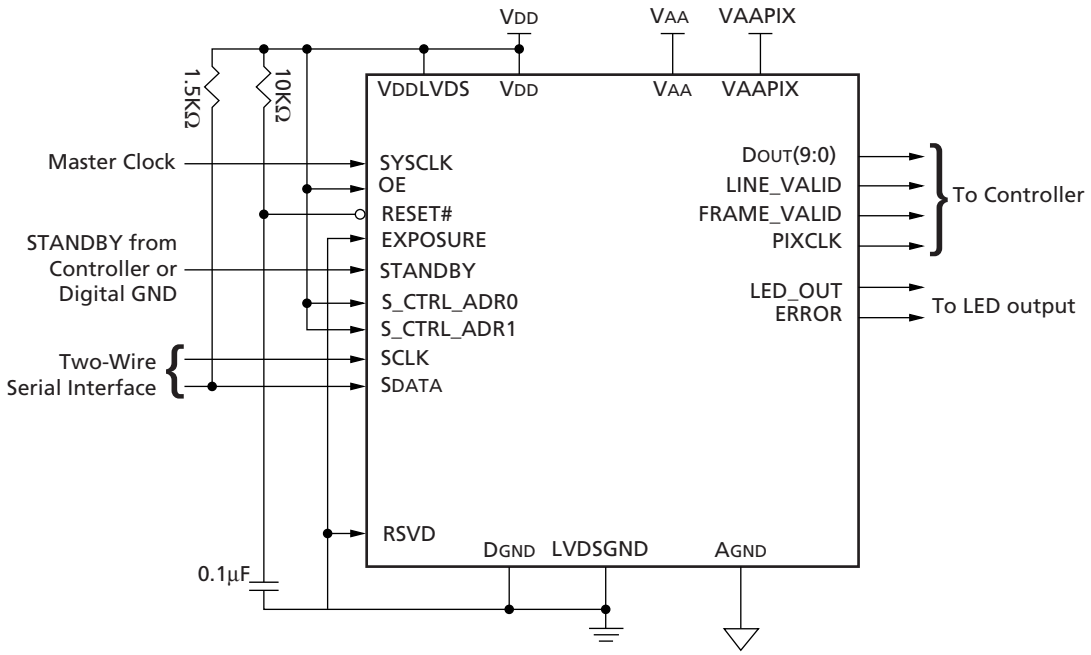
52-Ball IBGA Numbers	Symbol	Type	Description	Note
H7	RSVD	Input	Connect to DGND.	1
D2	SER_DATAIN_N	Input	Serial data in for stereoscopy (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
D1	SER_DATAIN_P	Input	Serial data in for stereoscopy (differential positive). Tie to DGND in non-stereoscopy mode.	
C2	BYPASS_CLKIN_N	Input	Input bypass shift-CLK (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
C1	BYPASS_CLKIN_P	Input	Input bypass shift-CLK (differential positive). Tie to DGND in non-stereoscopy mode.	
H3	EXPOSURE	Input	Rising edge starts exposure in slave mode.	
H4	SCLK	Input	Two-wire serial interface clock. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
H6	OE	Input	DOUT enable pad, active HIGH.	2
G7	S_CTRL_ADR0	Input	Two-wire serial interface slave address bit 3.	
H8	S_CTRL_ADR1	Input	Two-wire serial interface slave address bit 5.	
G8	RESET#	Input	Asynchronous reset. All registers assume defaults.	
F8	STANDBY	Input	Shut down sensor operation for power saving.	
A5	SYSCLK	Input	Master clock (26.6 MHz).	
G4	SDATA	I/O	Two-wire serial interface data. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
G3	STLN_OUT	I/O	Output in master mode—start line sync to drive slave chip in-phase; input in slave mode.	
G5	STFRM_OUT	I/O	Output in master mode—start frame sync to drive a slave chip in-phase; input in slave mode.	
H2	LINE_VALID	Output	Asserted when DOUT data is valid.	
G2	FRAME_VALID	Output	Asserted when DOUT data is valid.	
E1	DOUT5	Output	Parallel pixel data output 5.	
F1	DOUT6	Output	Parallel pixel data output 6.	
F2	DOUT7	Output	Parallel pixel data output 7.	
G1	DOUT8	Output	Parallel pixel data output 8	
H1	DOUT9	Output	Parallel pixel data output 9.	
H5	ERROR	Output	Error detected. Directly connected to STEREO ERROR FLAG.	
G6	LED_OUT	Output	LED strobe output.	
B7	DOUT4	Output	Parallel pixel data output 4.	
A8	DOUT3	Output	Parallel pixel data output 3.	
A7	DOUT2	Output	Parallel pixel data output 2.	
B6	DOUT1	Output	Parallel pixel data output 1.	
A6	DOUT0	Output	Parallel pixel data output 0.	
B5	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.	

Table 1: Ball Descriptions (continued)
Only pins DOUT0 through DOUT9 may be tri-stated.

52-Ball IBGA Numbers	Symbol	Type	Description	Note
B3	SHFT_CLKOUT_N	Output	Output shift CLK (differential negative).	
B2	SHFT_CLKOUT_P	Output	Output shift CLK (differential positive).	
A3	SER_DATAOUT_N	Output	Serial data out (differential negative).	
A2	SER_DATAOUT_P	Output	Serial data out (differential positive).	
B4, E2	VDD	Supply	Digital power 3.3V.	
C8, F7	VAA	Supply	Analog power 3.3V.	
B8	VAAPIX	Supply	Pixel power 3.3V.	
A1, A4	VDDLVDS	Supply	Dedicated power for LVDS pads.	
B1, C3	LVDSGND	Ground	Dedicated GND for LVDS pads.	
C6, F3	DGND	Ground	Digital GND.	
C7, F6	AGND	Ground	Analog GND.	
E7, E8, D7, D8	NC	NC	No connect.	3

Notes:
1. Pin H7 (RSVD) must be tied to GND.
2. Output Enable (OE) tri-states signals DOUT0–DOUT9. No other signals are tri-stated with OE.
3. No connect. These pins must be left floating for proper operation.

Figure 3: Typical Configuration (Connection)—Parallel Output Mode



Note: LVDS signals are to be left floating.

Pixel Data Format

Pixel Array Structure

The MT9V022 pixel array is configured as 782 columns by 492 rows, shown in Figure 4. The left 26 columns and the top eight rows of pixels are optically black and can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment. However, the middle four black rows can also be read out by setting the sensor to raw data output mode. There are 753 columns by 481 rows of optically active pixels. The active area is surrounded with optically transparent dummy columns and rows to improve image uniformity within the active area. One additional active column and active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel.

Figure 4: Pixel Array Description

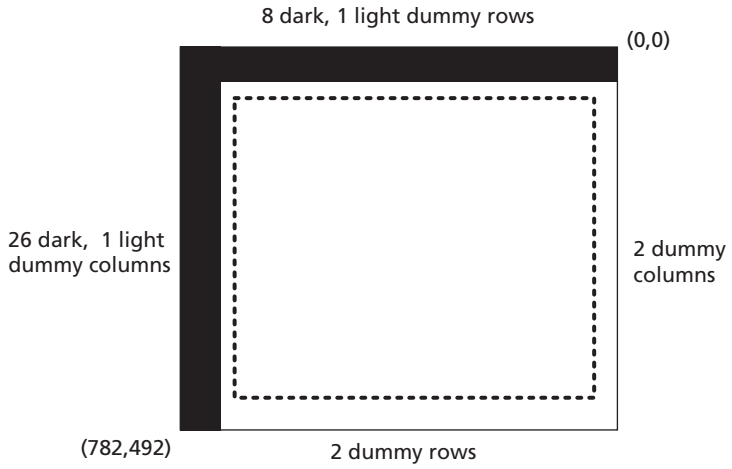
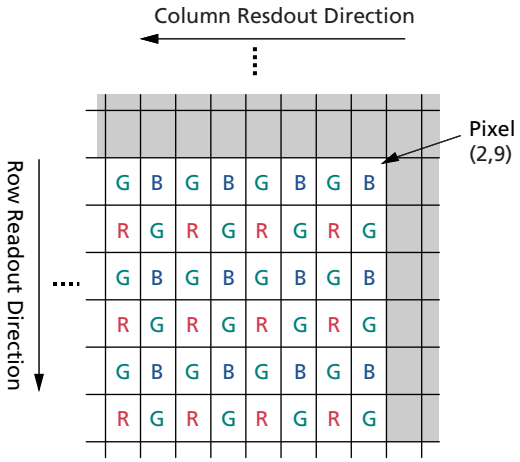


Figure 5: Pixel Color Pattern Detail (Top Right Corner)



Color Device Limitations

The color version of the MT9V022 does not support or offers reduced performance for the following functionalities.

Pixel Binning

Pixel binning is done on immediate neighbor pixels only, no facility is provided to skip pixels according to a Bayer pattern. Therefore, the result of binning combines pixels of different colors. For more information, see “Pixel Binning” on page 34.

Interlaced Readout

Interlaced readout yields one field consisting only of red and green pixels and another consisting only of blue and green pixels. This is due to the Bayer pattern of the CFA.

Automatic Black Level Calibration

When the color bit is set (R0x0F[2]=1), the sensor uses GREEN1 pixels black level correction value, which is applied to all colors. To use calibration value based on all dark pixels offset values, the color bit should be cleared.

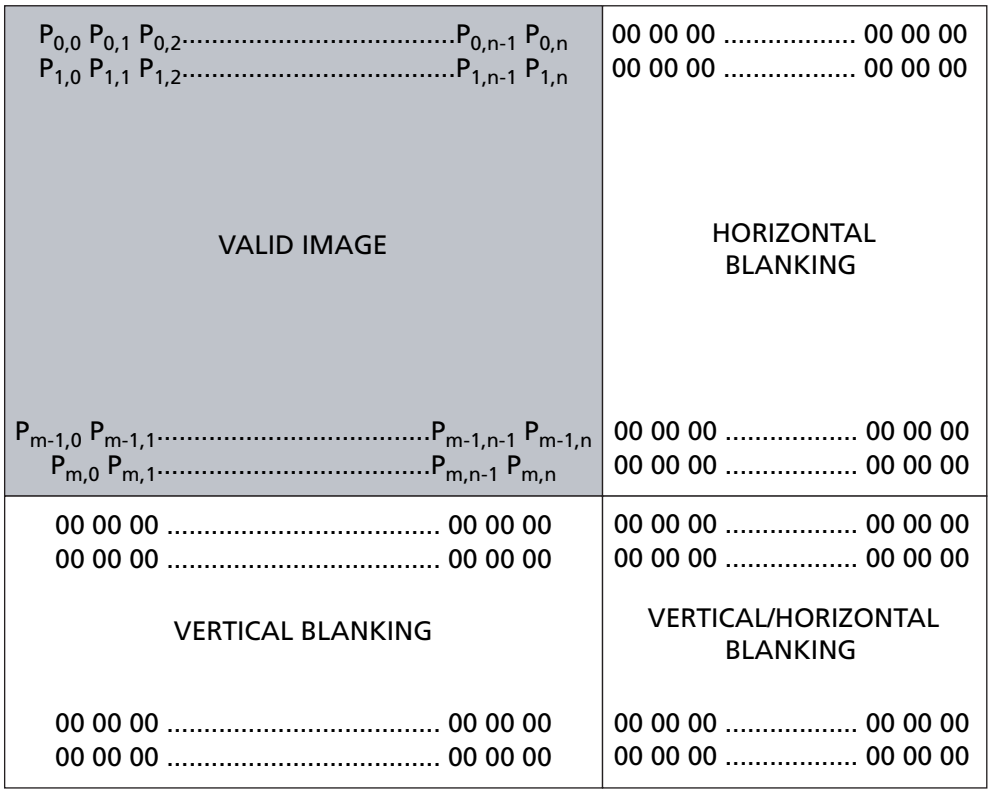
Other Limiting Factors

Black level correction and row-wise noise correction are applied uniformly to each color. Automatic exposure and gain control calculations are made based on all three colors, not just the green luma channel. High dynamic range does operate; however, ON Semiconductor strongly recommends limiting use to linear operation if good color fidelity is required.

Output Data Format

The MT9V022 image data can be read out in a progressive scan or interlaced scan mode. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 6. The amount of horizontal and vertical blanking is programmable through R0x05 and R0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See “Output Data Timing” on page 13 for the description of FRAME_VALID timing.

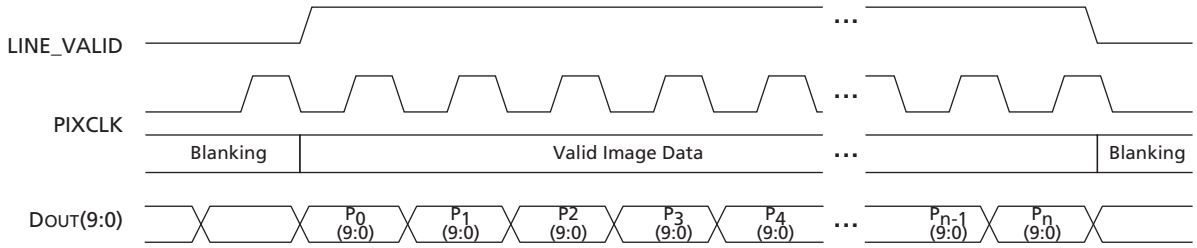
Figure 6: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9V022 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

Figure 7: Timing Example of Pixel Data



The PIXCLK is a nominally inverted version of the master clock (SYSCLK). This allows PIXCLK to be used as a clock to latch the data. However, when column bin 2 is enabled, the PIXCLK is HIGH for one complete master clock master period and then LOW for one complete master clock period; when column bin 4 is enabled, the PIXCLK is HIGH for two complete master clock periods and then LOW for two complete master clock periods. It is continuously enabled, even during the blanking period. Setting R0x74 bit[4] = 1 causes the MT9V022 to invert the polarity of the PIXCLK.

The parameters P1, A, Q, and P2 in Figure 8 are defined in Table 2.

Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals

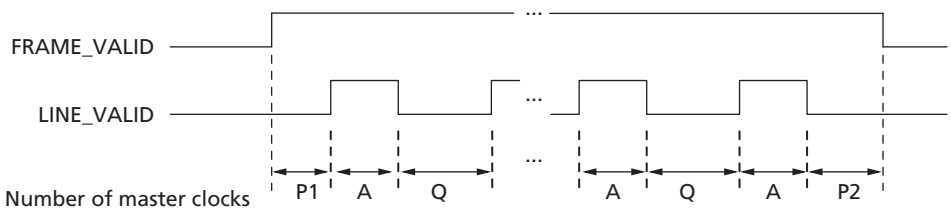


Table 2: Frame Time

Parameter	Name	Equation	Default Timing at 26.66 MHz
A	Active data time	R0x04	752 pixel clocks = 752 master = 28.20µs
P1	Frame start blanking	R0x05 - 23	71 pixel clocks = 71master = 2.66µs
P2	Frame end blanking	23 (fixed)	23 pixel clocks = 23 master = 0.86µs
Q	Horizontal blanking	R0x05	94 pixel clocks = 94 master = 3.52µs

Table 2: Frame Time (continued)

Parameter	Name	Equation	Default Timing at 26.66 MHz
A+Q	Row time	R0x04 + R0x05	846 pixel clocks = 846 master = 31.72µs
V	Vertical blanking	(R0x06) x (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43ms
Nrows x (A + Q)	Frame valid time	(R0x03) × (A + Q)	406,080 pixel clocks = 406,080 master = 15.23ms
F	Total frame time	V + (Nrows x (A + Q))	444,154 pixel clocks = 444,154 master = 16.66ms

Sensor timing is shown above in terms of pixel clock and master clock cycles (refer to Figure 7 on page 13). The recommended master clock frequency is 26.66 MHz. The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of R0x0B) is less than the number of active rows plus blanking rows minus overhead rows (R0x03 + R0x06 - 2). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 3. In this example it is assumed that R0x0B is programmed with 523 rows. For Simultaneous Mode, if the exposure time register (0x0B) exceeds the total readout time, then vertical blanking is internally extended automatically to adjust for the additional integration time required. This extended value is **not** written back to R0x06 (vertical blanking). R0x06 can be used to adjust frame to frame readout time. This register does not effect the exposure time but it may extend the readout time.

Table 3: Frame Time—Long Integration Time

Parameter	Name	Equation (Number of Master Clock Cycles)	Default Timing at 26.66 MHz
V’	Vertical blanking (long integration time)	(R0x0B + 2 - R0x03) × (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43ms
F”	Total frame time (long integration time)	(R0x0B + 2) × (A + Q) + 4	444,154 pixel clocks = 444,154 master = 16.66ms

Notes: 1. The MT9V022 uses column parallel analog-digital converters, thus short row timing is not possible. The minimum total row time is 660 columns (horizontal width + horizontal blanking). The minimum horizontal blanking is 43. When the window width is set below 617, horizontal blanking must be increased. The frame rate will not increase for row times less than 660 columns.

Serial Bus Description

Registers are written to and read from the MT9V022 through the two-wire serial interface bus. The MT9V022 is a serial interface slave with four possible IDs (0x90, 0x98, 0xB0 and 0xB8) determined by the S_CTRL_ADR0 and S_CTRL_ADR1 input pins. Data is transferred into the MT9V022 and out through the serial data (SDATA) line. The SDATA line is pulled up to VDD off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16-bit wide, and can be accessed through 16- or 8-bit two-wire serial interface sequences.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(n) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9V022 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit. The MT9V022 allows for 8-bit data transfers through the two-wire serial interface by writing (or reading) the most significant 8 bits to the register and then writing (or reading) the least significant 8 bits to R0xF0 (240).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB of the address indicates write mode, and a "1" indicates read mode. As indicated above, the MT9V022 allows four possible slave addresses determined by the two input pins, S_CTRL_ADR0 and S_CTRL_ADR1.

Table 4: Slave Address Modes

{S_CTRL_ADR1, S_CTRL_ADR0}	Slave Address	Write/Read Mode
00	0x90	Write
	0x91	Read
01	0x98	Write
	0x99	Read
10	0xB0	Write
	0xB1	Read
11	0xB8	Write
	0xB9	Read

Data Bit Transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

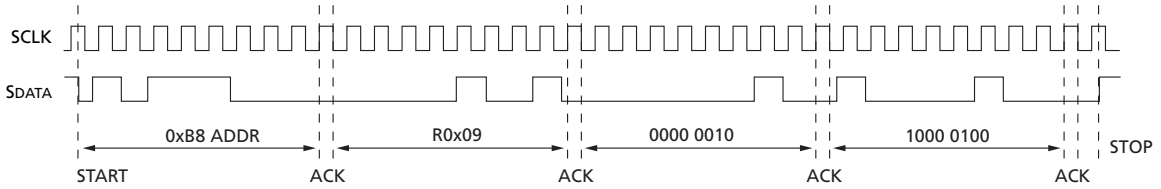
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Read and Write Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 9. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

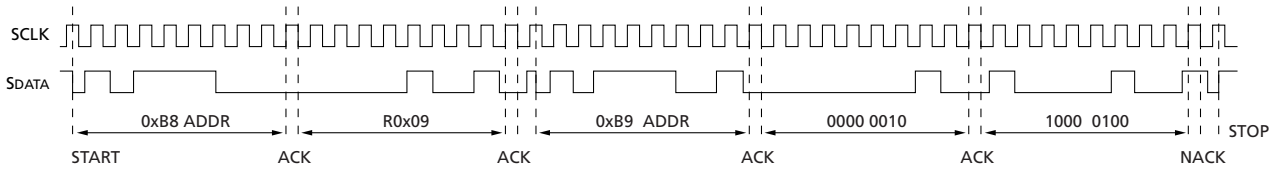
Figure 9: Timing Diagram Showing a Write to R0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 10. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

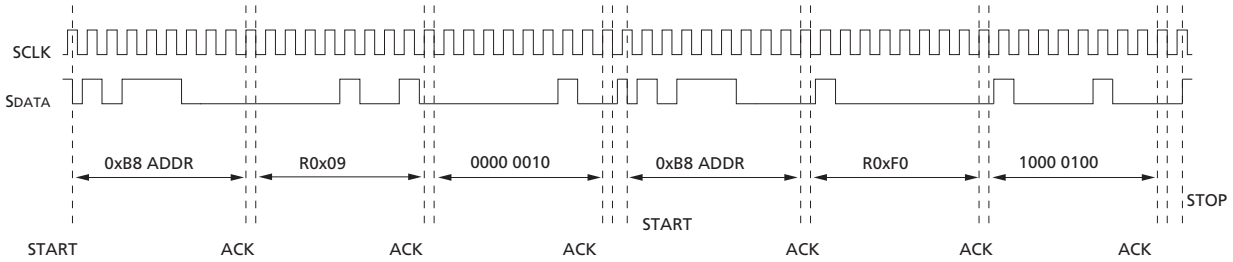
Figure 10: Timing Diagram Showing a Read from R0x09; Returned Value 0x0284



8-Bit Write Sequence

To be able to write 1 byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (R0xF0). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 11 on page 18, a typical sequence for 8-bit writing is shown. The second byte is written to the special register (R0xF0).

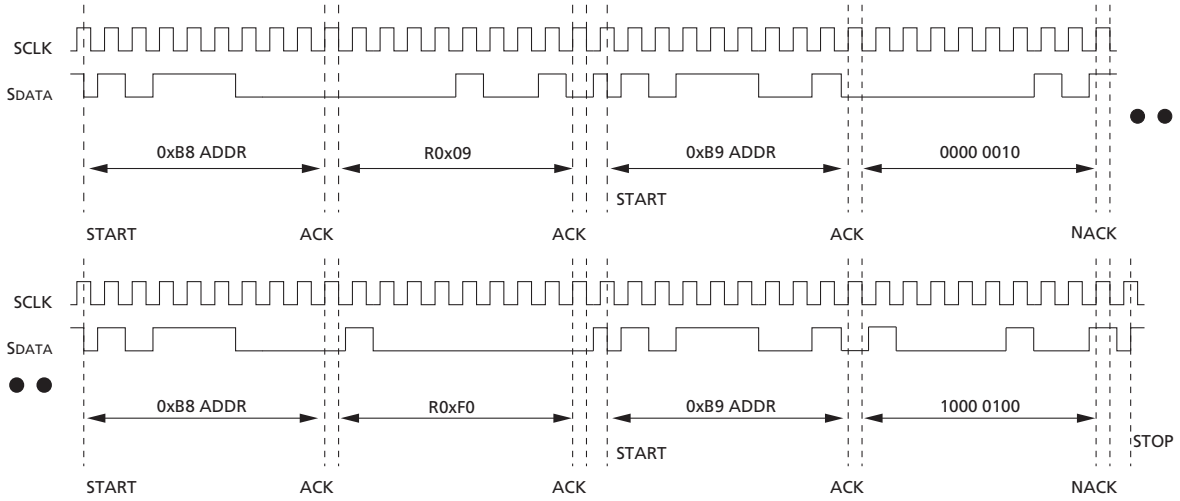
Figure 11: Timing Diagram Showing a Bytewise Write to R0x09 with the Value 0x0284



8-Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (R0xF1) the lower 8 bits are accessed (Figure 12). The master sets the no-acknowledge bits shown.

Figure 12: Timing Diagram Showing a Bytewise Read from R0x09; Returned Value 0x0284



Register Lock

Included in the MT9V022 is a register lock (R0xFE) feature that can be used as a solution to reduce the probability of an inadvertent noise-triggered two-wire serial interface write to the sensor. All registers (or read mode register—register 13 only) can be locked; it is important to prevent an inadvertent two-wire serial interface write to register 13 in automotive applications since this register controls the image orientation and any unintended flip to an image can cause serious results.

At power-up, the register lock defaults to a value of 0xBEEF, which implies that all registers are unlocked and any two-wire serial interface writes to the register gets committed.

Lock All Registers

If a unique pattern (0xDEAD) to R0xFE is programmed, any subsequent two-wire serial interface writes to registers (except R0xFE) are NOT committed. Alternatively, if the user writes a 0xBEEF to the register lock register, all registers are unlocked and any subsequent two-wire serial interface writes to the register are committed.

Lock Read Mode Register Only (R0x0D)

If a unique pattern (0xDEAF) to R0xFE is programmed, any subsequent two-wire serial interface writes to register 13 is NOT committed. Alternatively, if the user writes a 0xBEEF to register lock register, register 13 is unlocked and any subsequent two-wire serial interface writes to this register is committed.

Feature Description

Operational Modes

The MT9V022 works in master, snapshot, or slave mode. In master mode the sensor generates the readout timing. In snapshot mode it accepts an external trigger to start integration, then generates the readout timing. In slave mode the sensor accepts both external integration and readout controls. The integration time is programmed through the two-wire serial interface during master or snapshot modes, or controlled via externally generated control signal during slave mode.

Master Mode

There are two possible operation methods for master mode: simultaneous and sequential. One of these operation modes must be selected via the two-wire serial interface.

Simultaneous Master Mode

In simultaneous master mode, the exposure period occurs during readout. The frame synchronization waveforms are shown in Figure 13 and Figure 14. The exposure and readout happen in parallel rather than sequential, making this the fastest mode of operation.

Figure 13: Simultaneous Master Mode Synchronization Waveforms #1

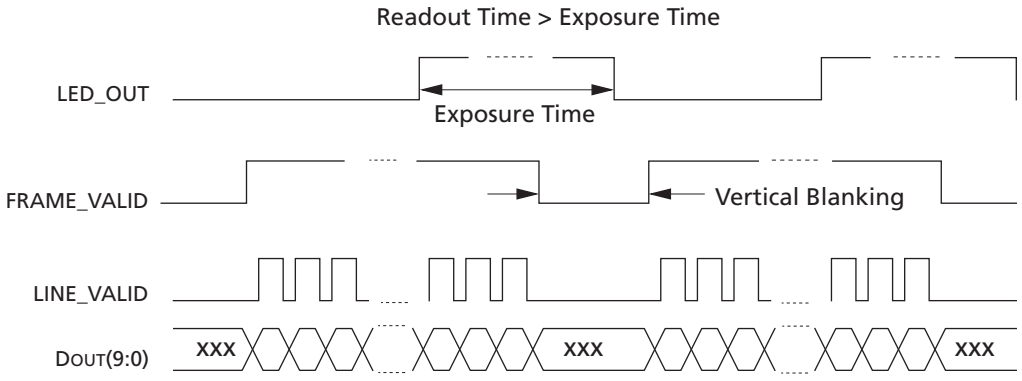
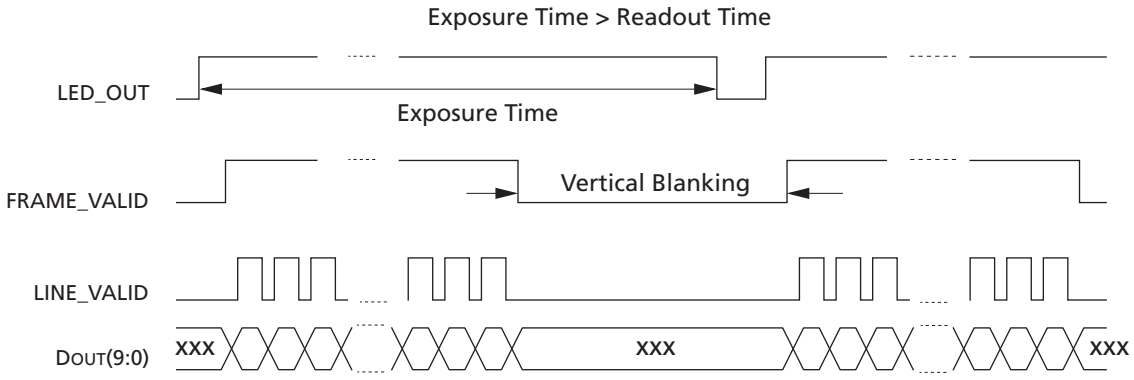


Figure 14: Simultaneous Master Mode Synchronization Waveforms #2

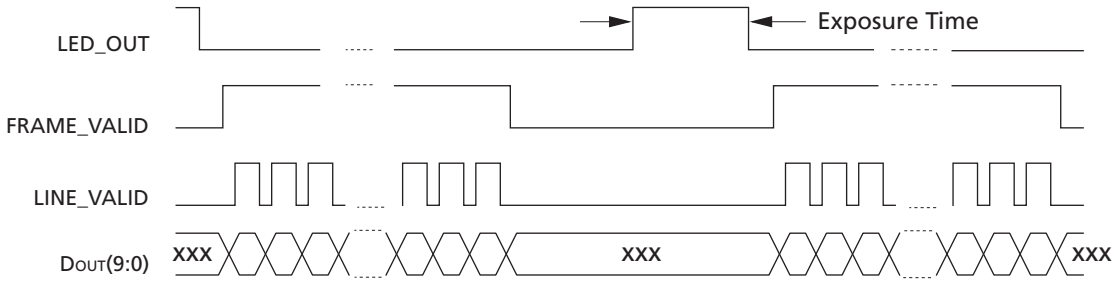


When exposure time is greater than the sum of vertical blank and window height, the number of vertical blank rows is increased automatically to accommodate the exposure time.

Sequential Master Mode

In sequential master mode the exposure period is followed by readout. The frame synchronization waveforms for sequential master mode are shown in Figure 15. The frame rate changes as the integration time changes.

Figure 15: Sequential Master Mode Synchronization Waveforms



Snapshot Mode

In snapshot mode the sensor accepts an input trigger signal which initiates exposure, and is immediately followed by readout. Figure 16 shows the interface signals used in snapshot mode. In snapshot mode, the start of the integration period is determined by the externally applied EXPOSURE pulse that is input to the MT9V022. The integration time is preprogrammed via the two-wire serial interface on R0x0B. After the frame's integration period is complete the readout process commences and the syncs and data are output. Sensor in snapshot mode can capture a single image or a sequence of images. The frame rate may only be controlled by changing the period of the user supplied EXPOSURE pulse train. The frame synchronization waveforms for snapshot mode are shown in Figure 17.

Figure 16: Snapshot Mode Interface Signals

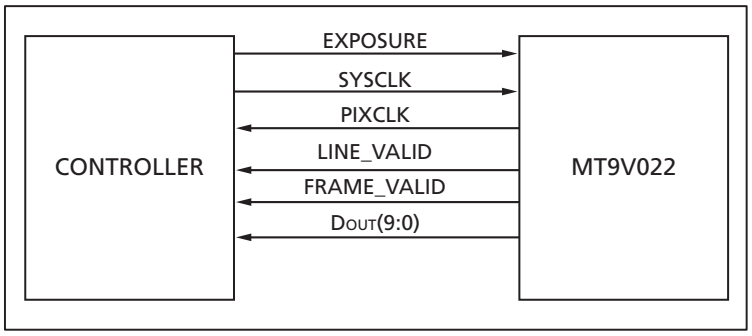
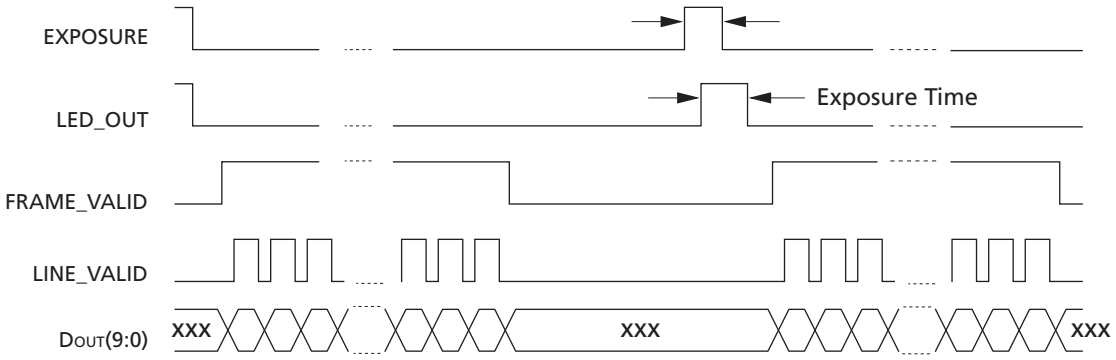


Figure 17: Snapshot Mode Frame Synchronization Waveforms



Slave Mode

In slave mode, the exposure and readout are controlled using the EXPOSURE, STFRM_OUT, and STLN_OUT pins. When the slave mode is enabled, STFRM_OUT and STLN_OUT become input pins.

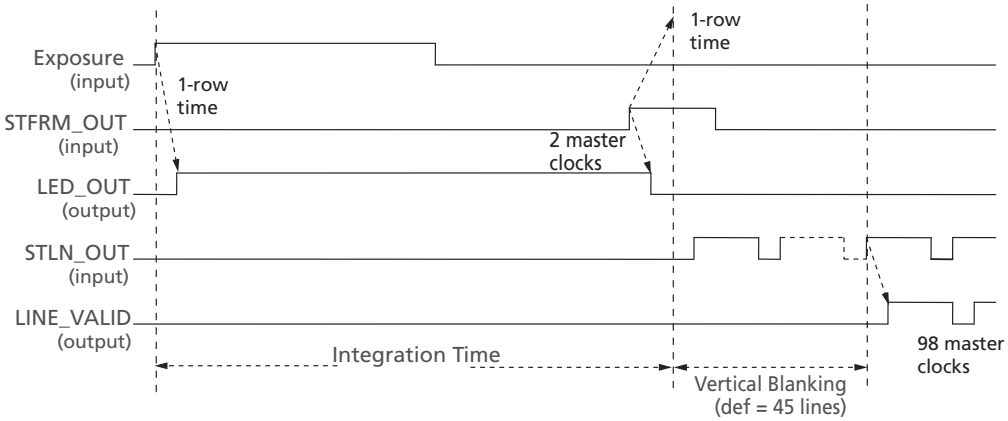
The start and end of integration are controlled by EXPOSURE and STFRM_OUT pulses, respectively. While a STFRM_OUT pulse is used to stop integration, it is also used to enable the readout process.

After integration is stopped, the user provides STLN_OUT pulses to trigger row readout. A full row of data is read out with each STLN_OUT pulse. The user must provide enough time between successive STLN_OUT pulses to allow the complete readout of one row.

It is also important to provide additional STLN_OUT pulses to allow the sensors to read the vertical blanking rows. It is recommended that the user program the vertical blank register (R0x06) with a value of 4, and achieve additional vertical blanking between frames by delaying the application of the STFRM_OUT pulse.

The elapsed time between the rising edge of STLN_OUT and the first valid pixel data is [horizontal blanking register (R0x05) + 4] clock cycles.

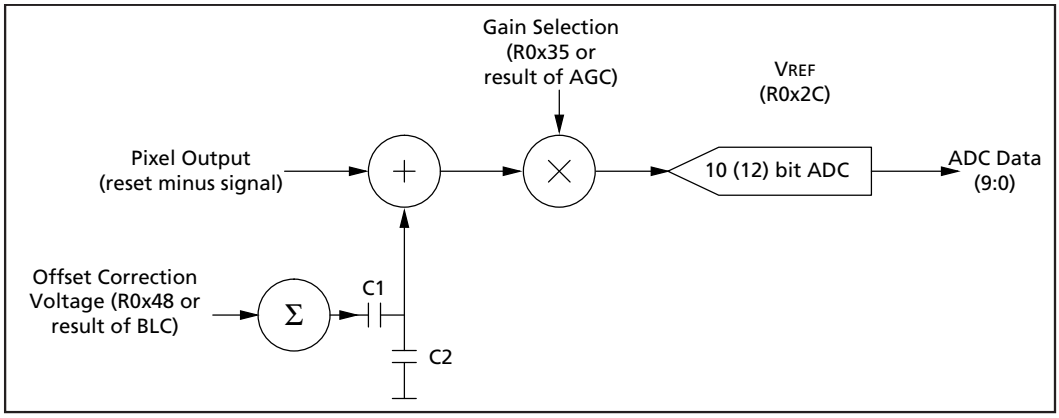
Figure 18: Slave Mode Operation



Signal Path

The MT9V022 signal path consists of a programmable gain, a programmable analog offset, and a 10-bit ADC. See "Black Level Calibration" on page 30 for the programmable offset operation description.

Figure 19: Signal Path



On-Chip Biases

ADC Voltage Reference

The ADC voltage reference is programmed through R0x2C, bits 2:0. The ADC reference ranges from 1.0V to 2.1V. The default value is 1.4V. The increment size of the voltage reference is 0.1V from 1.0V to 1.6V (R0x2C[2:0] values 0 to 6). At R0x2C[2:0] = 7, the reference voltage jumps to 2.1V.

The effect of the ADC calibration does not scale with VREF. Instead it is a fixed value relative to the output of the analog gain stage. At default, one LSB of calibration equals two LSB in output data ($1LSB_{Offset}$ = 2mV, $1LSB_{ADC}$ = 1mV).

It is very important to preserve the correct values of the other bits in R0x2C. The default register setting is 0x0004.

V_Step Voltage Reference

This voltage is used for pixel high dynamic range operations, programmable from R0x31 through R0x34.

Chip Version

Chip version registers R0x00 and R0xFF are read-only.

Window Control

Registers R0x01 column start, R0x02 Row Start, R0x03 window height (row size), and R0x04 Window Width (column size) control the size and starting coordinates of the window.

The values programmed in the window height and width registers are the exact window height and width out of the sensor. The window start value should never be set below four.

To read out the dark rows set bit 6 of R0x0D. In addition, bit 7 of R0x0D can be used to display the dark columns in the image.

Blanking Control

Horizontal blanking and vertical blanking registers R0x05 and R0x06 respectively control the blanking time in a row (horizontal blanking) and between frames (vertical blanking).

- Horizontal blanking is specified in terms of pixel clocks.
- Vertical blanking is specified in terms of numbers of rows.

The actual imager timing can be calculated using Table 2 on page 13 and Table 3 on page 14 which describe "Row Timing and FRAME_VALID/LINE_VALID signals." The minimum number of vertical blank rows is 4.

Pixel Integration Control

Total Integration

R0x0B Total Shutter Width (In Terms of Number of Rows)

This register (along with the window width and horizontal blanking registers) controls the integration time for the pixels.

The actual total integration time, ^{t}INT, is:

^{t}INT = (Number of rows of integration × row time) + Overhead, where:
The number of rows integration is equal to the result of automatic exposure control (AEC) which may vary from frame to frame, or, if AEC is disabled, the value in R0x0B
Row time = (R0x04 + R0x05) master clock periods
Overhead = (R0x04 + R0x05 – 255) master clock periods

Typically, the value of R0x0B (total shutter width) is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If R0x0B is increased beyond the total number of rows per frame, it is required to add additional blanking rows using R0x06 as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means frame time must be a multiple of 1/120 of a second. Under 50Hz flicker, frame time must be a multiple of 1/100 of a second.

Changes to Integration Time

With automatic exposure control disabled (R0xAF, bit 0 is cleared to LOW), and if the total integration time (R0x0B) is changed via the two-wire serial interface while FRAME_VALID is asserted for frame *n*, the first frame output using the new integration time is frame (*n* + *2*). Similarly, when automatic exposure control is enabled, any change to the integration time for frame *n* first appears in frame (*n* + *2*) output.

The sequence is as follows:

1. During frame *n*, the new integration time is held in the R0x0B live register.
2. At the start of frame (*n* + *1*), the new integration time is transferred to the exposure control module. Integration for each row of frame (*n* + *1*) has been completed using the old integration time. The earliest time that a row can start integrating using the new integration time is immediately after that row has been read for frame (*n* + *1*). The actual time that rows start integrating using the new integration time is dependent on the new value of the integration time.
3. When frame (*n* + *1*) is read out, it is integrated using the new integration time. If the integration time is changed (R0x0B written) on successive frames, each value written is applied to a single frame; the latency between writing a value and it affecting the frame readout remains at two frames.
   However, when automatic exposure control is disabled, if the integration time is changed through the two-wire serial interface after the falling edge of FRAME_VALID for frame *n*, the first frame output using the new integration time becomes frame (*n* + *3*).

Figure 20: Latency When Changing Integration