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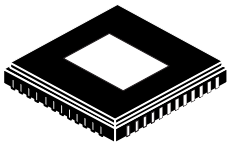
MT9V032

MT9V032 1/3-Inch Wide VGA CMOS Digital Image Sensor

ON Semiconductor®

www.onsemi.com



CLCC48 11.43 × 11.43
CASE 848AQ

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Value
Optical Format	1/3-inch
Active Imager Size	4.51 mm (H) × 2.88 mm (V) 5.35 mm diagonal
Active Pixels	752H × 480 V
Pixel Size	6.0 μm × 6.0 μm
Color Filter Array	Monochrome or color RGB Bayer Pattern
Shutter Type	Global Shutter
Maximum Data Rate Master Clock	26.6 MPS/26.6 MHz
Full Resolution	752 x 480
Frame Rate	60 fps (at full resolution)
ADC Resolution	10−bit column−parallel
Responsivity	4.8 V/lux−sec (550 nm)
Dynamic Range	>55 dB; >80 dB−100dB in HDR mode
Supply Voltage	3.3 V ± 0.3 V (all supplies)
Power Consumption	<320 mW at maximum data rate; 100 μW standby Power
Operating Temperature	−30°C to + 70°C
Packaging	48−Pin CLCC

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Array Format: Wide−VGA, Active 752H x 480V (360,960 Pixels)
- Global Shutter Photodiode Pixels; Simultaneous Integration And Readout
- Monochrome Or Color: Near_IR Enhanced Performance For Use With Non−Visible NIR Illumination
- Readout Modes: Progressive Or Interlaced
- Shutter Efficiency: >99%
- Simple Two−Wire Serial Interface
- Register Lock Capability
- Window Size: User Programmable To Any Smaller Format (QVGA, CIF, QCIF, etc.). Data Rate Can Be Maintained Independent Of Window Size
- Binning: 2 x 2 And 4 x 4 Of The Full Resolution
- ADC: On−Chip, 10−bit Column−Parallel (Option To Operate In 12−bit To 10−bit Companding Mode)
- Automatic Controls: Auto Exposure Control (AEC) And Auto Gain Control (AGC); Variable Regional And Variable Weight AEC/AGC
- Support For Four Unique Serial Control Register IDs To Control Multiple Imagers On The Same Bus
- Data Output Formats:
- Single Sensor Mode:
  10−bit Parallel/Stand−Alone
  8−bit Or 10−bit Serial LVDS
- Stereo Sensor Mode:
  Interspersed 8−bit Serial LVDS

Applications

- Security
- High Dynamic Range Imaging
- Unattended Surveillance
- Stereo Vision
- Video As Input
- Machine Vision
- Automation

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ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description †
MT9V032C12STCD3−GEVK	48−pin CLCC demo3 kit (color)	
MT9V032C12STCD−GEVK	48−pin CLCC demo kit (color)	
MT9V032C12STC−DP	48−pin CLCC (color)	Dry Pack with Protective Film
MT9V032C12STC−DR	48−pin CLCC (color)	Dry Pack without Protective Film
MT9V032C12STCH−GEVB	48−pin CLCC headboard only (color)	
MT9V032C12STC−TP	48−pin CLCC (color)	Tape & Reel with Protective Film
MT9V032C12STMD−GEVK	48−pin CLCC demo kit (mono)	
MT9V032C12STM−DP	48−pin CLCC (mono)	Dry Pack with Protective Film
MT9V032C12STM−DR	48−pin CLCC (mono)	Dry Pack without Protective Film
MT9V032C12STMH−GEVB	48−pin CLCC headboard only (mono)	
MT9V032C12STM−TP	48−pin CLCC (mono)	Tape & Reel with Protective Film

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

GENERAL DESCRIPTION

The ON Semiconductor MT9V032 is a 1/3−inch wide−VGA format CMOS active−pixel digital image sensor with global shutter and high dynamic range (HDR) operation. The sensor has specifically been designed to support the demanding interior and exterior surveillance imaging needs, which makes this part ideal for a wide variety of imaging applications in real−world environments.

This wide−VGA CMOS image sensor features ON Semiconductor's breakthrough low−noise CMOS imaging technology that achieves CCD image quality (based on signal−to−noise ratio and low−light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The active imaging pixel array is 752H x 480V. It incorporates sophisticated camera functions on−chip—such as binning 2 x 2 and 4 x 4, to improve sensitivity when operating in smaller resolutions—as well as windowing, column and row mirroring. It is programmable through a simple two−wire serial interface.

The MT9V032 can be operated in its default mode or be programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide−VGA−size image at 60 frames per second (fps).

An on−chip analog−to−digital converter (ADC) provides 10 bits per pixel. A 12−bit resolution companded for 10 bits for small signals can be alternatively enabled, allowing more accurate digitization for darker areas in the image.

In addition to a traditional, parallel logic output the MT9V032 also features a serial low−voltage differential signaling (LVDS) output. The sensor can be operated in a stereo−camera, and the sensor, designated as a stereo−master, is able to merge the data from itself and the stereo−slave sensor into one serial LVDS stream.

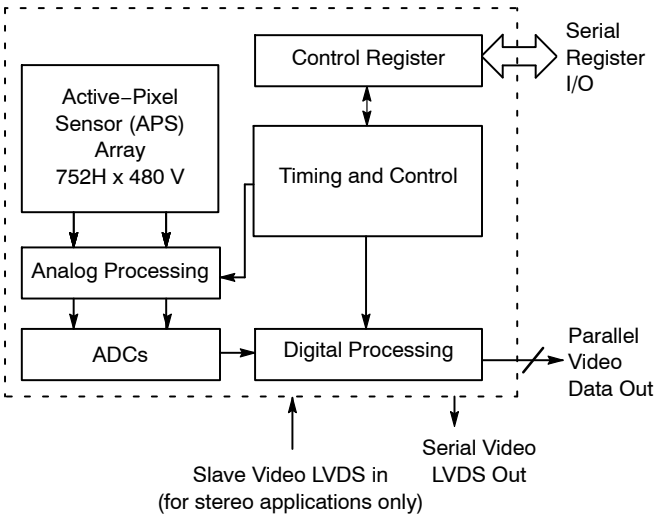


Figure 1. Block Diagram

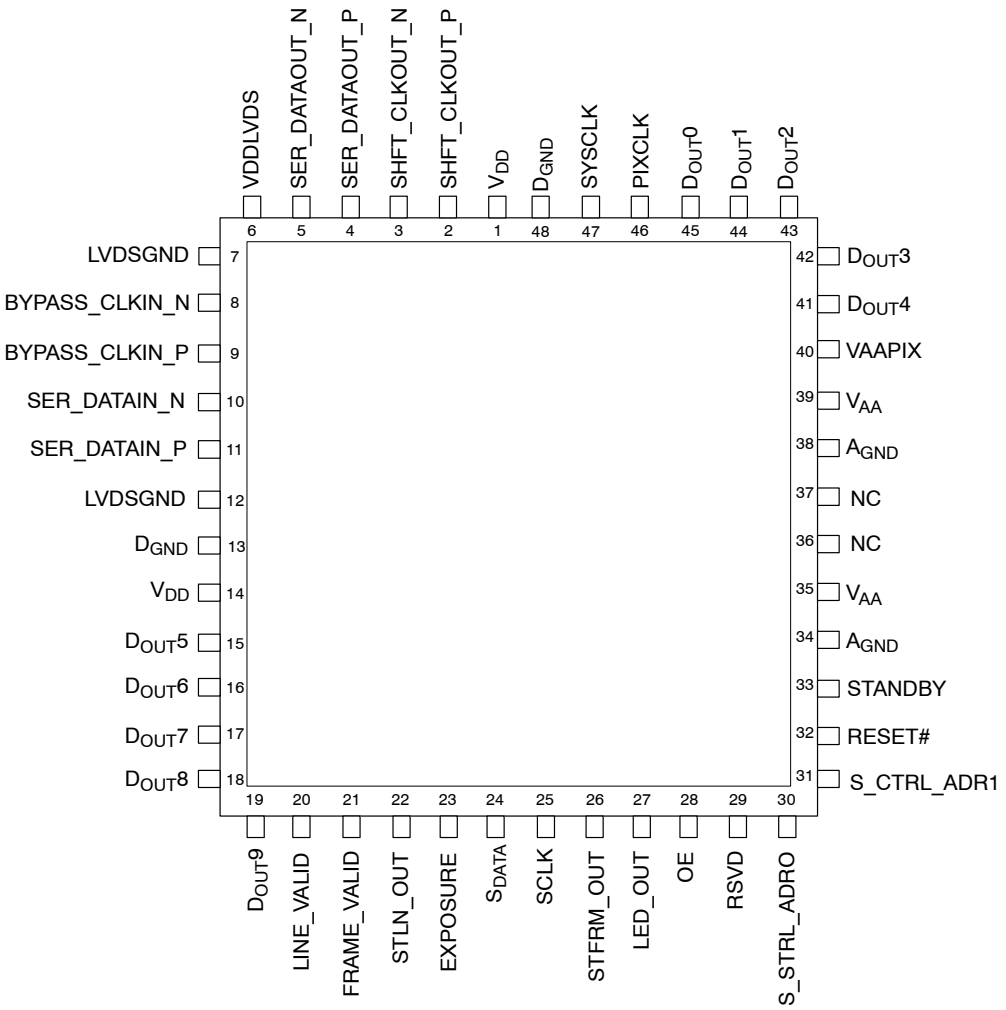


Figure 2. 48-Pin CLCC Pinout Diagram

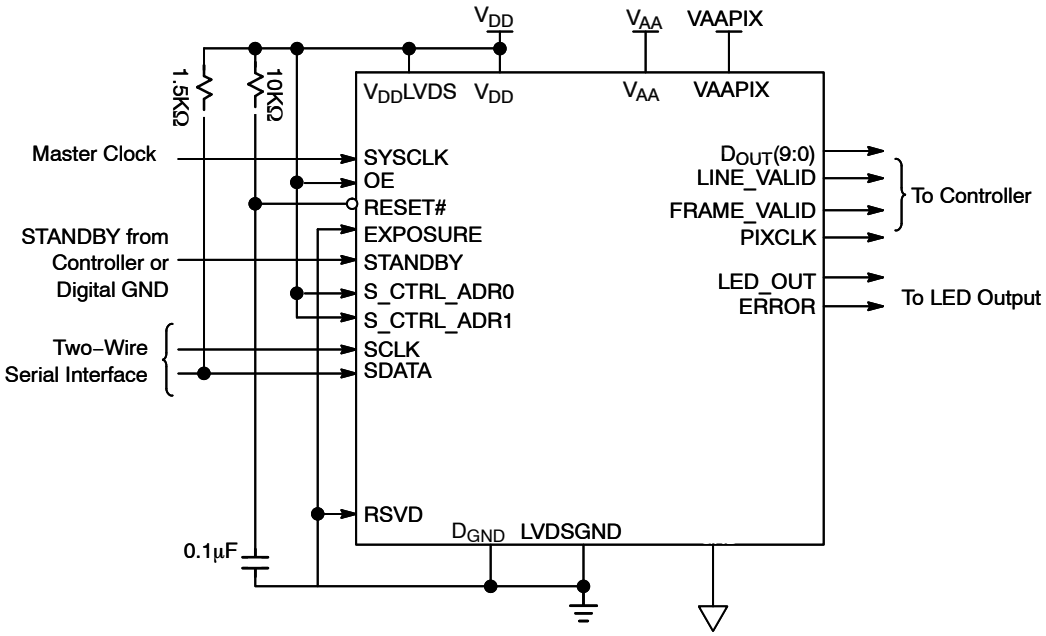
Table 3. PIN DESCRIPTIONS (Only pins DOUT0 through DOUT9 may be tri−stated)

48−Pin LLCC Numbers	Symbol	Type	Descriptions	Note
29	RSVD	Input	Connect to DGND.	1
10	SER_DATAIN_N	Input	Serial data in for stereoscopy (differential negative). Tie to 1kΩ pull−up (to 3.3V) in non−stereoscopy mode.	
11	SER_DATAIN_P	Input	Serial data in for stereoscopy (differential positive). Tie to DGND in non−stereoscopy mode.	
8	BYPASS_CLKIN_N	Input	Input bypass shift−CLK (differential negative). Tie to 1KΩ pull−up (to 3.3V) in non−stereoscopy mode.	
9	BYPASS_CLKIN_P	Input	Input bypass shift−CLK (differential positive). Tie to DGND in non−stereoscopy mode.	
23	EXPOSURE	Input	Rising edge starts exposure in slave mode.	
25	SCLK	Input	Two−wire serial interface clock. Connect to VDD with 1.5K resistor even when no other two−wire serial interface peripheral is attached.	
28	OE	Input	DOUT enable pad, active HIGH.	2
30	S_CTRL_ADR0	Input	Two−wire serial interface slave address bit 3.	
31	S_CTRL_ADR1	Input	Two−wire serial interface slave address bit 5.	
32	RESET#	Input	Asynchronous reset. All registers assume defaults.	
33	STANDBY	Input	Shut down sensor operation for power saving.	

Table 3. PIN DESCRIPTIONS (Only pins DOUT0 through DOUT9 may be tri−stated)

48−Pin LLCC Numbers	Symbol	Type	Descriptions	Note
47	SYSCLK	Input	Master clock (26.6 MHz).	
24	SDATA	I/O	Two−wire serial interface data. Connect to VDD with 1.5K resistor even when no other two−wire serial interface peripheral is attached.	
22	STLN_OUT	I/O	Output in master mode−−start line sync to drive slave chip in−phase; input in slave mode.	
26	STFRM_OUT	I/O	Output in master mode−−start frame sync to drive a slave chip in−phase; input in slave mode.	
20	LINE_VALID	Output	Asserted when DOUT data is valid.	
21	FRAME_VALID	Output	Asserted when DOUT data is valid.	
15	DOUT5	Output	Parallel pixel data output 5.	
16	DOUT6	Output	Parallel pixel data output 6.	
17	DOUT7	Output	Parallel pixel data output 7.	
18	DOUT8	Output	Parallel pixel data output 8	
19	DOUT9	Output	Parallel pixel data output 9.	
27	LED_OUT	Output	LED strobe output.	
41	DOUT4	Output	Parallel pixel data output 4.	
42	DOUT3	Output	Parallel pixel data output 3.	
43	DOUT2	Output	Parallel pixel data output 2.	
44	DOUT1	Output	Parallel pixel data output 1.	
45	DOUT0	Output	Parallel pixel data output 0.	
46	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.	
2	SHFT_CLKOUT_N	Output	Output shift CLK (differential negative).	
3	SHFT_CLKOUT_P	Output	Output shift CLK (differential positive).	
4	SER_DATAOUT_N	Output	Serial data out (differential negative).	
5	SER_DATAOUT_P	Output	Serial data out (differential positive).	
1, 14	VDD	Supply	Digital power 3.3V.	
35, 39	VAA	Supply	Analog power 3.3V.	
40	VAAPIX	Supply	Pixel power 3.3V.	
6	VDDLVDS	Supply	Dedicated power for LVDS pads.	
7, 12	LVDSGND	Ground	Dedicated GND for LVDS pads.	
13, 48	DGND	Ground	Digital GND.	
34, 38	AGND	Ground	Analog GND.	
36, 37	NC	NC	No connect.	3

1. Pin 29 (RSVD) must be tied to GND
2. Output Enable (OE) tri−states signals DOUT0−DOUT9. No other signals are tri−stated with OE.
3. No connect. These pins must be left floating for proper operation.



NOTE: LVDS signals are to be left floating.

Figure 3. Typical Configuration (Connection)−Parallel Output Mode

PIXEL DATA FORMAT

Pixel Array Structure

The MT9V032 pixel array is configured as 782 columns by 492 rows, shown in Figure 4. The left 26 columns and the top eight rows of pixels are optically black and can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment. However, the middle four black rows can also be read out by setting the sensor to raw data output mode. There are 753 columns by 481 rows of optically active pixels. The active area is surrounded with optically transparent dummy columns and rows to improve image uniformity within the active area. One additional active column and active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel.

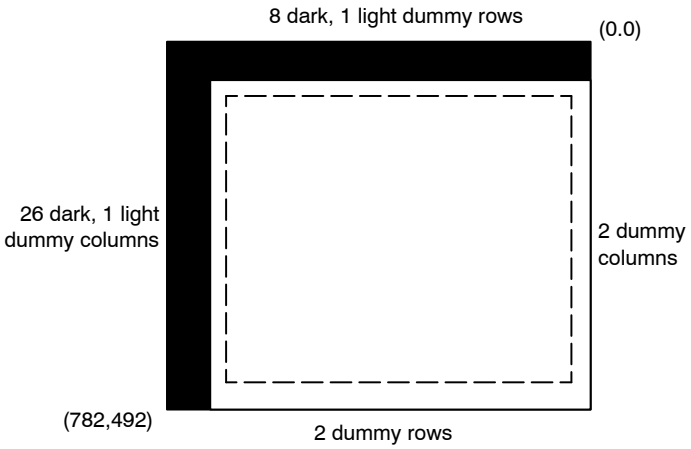


Figure 4. Pixel Array Description

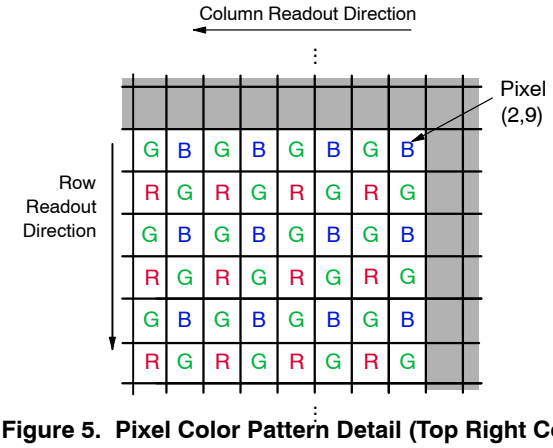


Figure 5. Pixel Color Pattern Detail (Top Right Corner)

COLOR DEVICE LIMITATIONS

The color version of the MT9V032 does not support or offers reduced performance for the following functionalities.

Pixel Binning

Pixel binning is done on immediate neighbor pixels only; no facility is provided to skip pixels according to a Bayer pattern. Therefore, the result of binning combines pixels of different colors. For more information, see “Pixel Binning”.

Interlaced Readout

Interlaced readout yields one field consisting only of red and green pixels and another consisting only of blue and green pixels. This is due to the Bayer pattern of the CFA.

Automatic Black Level Calibration

When the color bit is set (R0x0F[2]=1), the sensor uses GREEN1 pixels black level correction value, which is applied to all colors. To use calibration value based on all dark pixels offset values, the color bit should be cleared.

Other Limiting Factors

Black level correction and row−wise noise correction are applied uniformly to each color. Automatic exposure and gain control calculations are made based on all three colors, not just the green luma channel. High dynamic range does operate; however, ON Semiconductor strongly recommends limiting use to linear operation if good color fidelity is required.

OUTPUT DATA FORMAT

The MT9V032 image data can be read out in a progressive scan or interlaced scan mode. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 6. The amount of horizontal and vertical blanking is programmable through R0x05 and R0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See "Output Data Timing" for the description of FRAME_VALID timing.

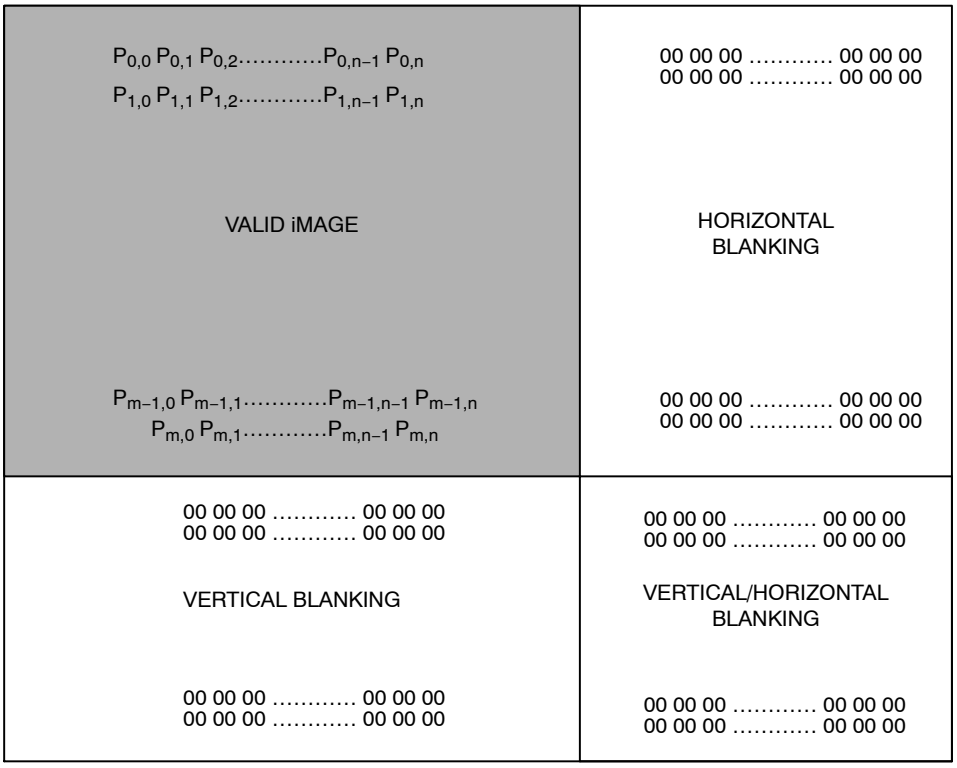


Figure 6. Spatial Illustration of Image Readout

Output Data Timing

The data output of the MT9V032 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10−bit pixel datum is output every PIXCLK period.

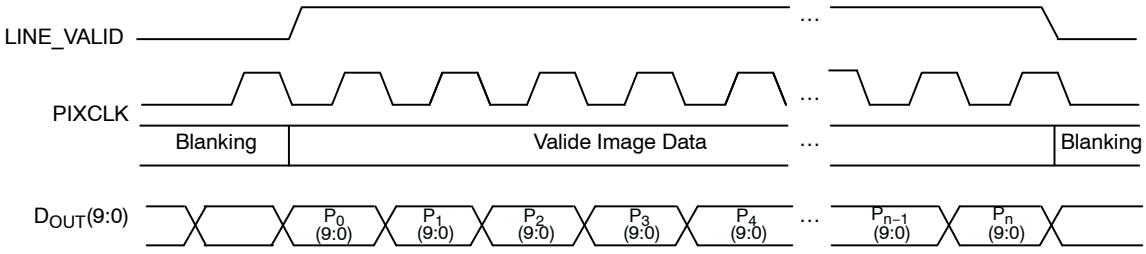


Figure 7. Timing Example of Pixel Data

The PIXCLK is a nominally inverted version of the master clock (SYSCLK). This allows PIXCLK to be used as a clock to latch the data. However, when column bin 2 is enabled, the PIXCLK is HIGH for one complete master clock master period and then LOW for one complete master clock period; when column bin 4 is enabled, the PIXCLK is HIGH for two complete master clock periods and then LOW for two complete master clock periods. It is continuously enabled, even during the blanking period. Setting R0x74 bit[4] = 1 causes the MT9V032 to invert the polarity of the PIXCLK.

The parameters P1, A, Q, and P2 in Figure 8 are defined in Table 4.

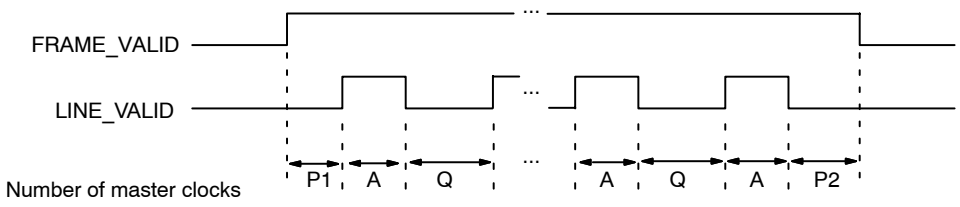


Figure 8. Row Timing and FRAME_VALID/LINE_VALID Signals

Table 4. FRAME TIME – LARGER THAN ONE FRAME

Parameter	Name	Equation	Default Timing at 26.66 MHz
A	Active data time	R0x04	752 pixel clocks = 752 master = 28.20μs
P1	Frame start blanking	R0x05 – 23	71 pixel clocks = 71master = 2.66μs
P2	Frame end blanking	23 (fixed)	23 pixel clocks = 23 master = 0.86μs
Q	Horizontal blanking	R0x05	94 pixel clocks = 94 master = 3.52μs
A+Q	Row time	R0x04 + R0x05	846 pixel clocks = 846 master = 31.72μs
V	Vertical blanking	(R0x06) x (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43ms
Nrows x (A + Q)	Frame valid time	(R0x03) × (A + Q)	406,080 pixel clocks = 406,080 master = 15.23ms
F	Total frame time	V + (Nrows x (A + Q))	444,154 pixel clocks = 444,154 master = 16.66ms

Sensor timing is shown above in terms of pixel clock and master clock cycles (refer to Figure 7). The recommended master clock frequency is 26.66 MHz. The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of R0x0B) is less than the number of active rows plus blanking rows minus overhead rows (R0x03 + R0x06 – 2). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 5. In this example it is assumed that R0x0B is programmed with 523 rows. For Simultaneous Mode, if the exposure time register (0x0B) exceeds the total readout time, then vertical blanking is internally extended automatically to adjust for the additional integration exposure time required. This extended value is **not** written back to R0x06 (vertical blanking). R0x06 can be used to adjust frame to frame readout time. This register does not affect the exposure time but it may extend the readout time.

Table 5. FRAME TIME – LONG INTEGRATION TIME

Parameter	Name	Equation (Number of Master Clock Cycles)	Default Timing at 26.66 MHz
V'	Vertical blanking (long integration time)	(R0x0B + 2 – R0x03) × (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43ms
F"	Total frame time (long integration exposure time)	(R0x0B + 2) × (A + Q) + 4	444,154 pixel clocks = 444,154 master = 16.66ms

4. The MT9V032 uses column parallel analog−to−digital converters, thus short row timing is not possible. The minimum total row time is 660 columns (horizontal width + horizontal blanking). The minimum horizontal blanking is 43. When the window width is set below 617, horizontal blanking must be increased. The frame rate will not increase for row times less than 660 columns.

SERIAL BUS DESCRIPTION

Registers are written to and read from the MT9V032 through the two−wire serial interface bus. The MT9V032 is a serial interface slave with four possible IDs (0x90, 0x98, 0xB0,and 0xB8) determined by the S_CTRL_ADR0 and S_CTRL_ADR1 input pins. Data is transferred into the MT9V032 and out through the serial data (SDATA) line. The SDATA line is pulled up to VDD off−chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16−bit wide, and can be accessed through 16− or 8−bit two−wire serial interface sequences.

Protocol

The two−wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8−bit address
- a(n) (no) acknowledge bit
- an 8−bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8−bit address. The last bit of the address determines if the request is a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8−bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9V032 uses 16−bit data for its internal registers, thus requiring two 8−bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write mode slave address and 8−bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is auto−incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit. The MT9V032 allows for 8−bit data transfers through the two−wire serial interface by writing (or reading) the most significant 8 bits to the register and then writing (or reading) the least significant 8 bits to R0xF0 (240).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH−to−LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW−to−HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8−bit address of a two−wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB of the address indicates write mode, and a "1" indicates read mode. As indicated above, the MT9V032 allows four possible slave addresses determined by the two input pins, S_CTRL_ADR0 and S_CTRL_ADR1.

Table 6. SLAVE ADDRESS MODES

{S_CTRL_ADR1, S_CTRL_ADR0}	Slave Address	Write/Read Mode
00	0x90	Write
	0x91	Read
01	0x98	Write
	0x99	Read
10	0xB0	Write
	0xB1	Read
11	0xB8	Write
	0xB9	Read

Data Bit Transfer

One data bit is transferred during each clock pulse. The two−wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two−wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No−Acknowledge Bit

The no−acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no−acknowledge bit is used to terminate a read sequence.

TWO−WIRE SERIAL INTERFACE SAMPLE READ AND WRITE SEQUENCES

16−Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 9. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16−bit data. After each 8−bit word is sent, the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

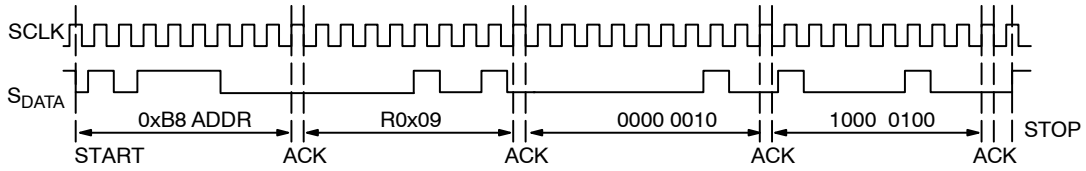


Figure 9. Timing Diagram Showing a Write to R0x09 with Value 0x0284

16−Bit Read Sequence

A typical read sequence is shown in Figure 10. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specify that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is auto−incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

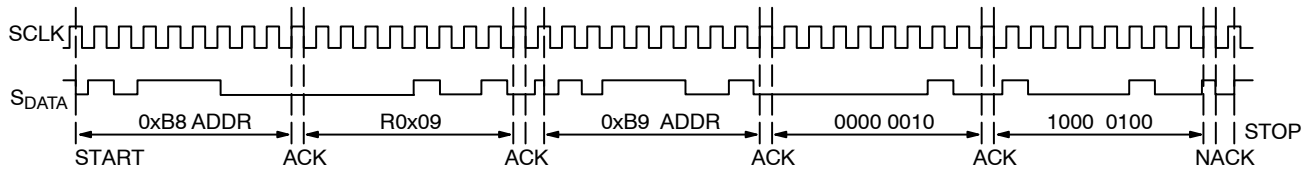


Figure 10. Timing Diagram Showing a Read from R0x09; Returned Value 0x0284

8−Bit Write Sequence

To be able to write 1 byte at a time to the register, a special register address is added. The 8−bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (R0xF0). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 11, a typical sequence for 8−bit writing is shown. The second byte is written to the special register (R0xF0).

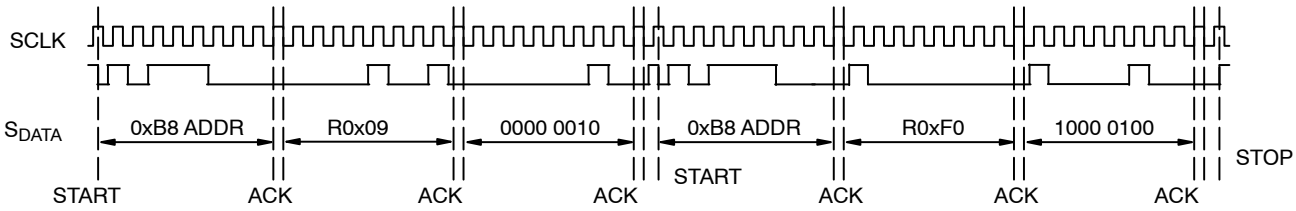


Figure 11. Timing Diagram Showing a Bytewise Write to R0x09 with Value 0x0284

8−Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (R0xF1) the lower 8 bits are accessed (Figure 12). The master sets the no−acknowledge bits shown.

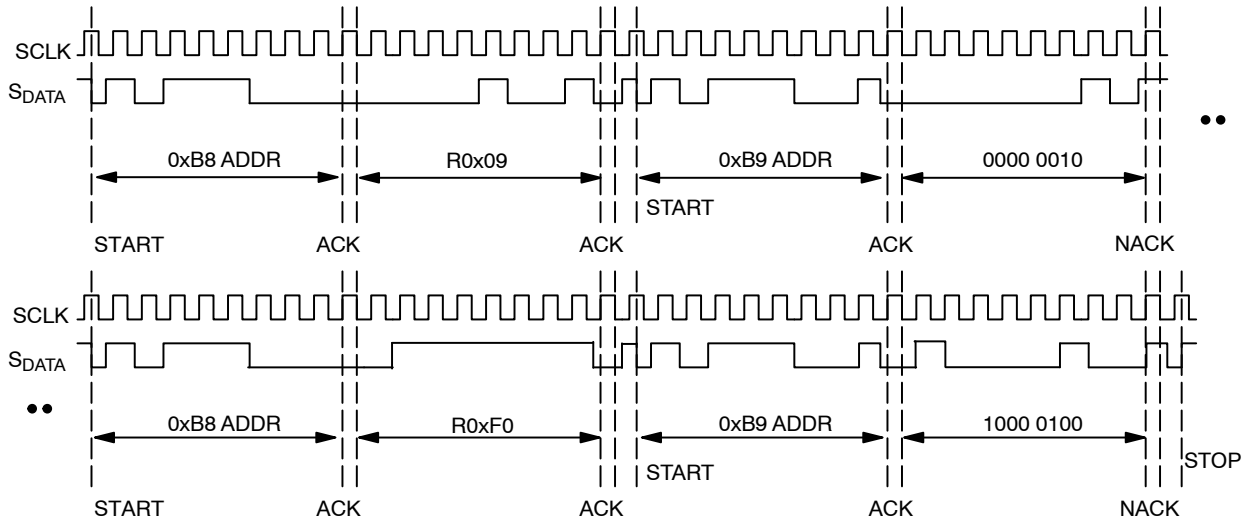


Figure 12. Timing Diagram Showing a Bytewise Read from R0x09; Returned Value 0x0284

Register Lock

Included in the MT9V032 is a register lock (R0xFE) feature that can be used as a solution to reduce the probability of an inadvertent noise−triggered two−wire serial interface write to the sensor. All registers (or read mode register—register 13 only) can be locked.

At power−up, the register lock defaults to a value of 0xBEEF, which implies that all registers are unlocked and any two−wire serial interface writes to the register get committed.

Lock All Registers

If a unique pattern (0xDEAD) to R0xFE is programmed, any subsequent two−wire serial interface writes to registers (except R0xFE) are NOT committed. Alternatively, if the user writes a 0xBEEF to the register lock register, all registers are unlocked and any subsequent two−wire serial interface writes to the register are committed.

Lock Read More Register Only (R0x0D)

If a unique pattern (0xDEAF) to R0xFE is programmed, any subsequent two−wire serial interface writes to register 13 are NOT committed. Alternatively, if the user writes a 0xBEEF to register lock register, register 13 is unlocked and any subsequent two−wire serial interface writes to this register are committed.

REGISTERS

CAUTION: Writing and changing the value of a reserved register (word or bit) puts the device in an unknown state and may damage the device.

Table 7 provides default register descriptions of the registers.

Table 8 provides detailed descriptions of the registers.

Table 7. DEFAULT REGISTER DESCRIPTIONS (1 = always 1;0 = always; d = programmable; ? = read only)

Register # (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x00	Chip Version	0001 0011 0001 00001 (LSB)	Iter. 1: 0x1311 Iter. 2: 0x1311 Iter. 3: 0x1313
0x01	Column Start	0000 00dd dddd dddd	0x0001
0x02	Row Start	0000 000d dddd dddd	0x0004
0x03	Window Height	0000 000d dddd dddd	0x01E0
0x04	Window Width	0000 00dd dddd dddd	0x02F0
0x05	Horizontal Blanking	0000 00dd dddd dddd	0x005E
0x06	Vertical Blanking	0ddd dddd dddd dddd	0x002D
0x07	Chip Control	0000 dddd dddd dddd	0x0388
0x08	Shutter Width 1	0ddd dddd dddd dddd	0x01BB
0x09	Shutter Width 2	0ddd dddd dddd dddd	0x01D9
0x0A	Shutter Width Ctrl	0000 00dd dddd dddd	0x0164
0x0B	Total Shutter Width	0ddd dddd dddd dddd	0x01E0
0x0C	Reset	0000 0000 0000 00dd	0x0000
0x0D	Read Mode	0000 0011 dddd dddd	0x0300
0x0E	Monitor Mode	0000 0000 0000 000d	0x0000
0x0F	Pixel Operation Mode	0000 0000 dddd dddd	0x0011
0x10	Reserved	–	0x0040
0x11	Reserved	–	0x8042
0x12	Reserved	–	0x0022
0x13	Reserved	–	0x2D32
0x14	Reserved	–	0x0E02
0x15	Reserved	–	0x7F32
0x16	Reserved	–	0x2802
0x17	Reserved	–	0x3E38
0x18	Reserved	–	0x3E38
0x19	Reserved	–	0x2802
0x1A	Reserved	–	0x0428
0x1B	LED_OUT Ctrl	0000 0000 0000 00dd	0x0000
0x1C	ADC Mode Control	0000 0000 0000 00dd	0x0002
0x1D	Reserved	–	0x0000
0x1E	Reserved	–	0x0000
0x1F	Reserved	–	0x0000
0x20	Reserved	–	0x01D1
0x21	Reserved	–	0x0020
0x22	Reserved	–	0x0020
0x23	Reserved	–	0x0010

Table 7. DEFAULT REGISTER DESCRIPTIONS (continued)(1 = always 1;0 = always; d = programmable; ? = read only)

Register # (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x24	Reserved	–	0x0010
0x25	Reserved	–	0x0020
0x26	Reserved	–	0x0010
0x27	Reserved	–	0x0010
0x28	Reserved	–	0x0010
0x29	Reserved	–	0x0010
0x2A	Reserved	–	0x0020
0x2B	Reserved	–	0x0004
0x2C	VREF_ADC Control	0000 0000 0000 0ddd	0x0840
0x2D	Reserved	–	0x0004
0x2E	Reserved	–	0x0007
0x2F	Reserved	–	0x0004
0x30	Reserved	–	0x0003
0x31	V1	0000 0000 000d dddd	0x001D
0x32	V2	0000 0000 000d dddd	0x0018
0x33	V3	0000 0000 000d dddd	0x0015
0x34	V4	0000 0000 000d dddd	0x0004
0x35	Analog Gain	0000 0000 0ddd dddd	0x0010
0x36	Max Analog Gain	0000 0000 0ddd dddd	0x0040
0x37	Reserved	–	0x0000
0x38	Reserved	–	0x0000
0x42	Frame Dark Average	0000 0000 ???? ????	RO
0x46	Dark Avg Thresholds	dddd dddd dddd dddd	0x231D
0x47	BL Calib Control	1000 0000 ddd0 000d	0x8080
0x48	BL Calibration Value	0000 0000 dddd dddd	0x0000
0x4C	BL Calib Step Size	0000 0000 000d dddd	0x0002
0x60	Reserved	–	0x0000
0x61	Reserved	–	0x0000
0x62	Reserved	–	0x0000
0x63	Reserved	–	0x0000
0x64	Reserved	–	0x0000
0x65	Reserved	–	0x0000
0x66	Reserved	–	0x0000
0x67	Reserved	–	0x0000
0x68	Reserved	–	RO
0x69	Reserved	–	RO
0x6A	Reserved	–	RO
0x6B	Reserved	–	RO
0x6C	Reserved	–	0x0000
0x70	Row Noise Corr Ctrl 1	0000 d000 00d1 dddd	0x0034
0x71	Reserved	–	0x0000
0x72	Row Noise Constant	0000 0000 dddd dddd	0x002A

Table 7. DEFAULT REGISTER DESCRIPTIONS (continued)(1 = always 1;0 = always; d = programmable; ? = read only)

Register # (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x73	Row Noise Corr Ctrl 2	0000 00dd dddd dddd	0x02F7
0x74	Pixclk, FV, LV	0000 0000 000d dddd	0x0000
0x7F	Digital Test Pattern	0ddd ddd dddd dddd	0x0000
0x80	Tile Weight/Gain X0_Y0	0000 0000 dddd dddd	0x00F4
0x81	Tile Weight/Gain X1_Y0	0000 0000 dddd dddd	0x00F4
0x82	Tile Weight/Gain X2_Y0	0000 0000 dddd dddd	0x00F4
0x83	Tile Weight/Gain X3_Y0	0000 0000 dddd dddd	0x00F4
0x84	Tile Weight/Gain X4_Y0	0000 0000 dddd dddd	0x00F4
0x85	Tile Weight/Gain X0_Y1	0000 0000 dddd dddd	0x00F4
0x86	Tile Weight/Gain X1_Y1	0000 0000 dddd dddd	0x00F4
0x87	Tile Weight/Gain X2_Y1	0000 0000 dddd dddd	0x00F4
0x88	Tile Weight/Gain X3_Y1	0000 0000 dddd dddd	0x00F4
0x89	Tile Weight/Gain X4_Y1	0000 0000 dddd dddd	0x00F4
0x8A	Tile Weight/Gain X0_Y2	0000 0000 dddd dddd	0x00F4
0x8B	Tile Weight/Gain X1_Y2	0000 0000 dddd dddd	0x00F4
0x8C	Tile Weight/Gain X2_Y2	0000 0000 dddd dddd	0x00F4
0x8D	Tile Weight/Gain X3_Y2	0000 0000 dddd dddd	0x00F4
0x8E	Tile Weight/Gain X4_Y2	0000 0000 dddd dddd	0x00F4
0x8F	Tile Weight/Gain X0_Y3	0000 0000 dddd dddd	0x00F4
0x90	Tile Weight/Gain X1_Y3	0000 0000 dddd dddd	0x00F4
0x91	Tile Weight/Gain X2_Y3	0000 0000 dddd dddd	0x00F4
0x92	Tile Weight/Gain X3_Y3	0000 0000 dddd dddd	0x00F4
0x93	Tile Weight/Gain X4_Y3	0000 0000 dddd dddd	0x00F4
0x94	Tile Weight/Gain X0_Y4	0000 0000 dddd dddd	0x00F4
0x95	Tile Weight/Gain X1_Y4	0000 0000 dddd dddd	0x00F4
0x96	Tile Weight/Gain X2_Y4	0000 0000 dddd dddd	0x00F4
0x97	Tile Weight/Gain X3_Y4	0000 0000 dddd dddd	0x00F4
0x98	Tile Weight/Gain X4_Y4	0000 0000 dddd dddd	0x00F4
0x99	Tile Coord. X 0/5	0000 00dd dddd dddd	0x0000
0x9A	Tile Coord. X 1/5	0000 00dd dddd dddd	0x0096
0x9B	Tile Coord. X 2/5	0000 00dd dddd dddd	0x012C
0x9C	Tile Coord. X 3/5	0000 00dd dddd dddd	0x01C2
0x9D	Tile Coord. X 4/5	0000 00dd dddd dddd	0x0258
0x9E	Tile Coord. X 5/5	0000 00dd dddd dddd	0x02F0
0x9F	Tile Coord. Y 0/5	0000 000d dddd dddd	0x0000
0xA0	Tile Coord. Y 1/5	0000 000d dddd dddd	0x0060
0xA1	Tile Coord. Y 2/5	0000 000d dddd dddd	0x00C0
0xA2	Tile Coord. Y 3/5	0000 000d dddd dddd	0x0120
0xA3	Tile Coord. Y 4/5	0000 000d dddd dddd	0x0180
0xA4	Tile Coord. Y 5/5	0000 000d dddd dddd	0x01E0
0XA5	AEC/AGC Desired Bin	0000 0000 00dd dddd	0x003A
0xA6	AEC Update Frequency	0000 0000 0000 dddd	0x0002

Table 7. DEFAULT REGISTER DESCRIPTIONS (continued)(1 = always 1;0 = always; d = programmable; ? = read only)

Register # (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0xA7	Reserved	–	0x0000
0xA8	AEC LPF	0000 0000 0000 00dd	0x0000
0xA9	AGC Update Frequency	0000 0000 0000 dddd	0x0002
0xAA	Reserved	–	0x0000
0xAB	AGC LPF	0000 0000 0000 00dd	0x0002
0xAF	AEC/AGC Enable	0000 0000 0000 00dd	0x0003
0xB0	AEC/AGC Pix Count	dddd dddd dddd dddd	0xABE0
0xB1	LVDS Master Ctrl	0000 0000 0000 dddd	0x0002
0xB2	LVDS Shift Clk Ctrl	0000 0000 000d 0ddd	0x0010
0xB3	LVDS Data Ctrl	0000 0000 000d 0ddd	0x0010
0xB4	Data Stream Latency	0000 0000 0000 00dd	0x0000
0xB5	LVDS Internal Sync	0000 0000 0000 000d	0x0000
0xB6	LVDS Payload Control	0000 0000 0000 000d	0x0000
0xB7	Stereoscop. Error Ctrl	0000 0000 0000 0ddd	0x0000
0xB8	Stereoscop. Error Flag	0000 0000 0000 000?	RO
0xB9	LVDS Data Output	???? ???? ???? ????	RO
0xBA	AGC Gain Output	0000 0000 0??? ????	RO
0XBB	AEC Gain Output	???? ???? ???? ????	RO
0xBC	AGC/AEC Current Bin	0000 0000 00?? ????	RO
0xBD	Maximum Shutter Width	dddd dddd dddd dddd	0x01E0
0xBE	AGC/AEC Bin Difference Threshold	0000 0000 dddd dddd	0x0014
0xBF	Field Blank	0000 000d dddd dddd	0x0016
0xC0	Mon Mode Capture Ctrl	0000 0000 dddd dddd	0x000A
0xC1	Temperature	0000 00?? ???? ????	RO
0xC2	Analog Controls	dddd dddd dddd dddd	0x0840
0xC3	NTSC FV & LV Ctrl	0000 0000 0000 00dd	0x03840
0xC4	NTSC Horiz Blank Ctrl	dddd dddd dddd dddd	0x4416
0xC5	NTSC Vert Blank Ctrl	dddd dddd dddd dddd	0x4421
0xF0	Bytewise Addr	–	0x0000
0xF1	Reserved	–	Reserved
0xFE	Register Lock	dddd dddd dddd dddd	0xBEEF
0xFF	Chip Version	0001 0011 0000 0000	Iter. 1: 0x1311 Iter. 2 : 0x1311 Iter. 3: 0x1313

Shadowed Registers

Some sensor settings cannot be changed during frame readout. For example, changing the register Window Width (R0x04) part way through frame readout results in inconsistent LINE_VALID behavior. To avoid this, the MT9V032 double buffers many registers by implementing a “pending” and a “live” version. Two−wire serial interface reads and writes access the pending register. The live register controls the sensor operation. The value in the pending register is transferred to a live register at a fixed point in the frame timing, called “frame−start.” Frame−start is defined as the point at which the first dark row is read out. By default, this occurs four row times before FRAME_VALID goes HIGH. To determine which registers or register fields are double−buffered in this way, see the “Shadowed” column in Table 8.

- Shadowed
  N = No. The register value is updated and used immediately.
  Y = Yes. The register value is updated at next frame start. Frame start is defined as when the first dark row is read out. By default this is four rows before FRAME_VALID goes HIGH.
- Read/Write
  R = Read−only register/bit.
  W = Read/Write register/bit.

Table 8 provides a detailed description of the registers. Bit fields that are not identified in the table are read only.

Table 8. REGISTER DESCRIPTIONS

Bit	Bit Name	Bit Description	Default in Hex (Dec)	Shad-owed	Legal Values (Dec)	Read/ Write
0X00/0XFF (0/255) CHIP VERSION						
15:0	Chip Version	Chip version—read−only	Iter. 1: 0x1311 (4881) Iter. 2: 0x1311 (4881) Iter. 3: 0x1313 (4883)			R
0X01 (1) COLUMN START						
9:0	Column Start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Readable/active columns are 1−752.	1	Y	1−752	W
0X02 (2) ROW START						
8:0	Row Start	The first row to be read out (not counting any dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than four is not recommended since the dark rows should be read using R0x0D.	4	Y	4−482	W
0X03 (3) WINDOW HEIGHT						
8:0	Window Height	Number of rows in the image to be read out (not counting any dark rows or border rows that may be read).	1E0 (480)	Y	1−480	W
0X04 (4) WINDOW WIDTH						
9:0	Window Width	Number of columns in image to be read out (not counting any dark columns or border columns that may be read).	2F0 (752)	Y	1−752	W
0X05 (5) HORIZONTAL BLANKING						
9:0	Horizontal Blanking	Number of blank columns in a row. Minimum horizontal blanking is 43 columns.	05E (94)	Y	43−1023	W
0X06 (6) VERTICAL BLANKING						
14:0	Vertical Blanking	Number of blank rows in a frame. This number must be equal to or larger than four.	002D (45)	Y	4−3000	W
0X07 (7) CHIP CONTROL						

Table 8. REGISTER DESCRIPTIONS

0X06 (6) VERTICAL BLANKING

2:0	Scan Mode	0 = Progressive scan. 1 = Not valid. 2 = Two−field Interlaced scan. Even−numbered rows are read first, and followed by odd−numbered rows. 3 = Single−field Interlaced scan. If start address is even number, only even−numbered rows are read out; if start address is odd number, only odd−numbered rows are read out. Effective image size is decreased by half.	0	Y	0, 2, 3	W
3	Sensor Master/Slave Mode	0 = Slave mode. Initiating exposure and readout is allowed. 1 = Master mode. Sensor generates its own exp sure and readout timing according to simultaneous/sequential mode control bit.	1	Y	0,1	W
4	Sensor Snapshot Mode	0 = Snapshot disabled. 1 = Snapshot mode enabled. The start of frame is triggered by providing a pulse at EXPOSURE pin. Sensor master/slave mode should be set to logic 1 to turn on this mode.	0	Y	0,1	W
5	Stereoscopy Mode	0 = Stereoscopy disabled. Sensor is stand−alone and the PLL generates a 320 MHz (x12) clock. 1 = Stereoscopy enabled. The PLL generates a 480 MHz (x18) clock.	0	Y	0,1	W
6	Stereoscopic Master/Slave mode	0 = Stereoscopic master. 1 = Stereoscopic slave. Stereoscopy mode should be enabled when using this bit.	0	Y	0,1	W
7	Parallel Output Enable	0 = Disable parallel output. $D_{OUT(9:0)}$ are in High−Z. 1 = Enable parallel output.	1	Y	0,1	W
8	Simultaneous/ Sequential Mode	0 = Sequential mode. Pixel and column readout takes place only after exposure is complete. 1 = Simultaneous mode. Pixel and column readout takes place in conjunction with exposure.	1	Y	0,1	W

0X08 (8) SHUTTER WIDTH 1

14:0	Shutter Width 1	The row number in which the first knee occurs. This may be used only when high dynamic range option (bit 6 of R0x0F) is enabled and exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame.	1BB (443)	N	1−32767	W

0X09 (9) SHUTTER WIDTH 2

14:0	Shutter Width 2	The row number in which the second knee occurs. This may be used only when high dynamic range option (bit 6 of R0x0F) is enabled and exposure knee point auto adjust control bit is disabled. This register is not shadowed, but any change made does not take effect until the following new frame. Shutter width 2 = (bits 14:0) Note: t_1 = Shutter width 1; t_2 = Shutter width 2 − Shutter 1; t_3 = Total integration − Shutter width 2.	1D9 (473)	N	1−32767	W

0X0A (10) SHUTTER WIDTH CONTROL

3:0	T2 Ratio	One−half to the power of this value indicates the ratio of duration time t_2, when saturation control gate is adjusted to level V2 to total integration when exposure knee point auto adjust control bit is enabled. This register is not shadowed, but any change made does not take effect until the following new frame. t_2 = Total integration × $(½)^{t2\_ratio}$.	4	N	0−15	W

Table 8. REGISTER DESCRIPTIONS

0X09 (9) SHUTTER WIDTH 2

7:4	T3 Ratio	One−half to the power of this value indicates the ratio of duration time t_3, when saturation control gate is adjusted to level V3 to total integration when exposure knee point auto adjust control bit is enabled. This register is not shadowed, but any change made does not take effect until the following new frame. t_3 = Total integration × $(½)^{t3\_ratio}$. Note: t_1 = Total integration − t_2 − t_3.	6	N	0−15	W
8	Exposure Knee Point Auto Adjust Enable	0 = Auto adjust disabled. 1 = Auto adjust enabled.	1	N	0,1	W
9	Single Knee Enable	0 = Single knee disabled. 1 = Single knee enabled.	0	N	0,1	W

0X0B (11) TOTAL SHUTTER WIDTH

14:0	Total Shutter Width	Total integration time in number of rows. This value is used only when AEC is disabled only (bit 0 of Register 175). This register is not shadowed, but any change made does not take effect until the following new frame.	1E0 (480)	N	1−32767	W

0X0C (12) RESET

0	Soft Reset	Setting this bit causes the sensor to abandon the current frame by resetting all digital logic except two−wire serial interface configuration. This is a self−resetting register bit and should always read “0.” (This bit de−asserts internal active LOW reset signal for 15 clock cycles.)	0	N	0, 1	W
1	Auto Block Soft Reset	Setting this bit causes the sensor to reset the automatic gain and exposure control logic. This is a self−resetting register bit and should always read “0.” (This bit de−asserts internal active LOW reset signal for 15 clock cycles.)	0	Y	0, 1	W

0X0D (13) READ MODE

1:0	Row Bin	0 = Normal operation. 1 = Row bin 2. Two pixel rows are read per row output. Image size is effectively reduced by a factor of 2 vertically while data rate and pixel clock are not affected. Resulting frame rate is increased by 2. 2 = Row bin 4. Four pixel rows are read per row output. Image size is effectively reduced by a factor of 4 vertically while data rate and pixel clock are not affected. Resulting frame rate is increased by 4. 3 = Not valid.	0	Y	0, 1, 2	W
3:2	Column Bin	0 = Normal operation. 1 = Column bin 2. When set, image size is reduced by a factor of 2 horizontally. Frame rate is not affected but data rate and pixel clock are reduced by one−half that of master clock. 2 = Column bin 4. When set, image size is reduced by a factor of 4 horizontally. Frame rate is not affected but data rate and pixel clock are reduced by one−fourth that of master clock. 3 = Not valid.	0	Y	0, 1, 2	W
4	Row Flip	Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Window Height) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Window Height − 1). This ensures that the starting color is maintained.	0	Y	0, 1	W

Table 8. REGISTER DESCRIPTIONS

0X09 (9) SHUTTER WIDTH 2

5	Column Flip	Read out columns from right to left (mirrored). When set, column readout starts from column (Col Start + Window Width) and continues down to (Col Start + 1). When clear, readout starts at Col Start and continues to (Col Start + Window Width − 1). This ensures that the starting color is maintained.	0	Y	0, 1	W
6	Show Dark Rows	When set, the programmed dark rows is output before the active window. Frame valid is thus asserted earlier than normal. This has no effect on integration time or frame rate. Whether the dark rows are shown in the image or not the definition frame start is before the dark rows are read out.	0	Y	0, 1	W
7	Show Dark Columns	When set, the programmed dark columns are output before the active pixels in a line. Line valid is thus asserted earlier than normal, and the horizontal blank time gets shorter by 18 pixel clocks.	0	Y	0, 1	W
9:8	Reserved	Reserved.	3			

0X0E (14) MONITOR MODE

0	Monitor Mode Enable	Setting this bit puts the sensor into a cycle of sleeping for five minutes, and waking up to capture a programmable number of frames (R0xC0). Clearing this bit resumes normal operation.	0	Y	0, 1	W

0X0F (15) PIXEL OPERATION MODE

2	Color/Mono	Should be set according to sensor type: 0 = Monochrome. 1 = Color.	0	Y	0, 1	W
6	High Dynamic Range	0 = Linear operation. 1 = High Dynamic Range. Voltage and shutter width must be correctly set for saturation control to operate.	0	Y	0, 1	W

0X1B (27) LED_OUT CONTROL

0	Disable LED_OUT	Disable LED_OUT output. When cleared, the output pin LED_OUT is pulsed high when the sensor is undergoing exposure.	0	Y	0, 1	W
1	Invert LED_OUT	Invert polarity of LED_OUT output. When set, the output pin LED_OUT is pulsed low when the sensor is undergoing exposure.	0	Y	0, 1	W

0X1C (28) ADC RESOLUTION CONTROL

1:0	ADC Mode	0 = Invalid. 1 = Invalid. 2 = 10−bit linear. 3 = 12−to10−bit companding.	2	Y	2, 3	W

0X2C (44) VREF_ADC CONTROL

2:0	VREF_ADC Voltage Level	0 = VREF_ADC = 1.0V. 1 = VREF_ADC = 1.1V. 2 = VREF_ADC = 1.2V. 3 = VREF_ADC = 1.3V. 4 = VREF_ADC = 1.4V. 5 = VREF_ADC = 1.5V. 6 = VREF_ADC = 1.6V. 7 = VREF_ADC = 2.1V. Range: 1.0−2.1V; Default: 1.4V VREF_ADC for ADC.	4	N	0−7	W

0X31 (49) V1 CONTROL

4:0	V1 voltage level	V_Step = bits (4:0) x 62.5mV + 0.5625V. Range: 0.5625 − 2.5V; Default: 2.375V. Usage: V_Step1 HiDy voltage.	1D (29)	N	0−31	W

0X32 (50) V2 CONTROL

Table 8. REGISTER DESCRIPTIONS

0X32 (50) V2 CONTROL

4:0	V2 voltage level	V_Step = bits (4:0) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 2.0625V. Usage: V_Step2 HiDy voltage.	18 (24)	N	0–31	W

0X33 (51) V3 CONTROL

4:0	V3 voltage level	V_Step = bits (4:0) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 1.875V. Usage: V_Step3 HiDy voltage.	15 (21)	N	0–31	W

0X34 (52) V4 CONTROL

4:0	V4 voltage level	V_Step = bits (4:0) x 62.5mV + 0.5625V. Range: 0.5625 – 2.5V; Default: 0.8125V. Usage: V_Step HiDy parking voltage, also provides anti–blooming when V_Step is disabled.	4	N	0–31	W

0X35 (53) ANALOG GAIN

6:0	Analog Gain	Analog gain = bits (6:0) x 0.0625 for values 16–31 Analog gain = bits (6:0)/2 x 0.125 for values 32–64 For values 16–31: each LSB increases analog gain 0.0625v/v. A value of 16 = 1X gain. Range: 1X to 1.9375X For values 32–64: each 2 LSB increases analog gain 0.125v/v. Range: 2X to 4X. An LSB increase of 1 will not increase the gain; the value must be incremented by 2 No exception detection is installed and caution should be taken when programming	10 (16)	Y	16–64	W

0X36 (54) MAXIMUM ANALOG GAIN

6:0	Maximum Analog Gain	This register is used by the automatic gain control (AGC) as the upper threshold of gain. This ensures the new calibrated gain value does not exceed that which the MT9V032 supports. Range: 16_{dec}–64_{dec} for 1X–4X respectively. Note: No exception detection is installed; caution should be taken when programming.	40 (64)	Y	16–64	W

0X42 (66) FRAME DARK AVERAGE

7:0	Frame Dark Average	The value read is the frame averaged black level, that is, used in the black level algorithm calculations.	0			R

0X46 (70) DARK AVERAGE THRESHOLDS

7:0	Lower threshold	Lower threshold for targeted black level in ADC LSBs.	1D (29)	N	0–255	W
15:8	Upper threshold	Upper threshold for targeted black level in ADC LSBs.	23 (35)	N	0–255	W

0X47 (71) BLACK LEVEL CALIBRATION CONTROL

0	Manual Override	Manual override of black level correction. 1 = Override automatic black level correction with programmed values. (R0x48). 0 = Normal operation (default).	0	N	0, 1	W
7:5	Frames to average over	Two to the power of this value decide how many frames to average over when the black level algorithm is in the averaging mode. In this mode the running frame average is calculated from the following formula: Running frame ave = Old running frame ave – (old running frame ave)/2n + (new frame ave)/ 2n.	4	N	0–7	W
15:8	Reserved	Reserved.	80 (128)			

0X48 (72) BLACK LEVEL CALIBRATION VALUE

Table 8. REGISTER DESCRIPTIONS

0X48 (72) BLACK LEVEL CALIBRATION VALUE

7:0	Black Level Calibration Value	Analog calibration offset: Negative numbers are represented with two's complement, which is shown in the following formula: Sign = bit 7 (0 is positive, 1 is negative). If positive offset value: Magnitude = bit 6:0. If negative offset value: Magnitude = not (bit 6:0) + 1. During two−wire serial interface read, this register returns the user−programmed value when manual override is enabled (R0x47 bit 0); otherwise, this register returns the result obtained from the calibration algorithm.	0	N	−127 to 127	W

0X4C (76) BLACK LEVEL CALIBRATION VALUE STEP SIZE

4:0	Step Size of Calibration Value	This is the size calibration value may change (positively or negatively) from frame to frame. 1 calib LSB = ½ ADC LSB, assuming analog gain = 1.	2	N	0–31	W

0X70 (112) ROW NOISE CORRECTION CONTROL 1

3:0	Number of Dark Pixels	The number of pixels used in the row−wise noise calculation. 0 = 2 pixels. 1 = 4 pixels. 2 = 6 pixels. 4 = 10 pixels. 8 = 18 pixels. See "Row−wise Noise Correction" for additional information.	4	Y	0, 1, 2, 4, 8	W
4	Reserved	Reserved.	1			
5	Enable noise correction	0 = Normal operation. 1 = Enable row noise cancellation algorithm. When this bit is set, on a per row basis, the dark average is subtracted from each pixel in the row, and then a constant (R0x72) is added.	1	Y	0, 1	W
11	Use black level average	1 = Use black level frame average from the dark rows in the row noise correction algorithm for low gains. This frame average was taken before the last adjustment of the offset DAC for that frame, so it might be slightly off. 0 = Use the average value of the dark columns read out in each row as dark average.	0	Y	0, 1	W

0X72 (114) ROW NOISE CONSTANT

7:0	Row noise constant	Constant used in the row noise cancellation algorithm. It should be set to the dark level targeted by the black level algorithm plus the noise expected between the averaged values of dark columns. At default the constant is set to 42 LSB.	2A (42)	Y	0–255	W

0X73 (115) ROW NOISE CORRECTION CONTROL 2

9:0	Dark start column address	The starting column address for the dark columns to be used in the row−wise noise correction algorithm.	2F7 (759)	Y	759–775	W

0X74 (116) PIXEL CLOCK, FRAME AND LINE VALID CONTROL

0	Invert Line Valid	Invert line valid. When set, LINE_VALID is reset to logic "0" when DOUT is valid.	0	Y	0, 1	W
1	Invert Frame Valid	Invert frame valid. When set, FRAME_VALID is reset to logic "0" when frame is valid.	0	Y	0, 1	W
2	XOR Line Valid	1 = Line valid = "Continuous" Line Valid XOR Frame Valid 0 = Line Valid determined by bit 3. Ineffective if Continuous Line Valid is set.	0	Y	0, 1	W
3	Continuous Line Valid	1 = "Continuous" Line Valid (continue producing line valid during vertical blank). 0 = Normal Line Valid (default, no line valid during vertical blank).	0	Y	0, 1	W