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Power Field Effect Transistor DPAK for Surface Mount

N-Channel Enhancement-Mode Silicon Gate

This Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

Features

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ 0.3 Ω Max
- Rugged SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement V_{GS(th)} = 4.0 V Max
- Surface Mount Package on 16 mm Tape
- Pb-Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 $M\Omega$)	V_{DGR}	150	Vdc
	V _{GS} V _{GSM}	± 20 ± 40	Vdc Vpk
Drain Current – Continuous – Pulsed	I _D I _{DM}	6.0 20	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	20 0.16	W W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C (Note 1)	P _D	1.25 0.01	W W/°C
Total Power Dissipation @ T _A = 25°C (Note 1) Derate above 25°C (Note 2)	P _D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	$egin{array}{l} R_{ hetaJC} \ R_{ hetaJA} \ R_{ hetaJA} \end{array}$	6.25 100 71.4	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using the minimum recommended

1

2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.

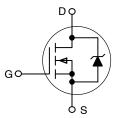


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
150 V	0.3 Ω	6.0 A

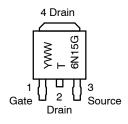
N-CHANNEL





CASE 369C DPAK (Surface Mount) STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



= Year ww = Work Week 6N15 = Device Code = Pb-Free Package

ORDERING INFORMATION

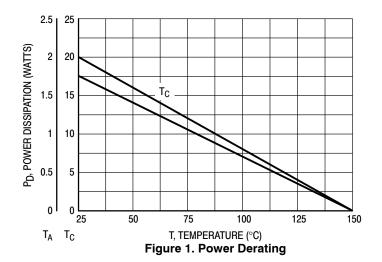
Device	Package	Shipping [†]
MTD6N15T4	DPAK	2500/Tape & Reel
MTD6N15T4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

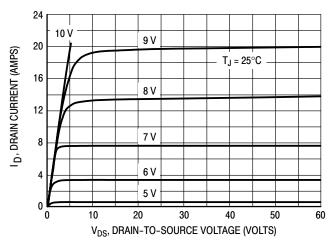
ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic			Min	Max	Unit
OFF CHARACTERISTICS		-1	•		
ain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) V _{(BR)DSS}			150	-	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0 Vdc) T _J = 125°C		I _{DSS}	_ _	10 100	μAdc
Gate-Body Leakage Current, Forwar	d (V _{GSF} = 20 Vdc, V _{DS} = 0)	I _{GSSF}	_	100	nAdc
Gate-Body Leakage Current, Revers	e (V _{GSR} = 20 Vdc, V _{DS} = 0)	I _{GSSR}	_	100	nAdc
ON CHARACTERISTICS (Note 3)		-1	•		
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $T_J = 100^{\circ}C$	I _D = 1.0 mAdc)	V _{GS(th)}	2.0 1.5	4.5 4.0	Vdc
Static Drain-Source On-Resistance	(V _{GS} = 10 Vdc, I _D = 3.0 Adc)	R _{DS(on)}	_	0.3	Ω
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 100°C)			_ _	1.8 1.5	Vdc
Forward Transconductance (V _{DS} = 15	Forward Transconductance (V _{DS} = 15 Vdc, I _D = 3.0 Adc)			-	mhos
DYNAMIC CHARACTERISTICS		-1	•		
Input Capacitance		C _{iss}	-	1200	pF
Output Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz) (See Figure 11)	C _{oss}	_	500	
Reverse Transfer Capacitance		C _{rss}	_	120	
SWITCHING CHARACTERISTICS* (T _J = 100°C)				
Turn-On Delay Time		t _{d(on)}	-	50	ns
Rise Time	$(V_{DD} = 25 \text{ Vdc}, I_D = 3.0 \text{ Adc}, R_G = 50 \Omega)$	t _r	-	180	
Turn-Off Delay Time	(See Figures 13 and 14)	t _{d(off)}	-	200	
Fall Time		t _f	_	100	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} ,	Qg	15 (Typ)	30	nC
Gate-Source Charge	I _D = Rated I _D , V _{GS} = 10 Vdc)	Q _{gs}	8.0 (Typ)	-	
Gate-Drain Charge	(See Figure 12)	Q _{gd}	7.0 (Typ)	-	
SOURCE-DRAIN DIODE CHARACT	ERISTICS*				
Forward On-Voltage		V_{SD}	1.3 (Typ)	2.0	Vdc
Forward Turn-On Time	(I _S = 6.0 Adc, di/dt = 25 A/μs, V _{GS} = 0 Vdc)	t _{on}	Limited by stray inductan		uctance
Reverse Recovery Time	7	t _{rr}	325 (Typ)	_	ns

^{3.} Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



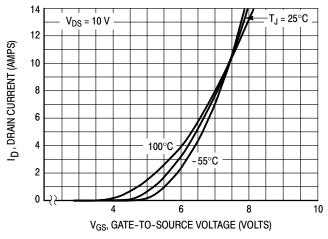
TYPICAL ELECTRICAL CHARACTERISTICS



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Figure 2. On-Region Characteristics

Figure 3. Gate-Threshold Voltage Variation With Temperature



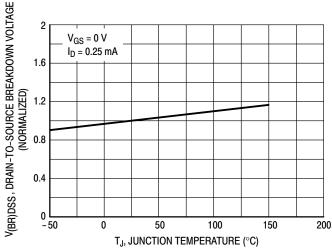
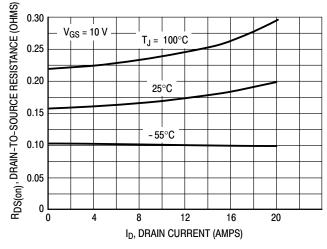


Figure 4. Transfer Characteristics

Figure 5. Breakdown Voltage Variation With Temperature



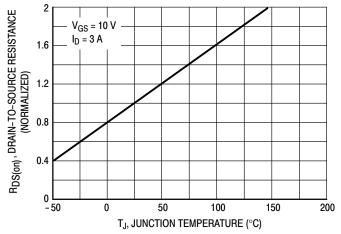


Figure 6. On-Resistance versus Drain Current

Figure 7. On–Resistance Variation With Temperature

SAFE OPERATING AREA

20

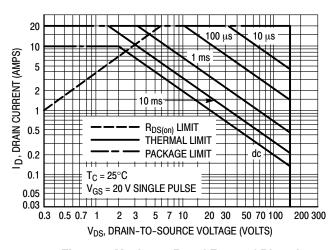


Figure 8. Maximum Rated Forward Biased Safe Operating Area

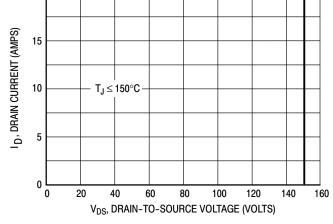


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn—on and turn—off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta,JC}}$$

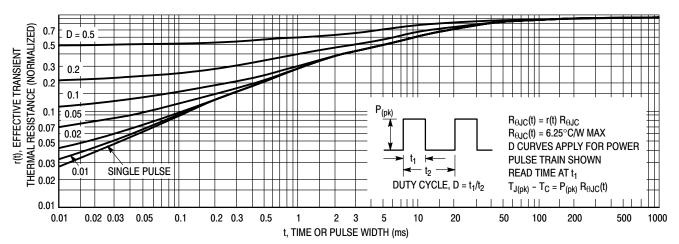
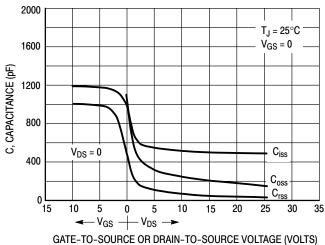


Figure 10. Thermal Response

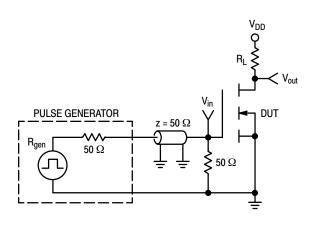


VGS, GATE SOURCE VOLTAGE (VOLTS) $T_J=25^{\circ}C$ $I_D = 6 A$ 12 75 V 120 V $V_{DS} = 50 \text{ V}$ 8 0 4 8 12 16 20 Qg, TOTAL GATE CHARGE (nC)

Figure 11. Capacitance Variation

Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING



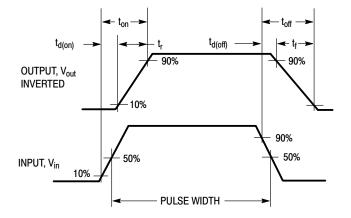


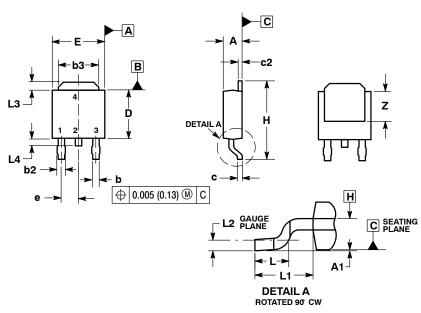
Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)

CASE 369C ISSUE D



NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME
- Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3, L3 and Z.
- MENSIONS D. A3 BID E.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD
 FLASH, PROTRUSIONS, OR BURRS. MOLD
 FLASH, PROTRUSIONS, OR GATE BURRS SHALL
 NOT EXCEED 0.006 INCHES PER SIDE.
- 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

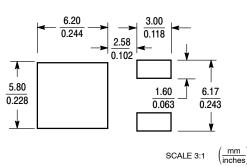
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
е	0.090 BSC		2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

STYLE 2:

- PIN 1. GATE 2. DRAIN

 - SOURCE DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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