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7100 M.2 NVMe PCIe SSD

MTFDHBG400MCG, MTFDHBG800MCG, MTFDHBG480MCH, MTFDHBG960MCH

Features

- Micron® 16nm MLC NAND Flash
- PCIe Gen3: M.2 x4
- NVMe 1.2a
- Capacity[1]
  - 7100 ECO: 480GB, 960GB
  - 7100 MAX: 400GB, 800GB
- Endurance (total bytes written)
  - 400GB/480GB: Up to 5.84PB
  - 800GB/960GB: Up to 11.6PB
- Industry-standard 512-byte and 4096-byte sector size support
- Power: 7W average, selectable 8.25, 6 or 4W MAX
- Power-backed cache
- Steady state performance[2] (varies by capacity)
  - Sequential 128KB read: 2.5 GB/s
  - Sequential 128KB write: 600 MB/s
  - Random 4KB read: 220,000 IOPS
  - Random 4KB write: 33,000 IOPS
  - 70/30 random 4KB read/write: 65,000 IOPS
- Latency to media performance, typical (QD = 1)
  - READ: 110µs, WRITE: 40µs
- Security
  - Signed firmware
  - TCG Opal 2.0-compliant self-encrypting drive (SED) (optional)
  - Compatible with Microsoft eDrive® (optional)
  - Cryptographic erase support (optional)
- Reliability
  - MTBF: 2 million hours[3]
  - Field-upgradable firmware
  - UBER: <1 sector per 10^{17} bits read
- NVMe-MI 1.0 Basic Management Command and Vital Product Data (VPD) over SMBus for drive management
- SMART command set support
- Temperature[4]
  - 0°C to 70°C operating temperature
  - -40°C to 85°C non-operating
  - Temperature protection
- Mechanical/electrical
  - 22.00 x 110.00mm, 3.3V ±5%
- Shock: 1500G at 0.5ms
- Vibration: 3.08 G_{RMS} 7–800Hz

Controller Features

- NVMe controller
  - Number of queues: 16 IO SQ/CQ pairs
  - Round robin arbitration
- Interrupt support coalescing
- NVMe command set attributes
  - Completion queue entry size: 64 bytes
  - Submission queue entry size: 64 bytes

Native Drivers

- Microsoft Windows® Server 2016
- Red Hat® Enterprise Linux 6.5+
- CentOS 6.5+
- SUSE® Linux Enterprise Server 11 SP4, 12+
- Ubuntu® 14.04+
- VMware® 5.5, 6.0+

Custom Drivers

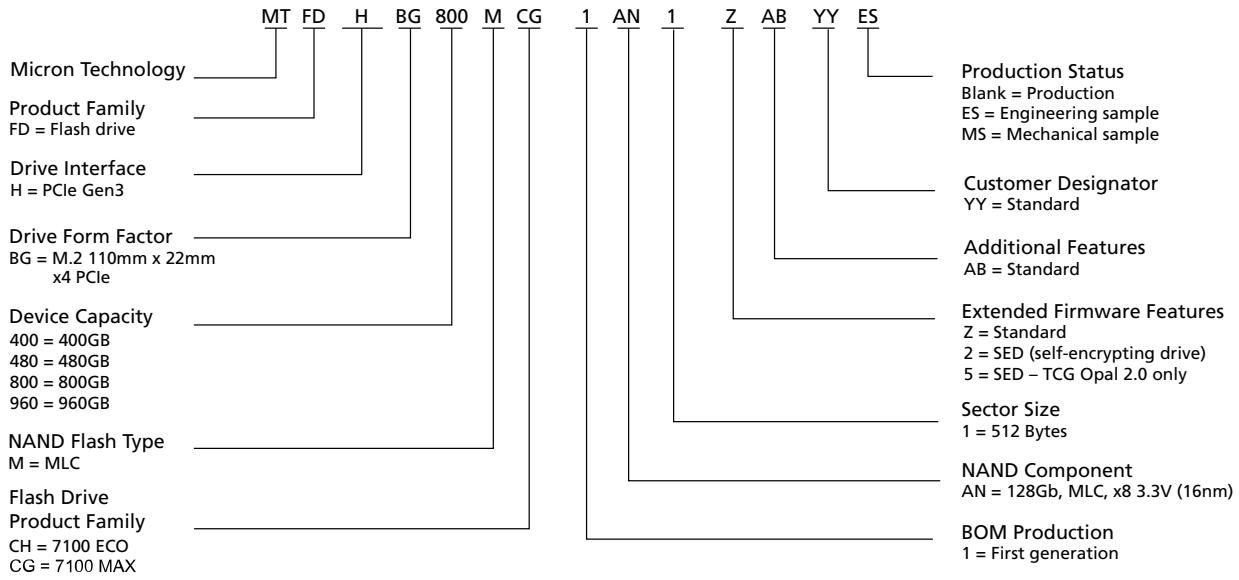
- Microsoft Windows Server 2012 R2, Hyper-V (recommended)
- RHEL 6.1–6.4
- CentOS 6.2–6.4
- SUSE Linux Enterprise Server 11 SP3
- Ubuntu® 12.04

Notes:
1. User capacity: 1GB = 1 billion bytes; 1TB = 1 trillion bytes.
2. Steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
3. See functional description section for more details.
4. Operating temperature is the drive case temperature as measured by the SMART temperature. See airflow recommendations.

Part Numbering Information

The Micron® 7100 SSD is available in different configurations and capacities. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

General Description

Micron's 7100 is a family of low-power NVMe solid state drives (SSDs). The 7100 utilizes a PCIe Gen3 interface, the innovative Non-Volatile Memory Express protocol and Micron's own high-speed NAND to provide exceptional throughput, very low latency, and consistent quality of service within a much lower power envelope than traditional PCIe storage. Its small M.2 form factor provides powerful performance in a very small space, enabling innovative, dense system designs. Reliability assurance measures include cyclic redundancy checks (CRC), capacitor-backed power loss protection and extensive validation, quality and reliability testing. It features thermal monitoring and protection, SMART attributes for status polling and optional self encryption with TCG Opal 2.0.

The device comes in two form factors: M.2 M-Key and 2.5-inch U.2 (small form factor 8639), both of which utilize a PCIe x4 Gen3 host interface. This document covers the M.2 form factor only.

The 7100 has two endurance classes: the 7100 ECO for read-centric use at roughly 0.3 DWPD, and the 7100 MAX for mixed-use workloads at about 3 DWPD. The ECO version comes in 480GB and 960GB capacities, while the 7100 MAX comes in 400GB or 800GB.

Logical Block Address Configuration

The number of logical block addresses (LBAs) reported by the device ensures sufficient storage space for the specified capacity.

Table 1: LBA Count in Accordance with IDEMA LBA1-03

Capacity	512-Byte Sector LBA Count	4KB Sector LBA Count
400GB	781,442,768	97,677,846
480GB	937,703,088	117,212,886
800GB	1,562,824,368	195,353,046
960GB	1,875,385,008	234,423,126

Performance

Table 2: Drive Performance

Specification	7100 ECO		7100 MAX		Unit
	480GB	960GB	400GB	800GB	
Sequential read (128KB I/O size)	2.4	2.5	2.4	2.5	GB/s
Sequential write (128KB I/O size)	475	600	475	600	MB/s
Random read (4KB I/O size)	180,000	220,000	180,000	220,000	IOPS
Random write (4KB I/O size)	10,000	12,000	25,000	33,000	
70/30 mixed workload random read/write (4KB I/O size)	25,000	35,000	55,000	65,000	
Random read latency, QD = 1 (typical)	110				µs
Random write latency, QD = 1 (typical)	40				

Notes:
1. Performance is steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
2. Performance may vary up to 10% over life of drive.
3. Quality of service is measured using random 4KB workloads at steady state with 512B sector size.

Functional Description

Mean Time to Failure

The mean time to failure (MTTF) for the device can be calculated based on the component reliability data using the methods referenced in the Telcordia SR-322 reliability prediction procedures for electronic equipment and measured during Reliability Demonstration Test.

Table 3: MTTF

Capacity	MTTF (Operating Hours)
All	2.0 million

Note: 1. Based on population statistics that are not relevant to individual units, 8760 power on hours per year, 250 power on/off cycles per year, nominal voltages and an environment that does not exceed specified case temperature.

Endurance

SSD endurance is dependent on many factors, including: usage conditions applied to the drive, drive performance and capacity, formatted sector size, error correction codes (ECCs) in use, internal NAND PROGRAM/ERASE cycles, write amplification factor, wear-leveling efficiency of the drive, over-provisioning ratio, valid user data on the drive, drive temperature, NAND process parameters, and data retention time.

The device is designed to operate under a wide variety of conditions, while delivering the maximum performance possible and meeting enterprise market demands.

While actual endurance varies depending on conditions, the drive lifetime can be estimated based on capacity, assumed fixed-use models, ECC, and formatted sector size. Lifetime estimates for the device are shown in the following tables in total bytes written.

Table 4: Total Bytes Written

Model	Capacity	Sequential Writes	Random Writes (4KB)	Unit
7100 ECO	480GB	5.84	0.26	PB
	960GB	11.6	0.52	
7100 MAX	400GB	5.84	2.19	
	800GB	11.6	4.38	

Note: 1. Values shown are based on system modeling.

Data Retention

Data retention refers to the capability of the SSD media (that is, NAND Flash) to retain programmed data. The three primary factors that affect data retention are:

- Power-on/power-off state: Data retention generally improves when the SSD is in use (that is, not shelved in a power-off state).
- Temperature: Data retention decreases as the temperature increases.
- Number of PROGRAM/ERASE cycles on the media: When the SSD ships from the factory, it is typically able to retain user data for up to 5 years in a powered-off state.

Data retention is guaranteed for three months at 40ºC (max), which assumes worst-case power and media wear (the SSD remains in a powered-off state and has reached end of life).

Wear Leveling

The device uses sophisticated wear-leveling algorithms to maximize endurance by distributing PROGRAM/ERASE cycles uniformly across all blocks in the array. Both static and dynamic wear leveling are utilized to optimize the drive's lifespan.

Both types of wear leveling aim to distribute "hot" data away from blocks that have experienced relatively heavy wear. Static wear leveling accomplishes this by moving data that has not been modified for an extended period of time out of blocks which have seen few P/E cycles and into more heavily worn blocks. This frees up fresher blocks for new data while reducing expected wear on tired blocks. Dynamic wear leveling, by contrast, acts on in-flight data to ensure it is preferentially written to the least-worn free blocks rather than those closer to the end of their rated life. These techniques are used together within the controller to optimally balance the wear profile of the NAND array.

Firmware Update Capability

The SSD supports firmware updates as defined by the NVMe specification. Once a download operation completes, an ACTIVATE command must be issued.

Power Loss Subsystem and Rebuild

The SSD supports an unexpected power loss with a power-backed write cache. No user data is lost during an unexpected power loss.

SMBus Sideband Management

The SSD uses the SMBus interface for presenting product data, monitoring drive health, checking drive status before power-up, and error posting.

Two protocols are supported: NVMe Basic Management Command revision 1.0 and Vital Product Data (VPD).

Table 5: Out of Band Management Details

Out of Band Protocol	SMBUS Address	Data	Detailed Structure
Vital Product Data	0xA6	Vital Product Data (VPD)	See the VPD table
NVMe Management Interface 1.0	0x6A	Basic Management Command	See the Basic Management Command table

Note: 1. SMBus addresses will appear at an alternate address in certain tools due the inclusion of direction bit in the SMBus spec.

Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Power Consumption

Specification	Value
Max active power	8.25W
Average power	7.0W
Power State 1 max	6.0W
Power State 2 max	4.0W

Notes:
1. Power varies significantly depending on IO workload.
2. Maximum power is RMS measured over 1ms.

Table 7: Operating Voltage

Electrical Characteristic	Value
Operating voltage	3.3Vdc (±5%)
Max/min rise time	5ms/100µs
Fall time	100ms @ 1A MAX discharge
Inrush current (typical peak)	300mA < 1s
Minimum off time	100ms

Environmental Conditions

Table 8: Temperature and Airflow

Temperature and Airflow	Value	Notes
Operating temperature (as indicated by the SMART temperature attribute)	0°C to 70°C	1
Operating ambient temperature	Ambient: 0°C to 35°C	2
Operating airflow	690 LFM at 35°C ambient	3, 4
Storage temperature	–40°C to 85°C	
Humidity	5% to 95%	

Notes:
1. If NAND temperature exceeds 80°C, performance will be throttled.
2. Temperature of air impinging on the SSD.
3. Airflow must flow along the length of the drive.
4. Airflow is measured upstream of the drive before any acceleration as the air goes around the drive. Assumes no heat sink.

Table 9: Shock and Vibration

Shock and Vibration	Value
Shock (non-operational)	1500G at 0.5ms half-sine
Vibration (non-operational)	3.08 G_{RMS} 7–800Hz

Note:
1. Shock and vibration ratings refer to ability to withstand stress events only. Prolonged or repeated exposure to conditions listed or greater stresses may result in permanent damage to the device. Functional operation of the device under these conditions is not implied. See warranty for more information.

Supported Commands

NVMe Features

The 7100 supports the following mandatory NVMe features, as described in the NVMe specification:

- 01h - Arbitration
- 02h - Power management
- 04h - Temperature threshold
- 05h - (Time limited) error recovery
- 07h - Number of queues
- 08h - Interrupt coalescing
- 09h - Interrupt vector configuration
- 0Bh - Asynchronous event configuration

The following vendor-specific NVMe admin features are also supported:

- C0h - System time
- C1h - Test unit ready
- C2h - Media life left threshold

NVMe Admin Command Set

The 7100 supports the following mandatory NVMe admin commands, as described in the NVMe specification:

- Delete I/O submission queue
- Create I/O submission queue
- Get log page
- Delete I/O completion queue
- Create I/O completion queue
- Identify
- Abort
- Set features
- Get features
- Asynchronous event request
- Firmware activate
- Firmware image download

The following optional NVMe admin commands are also supported:

- Format NVM
- Security send
- Security receive
- Diagnostic send (vendor specific)
- Diagnostic receive (vendor specific)

NVMe I/O Command Set

The 7100 supports the following mandatory NVMe I/O commands, as described in the NVMe specification:

- Flush
- Write
- Read
- Compare

The following optional NVMe I/O commands are also supported:

- Write uncorrectable
- Write zones
- Dataset management (de-allocate/trim only)

Log Pages

The Get Log Page command can be used to retrieve the following mandatory logs:

- 01h - Error information
- 02h - SMART / health information
- 03h - Firmware slot information

The following optional or vendor-specific logs are also supported:

- 05h - Commands supported and effects log
- C0h - Extended SMART attributes

SMART and Health Information

The SSD supports SMART/Health log information as defined in the NVMe specification as well as extended health information. These logs persist through power cycles and reflect lifetime data.

Table 10: SMART/Health Information (Log Identifier 02h)

Bytes	Name	Description
0	Critical warning	Indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to 0, the critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. • Bit 00: If set to 1, the available spare space has fallen below the threshold. • Bit 01: If set to 1, the temperature has exceeded a critical threshold. • Bit 02: If set to 1, the device reliability has been degraded due to significant media-related errors or any internal error that degrades device reliability. • Bit 03: If set to 1, the media has been placed in read-only mode. • Bit 04: If set to 1, the volatile memory backup device has failed. This field is only valid if the controller has a volatile memory backup solution. • Bits 07:05 Reserved
2:1	Temperature	Contains the temperature of the overall device (controller and NVM included) in units of Kelvin. If it exceeds the temperature threshold, an asynchronous event may be issued to the host. For the 7100, the value reported is the case temperature.
3	Available spare	Contains a normalized percentage (0–100%) of the remaining available spare capacity, beginning at 100% and decreasing.
4	Available spare threshold	When the available spare falls below the threshold indicated in this field, an asynchronous event may be issued to the host. The value is indicated as a normalized percentage (0–100%). Threshold is set to 10%.
5	Percentage used	Contains a vendor-specific estimate of the percentage of the device life used based on the actual device usage and the manufacturer's prediction of device life. A value of 100 indicates that the estimated endurance of the device has been consumed, but may not indicate a device failure. Refer to the JEDEC JESD218 standard for SSD device life and endurance measurement techniques.
31:6	Reserved	Reserved
47:32	Data units read	Contains the number of 512-byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data read to 512-byte units.

Table 10: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
63:48	Data units written	Contains the number of 512-byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data written to 512-byte units. For the NVM command set, logical blocks written as part of write operations shall be included in this value. Write uncorrectable commands shall not impact this value.
79:64	Host read commands	Contains the number of read commands issued to the controller.
95:80	Host write commands	Contains the number of write commands issued to the controller.
111:96	Controller busy time	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O completion queue.) This value is reported in minutes.
127:112	Power cycles	Contains the number of power cycles.
143:128	Power on hours	Contains the number of power-on hours. This does not include time that the controller was powered and in a low-power state condition.
159:144	Unsafe shutdowns	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	Media errors	Contains the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field.
191:176	Number of error info log entries	Contains the number of error information log entries over the life of the controller.
511:192	Reserved	Reserved

Out of Band Management

The 7100 allows sideband management using the SMBus and two protocols:

Table 11: Basic Management Command (Address 0x6A)

Command Code	Bytes	Description
0	00	**Length of Status:** Indicates number of additional bytes to read before encountering PEC. Always 6 (06h) in this version of the spec.
	01	**Status Flags (SFLGS):** This field indicates the status of the NVM subsystem. SMBus Arbitration – Bit 7 is set '1' after a SMBus block read is completed all the way to the stop bit without bus contention and cleared to '0' if a SMBus Send Byte FFh is received on this SMBus slave address. Drive Not Ready – Bit 6 is set to '1' when the subsystem cannot process NVMe management commands, and the rest of the transmission may be invalid. If cleared to '0', then the NVM subsystem is fully powered and ready to respond to management commands. This logic level intentionally identifies and prioritizes powered up and ready drives over their powered off neighbors on the same SMBus segment. Drive Functional – Bit 5 is set to '1' to indicate an NVM subsystem is functional. If cleared to '0', then there is an unrecoverable failure in the NVM subsystem and the rest of the transmission may be invalid. Reset Not Required - Bit 4 is set to '1' to indicate the NVM subsystem does not need a reset to resume normal operation. If cleared to '0' then the NVM subsystem has experienced an error that prevents continued normal operation. A controller reset is required to resume normal operation. Port 0 PCIe Link Active - Bit 3 is set to '1' to indicate the first port's PCIe link is up (i.e., the Data Link Control and Management State Machine is in the DL_Active state). If cleared to '0', then the PCIe link is down. Port 1 PCIe Link Active - Bit 2 is set to '1' to indicate the second port's PCIe link is up. If cleared to '0', then the second port's PCIe link is down or not present. Bits 1-0 shall be set to '1'.
	02	**SMART Warnings:** This field shall contain the Critical Warning field (byte 0) of the NVMe SMART / Health Information log. Each bit in this field shall be inverted from the NVMe definition (i.e., the management interface shall indicate a '0' value while the corresponding bit is '1' in the log page). Refer to the NVMe specification for bit definitions. If there are multiple controllers in the NVM subsystem, the management endpoint shall combine the Critical Warning field from every controller such that a bit in this field is: Cleared to '0' if any controller in the subsystem indicates a critical warning for that corresponding bit. Set to '1' if all controllers in the NVM subsystem do not indicate a critical warning for the corresponding bit.

Table 11: Basic Management Command (Address 0x6A) (Continued)

Command Code	Bytes	Description
0	03	Composite Temperature (CTemp): This field indicates the current temperature in degrees Celsius. If a temperature value is reported, it should be the same temperature as the Composite Temperature from the SMART log of hottest controller in the NVM subsystem. The reported temperature range is vendor specific, and shall not exceed the range -60 to +127°C. The 8 bit format of the data is shown below. This field should not report a temperature when that is older than 5 seconds. If recent data is not available, the NVMe management endpoint should indicate a value of 80h for this field. **Value: Description** • 00h-7Eh: Temperature is measured in degrees Celsius (0 to 126C) • 7Fh: 127C or higher • 80h: No temperature data or temperature data is more the 5 seconds old. • 81h: Temperature sensor failure • 82h-C3h: Reserved • C4: Temperature is -60C or lower • C5-FFh: Temperature measured in degrees Celsius is represented in twos complement (-1 to -59C)
	04	**Percentage Drive Life Used (PDLU):** Contains a vendor specific estimate of the percentage of NVM subsystem NVM life used based on the actual usage and the manufacturer's prediction of NVM life. If an NVM subsystem has multiple controllers the highest value is returned. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value should be updated once per power-on hour and equal the Percentage Used value in the NVMe SMART Health Log Page.
	06:05	**Reserved:** Shall be set to 0000h.
	07	**PEC:** An 8 bit CRC calculated over the slave address, command code, second slave address and returned data. Algorithm is in SMBus Specifications.
8	08	**Length of identification:** Indicates number of additional bytes to read before encountering PEC. Always 22 (16h) in this version of the spec.
	10:09	**Vendor ID:** The 2 byte vendor ID, assigned by the PCI SIG. Should match VID in the Identify Controller command response. MSB is transmitted first.
	30:11	**Serial Number:** 20 characters that match the serial number in the NVMe Identify Controller command response. First character is transmitted first.
	31	**PEC:** An 8 bit CRC calculated over the slave address, command code, second slave address and returned data. Algorithm is in SMBus Specifications.
32+	255:32	Vendor Specific

Table 12: Vital Product Data (VPD) (Address 0xA6)

Address	Function	Type	Size (B)	Description
0	Class Code	RO	3	Device type and programming interface
3	ID	RO	2	PCI-SIG Vendor ID
5			20	Serial Number
25			40	Model Number (ASCII string)
65	PCIe Port 0 Capabilities	RO	2	Maximum Link Speed
66				Maximum Link Width
67	PCIe Port 1 Capabilities	RO	2	Maximum Link Speed
68				Maximum Link Width
69	Initial Power Requirements	RO	3	12V power rail initial power requirement (W)
70				Reserved
71				Reserved
72	Maximum Power Requirements	RO	3	12V power rail maximum power requirement (W)
73				Reserved
74				Reserved
75	Capability List Pointer	RO	2	16-bit address pointer to start of capability list (zero means no capability list)

Interface Connectors

M.2 Pin Assignments

The M.2 form factor follows the PCIe M.2 M-Key specification.

Table 13: PCIe Interface Connector Pin Assignments (M.2 Form Factor)

Pin	Name	Description	Pin	Name	Description
74	+3.3V	3.3V power	75	GND	Ground
72	+3.3V	3.3V power	73	GND	Ground
70	+3.3V	3.3V power	71	GND	Ground
68		DNC	69		DNC
		Connector Key	67		DNC
		Connector Key			Connector Key
		Connector Key			Connector Key
		Connector Key			Connector Key
58		DNC			Connector Key
56		DNC	57	GND	Ground
54		DNC	55	REFCLKp	Reference clock p
52	CLKREQ#	Clock request	53	REFCLKn	Reference clock n
50	PERST#	PCIe Fundamental Reset	51	GND	Ground
48		DNC	49	PERp0	PCIe RX Lane 0 p
46		DNC	47	PERn0	PCIe RX Lane 0 n
44	ALERT#	I2C alert	45	GND	Ground
42	SMB_DATA	SMBus data	43	PETp0	PCIe TX Lane 0 p
40	SMB_CLK	SMBus clock	41	PETn0	PCIe TX Lane 0 n
38		DNC	39	GND	Ground
36		DNC	37	PERp1	PCIe RX Lane 1 p
34		DNC	35	PERn1	PCIe RX Lane 1 n
32		DNC	33	GND	Ground
30		DNC	31	PETp1	PCIe TX Lane 1 p
28		DNC	29	PETn1	PCIe TX Lane 1 n
26		DNC	27	GND	Ground
24		DNC	25	PERp2	PCIe RX Lane 2 p
22		DNC	23	PERn2	PCIe RX Lane 2 n
20		DNC	21	GND	Ground
18	+3.3V	3.3V power	19	PETp2	PCIe TX Lane 2 p
16	+3.3V	3.3V power	17	PETn2	PCIe TX Lane 2 n
14	+3.3V	3.3V power	15	GND	Ground
12	+3.3V	3.3V power	13	PERp3	PCIe RX Lane 3 p
10	LED1#	Status indicator for system LED	11	PERn3	PCIe RX Lane 3 n
8		DNC	9	GND	Ground

Table 13: PCIe Interface Connector Pin Assignments (M.2 Form Factor) (Continued)

Pin	Name	Description	Pin	Name	Description
6		DNC	7	PETp3	PCIe TX Lane 3 p
4	+3.3V	3.3V power	5	PETn3	PCIe TX Lane 3 n
2	+3.3V	3.3V power	3	GND	Ground
			1	GND	Ground

PCIe Header

Figure 2: 7100 ECO PCIe Header

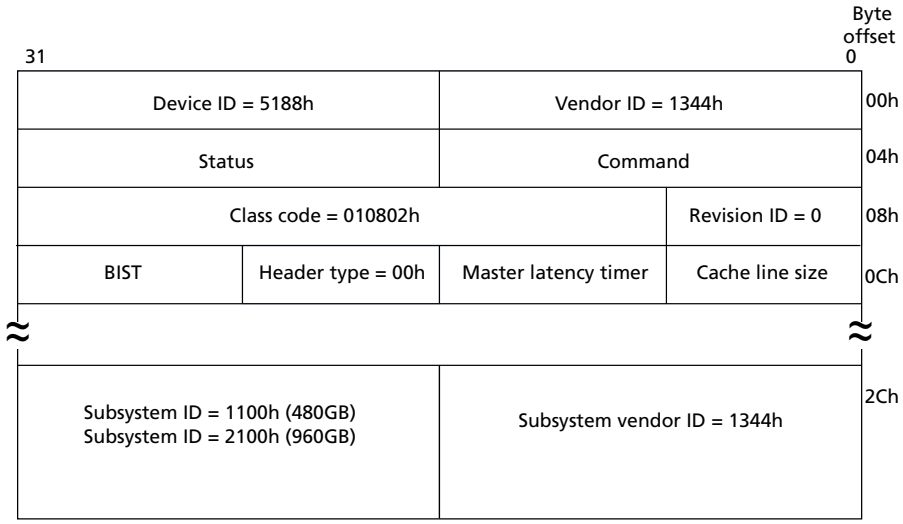
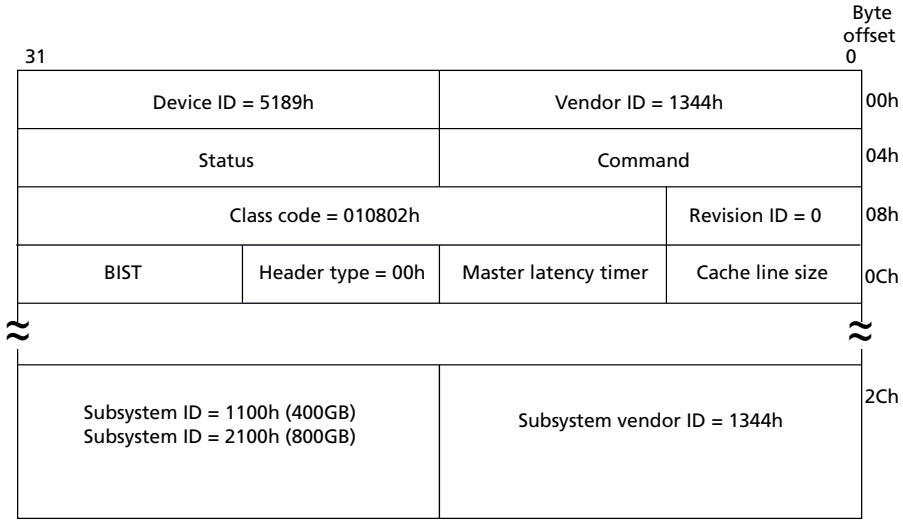


Figure 3: 7100 MAX PCIe Header



Physical Configuration

Micron's 7100 M.2 is a 22110 M-key configuration.

Figure 4: Nominal Dimensions

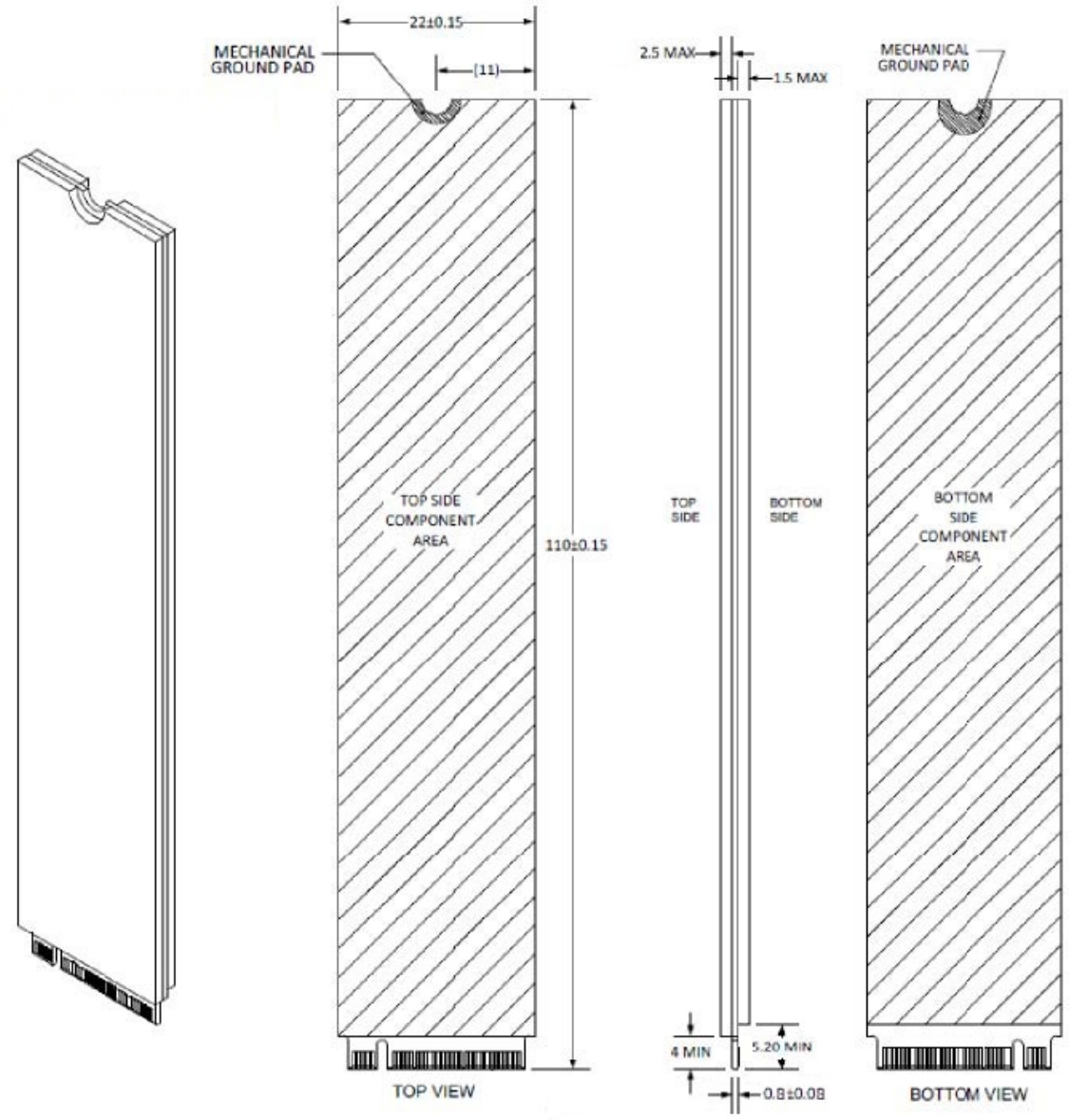
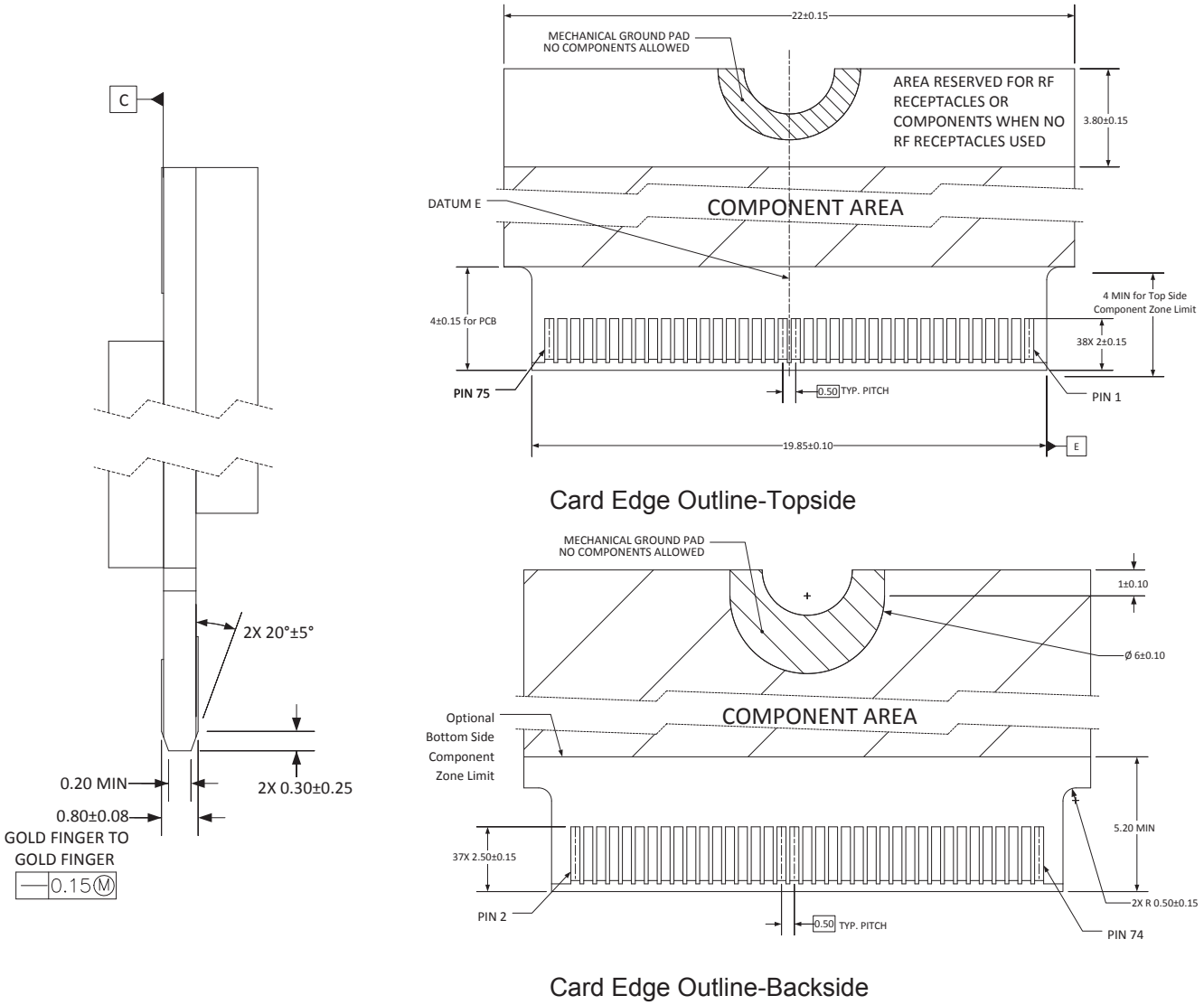


Figure 5: Dimensions Detail



Weight

Product mass: 12 grams.

Compliance

The device complies with the following specifications, if noted on the product label:

- CE (Europe): EN 55032 Class B, RoHS
- FCC: CFR Title 47, Part 15 Class B
- UL/cUL: approval to UL-60950-1, 2nd Edition, IEC 60950-1:2005 (2nd Edition); EN 60950-1 (2006) + A11:2009+ A1:2010 + A12:2011 + A2:2013
- BSMI (Taiwan): approval to CNS 13438 Class B
- RCM (Australia, New Zealand): AS/NZS CISPR32 Class B
- KC RRL (Korea): approval to KN32 Class B, KN 35 Class B

  B 급 기기 (가정용 정보통신기기) 이 기기는 가정용으로 전자파적합등록을한 기기로서 주거 지역에서는 물론 모든지역에서 사용할 수 있습니다.

- W.E.E.E.: compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): approval to IEC60950/EN60950
- VCCI (Japan): 2015-04 Class B

  この装置は、クラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
  取扱説明書に従って正しい取り扱いをして下さい。
  VCCIーB

- IC (Canada): ICES-003 Class B
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

References

- PCI Express Specification V3.0
- PCI Express CEM Specification V1.1
- JESD218
- JESD219
- TCG Storage Architecture Core Specification, Rev. 1.0
- TCG Storage Security Subsystem Class Opal Specification, Rev. 2.00
- NVM Express Specification revision 1.2a

Revision History

Rev. G – 03/17

- Updated TCG Opal references and MPN options.
- Modified power state values.
- Fixed typo on 400GB 4096-byte LBA count in Logical Block Address Configuration table.
- Corrected supported vendor-specific logs.
- Changes to Compliance section.

Rev. F – 07/16

- Fixed typo on 960GB 512-byte LBA count in Logical Block Address Configuration table.

Rev. E – 06/16

- Changes to compliance section.
- Fixed typo in pin assignment table. Pin 38 is DNC.

Rev. D – 05/16

- Corrected typo regarding number of IO SQ/CQ pairs.

Rev. C – 05/16

- Removed note that SMBus can be powered up independently. This does not apply to M.2.
- Corrected typo in product family section of part number chart.

Rev. B – 04/16

- Added part numbers and number scheme information
- Replaced TCG Enterprise reference with TCG Opal
- Latency measurement are taken with 512B sector sizes rather than 4K.
- Noted definition of max power.
- Added SMBus out-of-band management details.
- Updated lists of supported NVMe admin commands, NVMe I/O commands, and log pages. Added NVMe features list.

Rev. A – 03/16

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992