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Panasonic

MTM131270BBF

Silicon P-channel MOS FET

For switching

■ Features

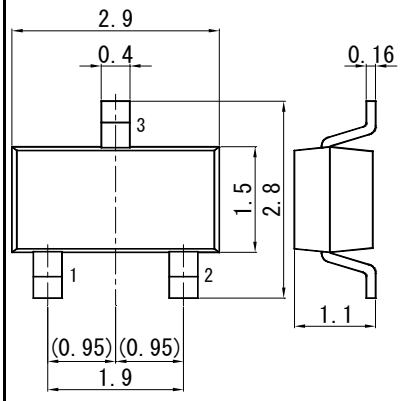
- Low Drain-source On-state Resistance : RDS(on) typ = 92 mΩ (VGS = -4.0 V)
- Low drive voltage: 1.8 V drive
- Halogen-free / RoHS compliant
  (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : EU

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)

Unit : mm



1. Gate
2. Source
3. Drain

Panasonic	Mini3-G3-B
JEITA	SC-59A
Code	TO-236AA/SOT-23

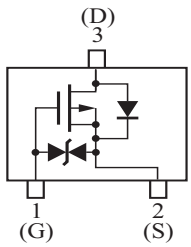
■ Absolute Maximum Ratings Ta = 25 °C

項目	記号	定格	単位
Drain-source Voltage	VDS	-20	V
Gate-source Voltage	VGS	±10	
Drain current	ID	-2	A
Peak drain current *1	IDp	-8	A
Power dissipation *2	PD	700	mW
Channel temperature	Tch	150	°C
Operating ambient temperature	Topr	-40 to + 85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Note *1 Pulse width ≦10 μs, Duty cycle ≦1 %

*2 Measuring on ceramic board at 40 × 38 × 0.1 mm.
Absolute maximum rating PD without heat sink shall be made 200 mW.

Internal Connection



Pin Name

1. Gate
2. Source
3. Drain

Established : 2011-07-19
Revised : 2014-02-03

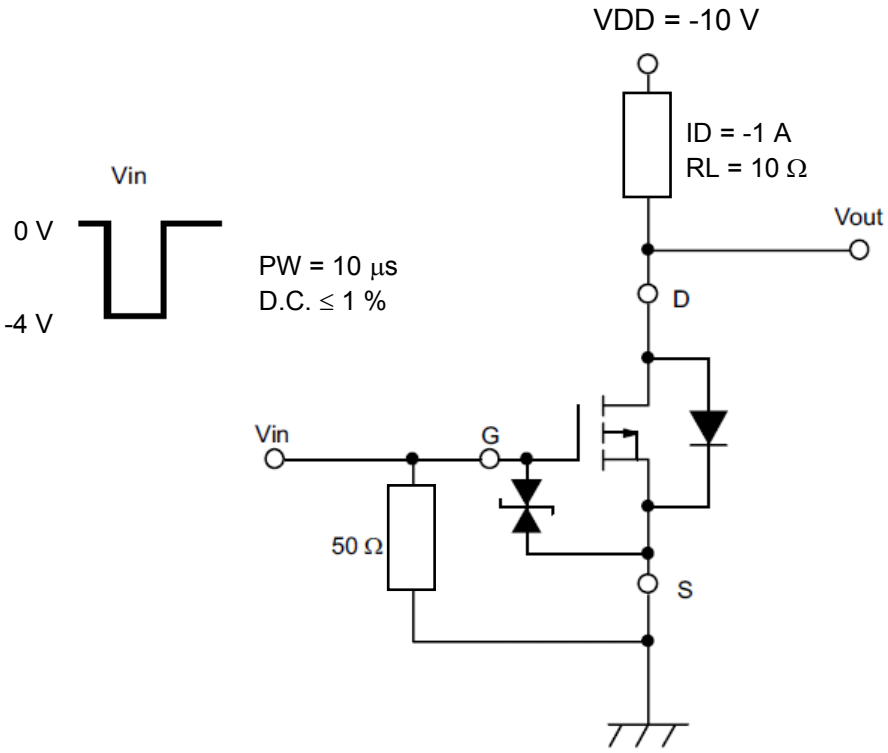
■ Electrical Characteristics Ta = 25 °C ± 3 °C

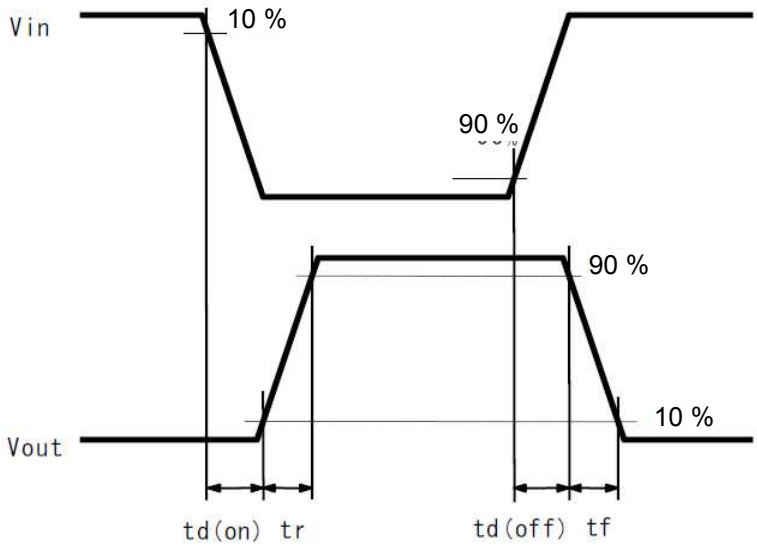
項目	記号	条件	最小	標準	最大	単位
Drain-source surrender voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Drain-source cutoff current	IDSS	VDS = -20 V, VGS = 0 V			-1	μA
Gate-source cutoff current	IGSS	VGS = ±8 V, VDS = 0 V			±10	
Gate threshold voltage	Vth	ID = -1 mA, VDS = -10 V	-0.4	-0.75	-1.1	V
Drain-source ON resistance *1	RDS(on)1	ID = -1 A, VGS = -4 V		92	130	mΩ
	RDS(on)2	ID = -1 A, VGS = -2.5 V		115	210	
	RDS(on)3	ID = -0.5 A, VGS = -1.8 V		161	280	
Forward transfer admittance *1	|Yfs|	ID = -1 A, VDS = -10 V, f = 1 kHz	3			S
Short-circuit input capacitance (Common source)	Ciss	VDS = -10 V, VGS = 0 V f = 1 MHz		300		pF
Short-circuit output capacitance (Common source)	Coss			30		
Reverse transfer capacitance (Common source)	Crss			35		
Turn-on Delay Time *2	td(on)	VDD = -10 V, VGS = 0 to -4 V ID = -1 A		6		ns
Rise Time *2	tr			8		
Turn-off Delay Time *2	td(off)	VDD = -10 V, VGS = -4 to 0 V ID = -1 A		57		
Fall Time *2	tf			55		

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
2. *1 Pulse test
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Established : 2011-07-19
Revised : 2014-02-03

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

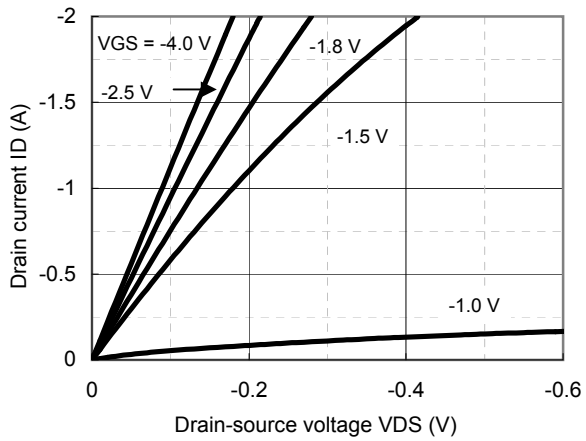




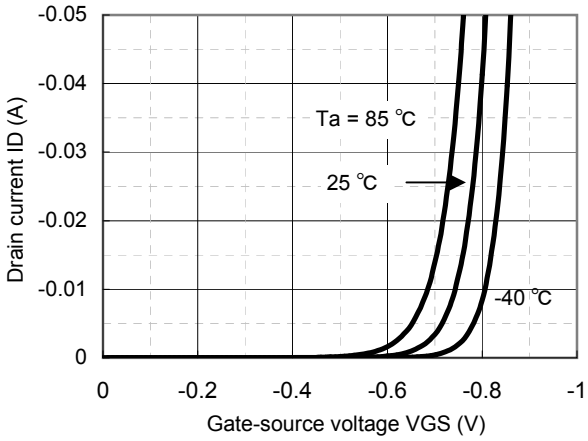
Established : 2011-07-19
Revised : 2014-02-03

Technical Data (reference)

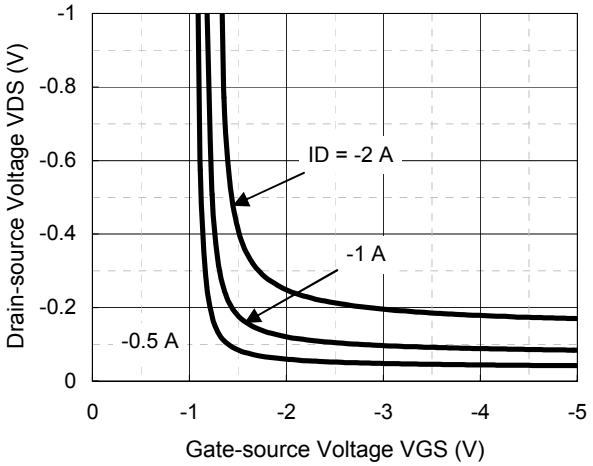
ID - VDS



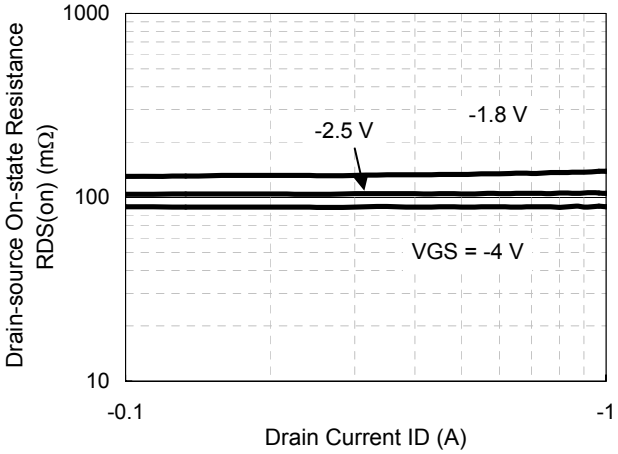
ID - VGS



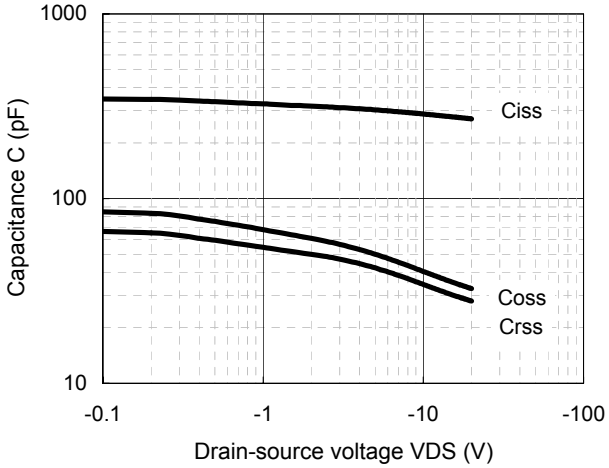
VDS - VGS



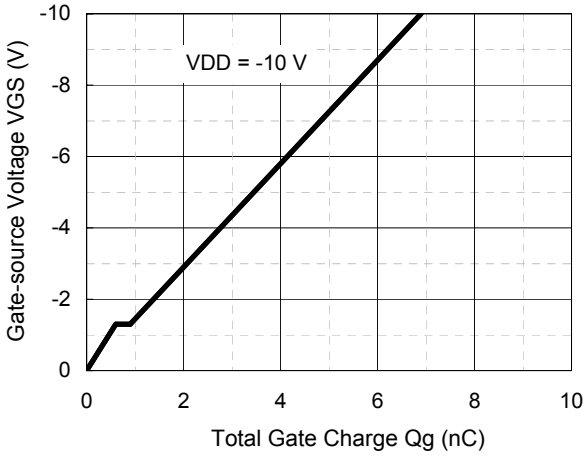
RDS(on) - ID



Capacitance - VDS



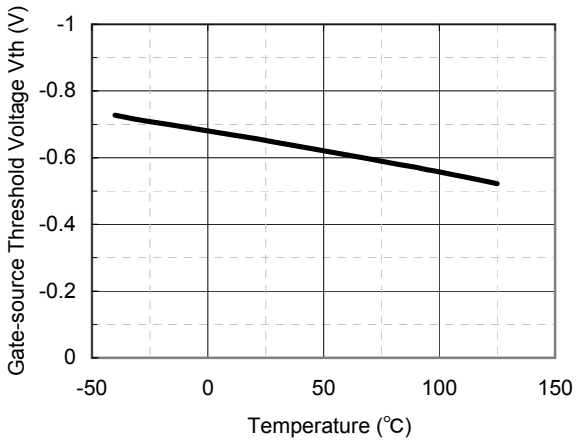
Dynamic Input/Output Characteristics



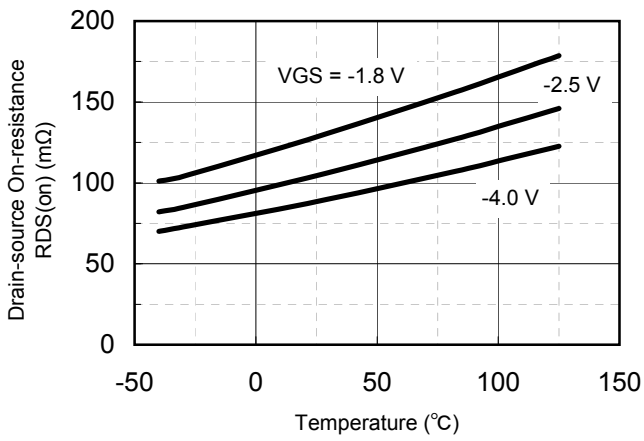
Established : 2011-07-19
Revised : 2014-02-03

Technical Data (reference)

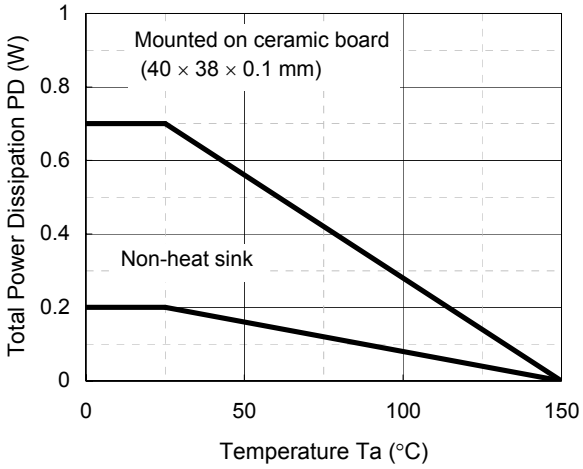
Vth - Ta



RDS(on) - Ta

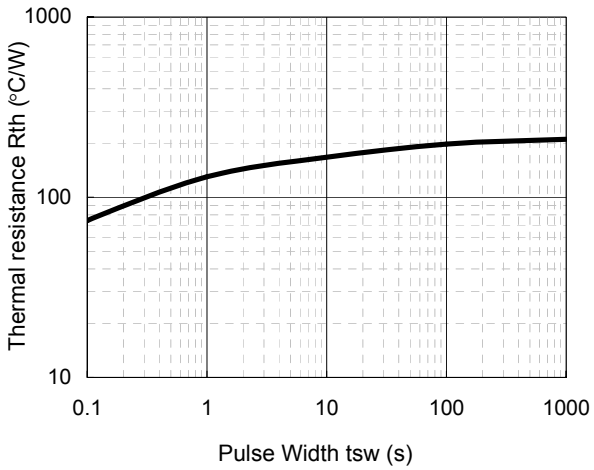


PD - Ta

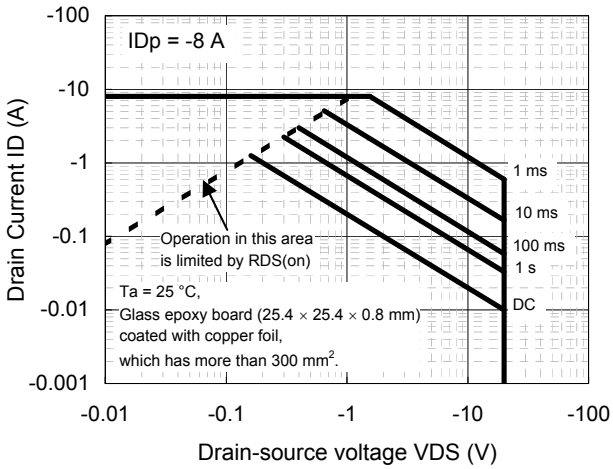


PD - Tc

Rth - tsw



Safe Operating Area



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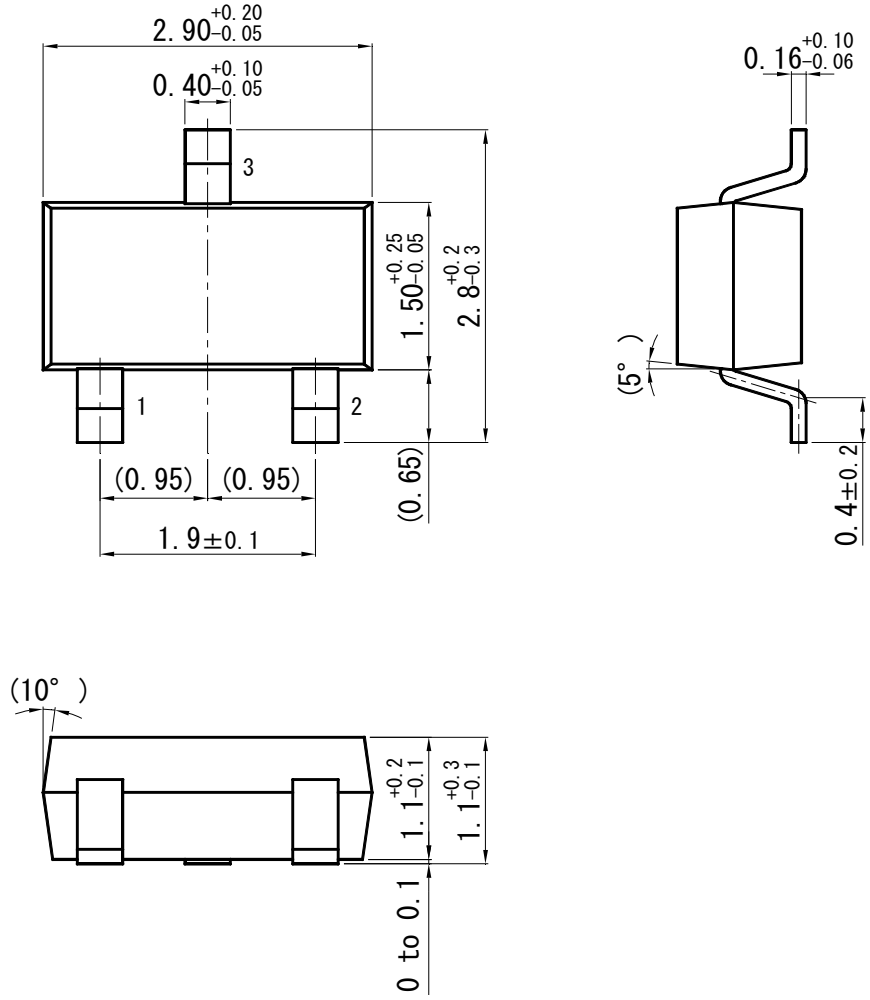
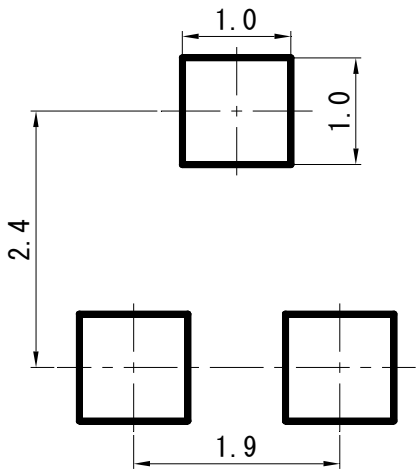
Revised : 2014-02-03

Mini3-G3-B

Unit: mm



■ Land Pattern (Reference) (Unit : mm)



Established : 2011-07-19
Revised : 2014-02-03

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