imall

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Panasonic

MTM861280LBF

MOS FET MTM861280LBF

Silicon P-channel MOSFET

For Switching

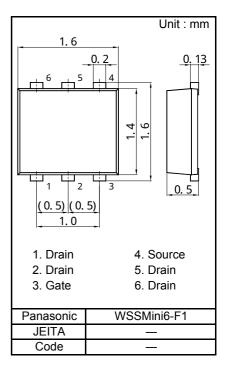
Features

- Low drain-source On-state Resistance : RDS(on) typ. = 300 m Ω (VGS = -4.0 V)
- Halogen-free / RoHS compliant
 (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : ML

Packaging

Embossed type (Thermo-compression sealing): 10 000 pcs / reel (standard)



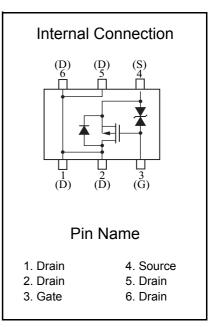
■ Absolute Maximum Ratings Ta = 25 °C

	0			
Parameter	Symbol	Rating	Unit	
Drain to Source Voltage	VDS	-20	V	
Gate to Source Voltage	VGS	±12		
Drain Current	ID	-1.0	Α	
Drain Current (Pulsed) *1	IDp	-4.0	A	
Total Power Dissipation	PD1 *2	540	mW	
	PD2 *3	150		
Channel Temperature	Tch	150		
Operating Ambient Temperature	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150		
Note) $*1$ t < 10 us Duty cycle < 1 %				

Note) *1 t \leq 10 μ s, Duty cycle \leq 1 %

*2 Glass epoxy substrate (25.4 \times 25.4 \times t 0.8 mm) coated with copper foil (more than 300 mm²)

*3 Non-heat sink



Panasonic

MOS FET MTM861280LBF

■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1.0 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±10 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = -1.0 mA, VDS = -10 V	-0.45	-1.0	-1.5	V
Drain-source On-state Resistance *1	RDS(on)1	ID = -0.5 A, VGS = -4.0 V		300	420	mΩ
	RDS(on)2	ID = -0.5 A, VGS = -2.5 V		420	560	
Forward transfer admittance ^{*1}	Yfs	ID = -0.5 A, VDS = -10 V	1.0	2.0		S
Input Capacitance	Ciss			80		pF
Output Capacitance	Coss	VDS = -10 V, VGS = 0 V f = 1 MHz		12		
Reverse Transfer Capacitance	Crss			12		
Turn-on Delay Time *2	td(on)	VDD = -15 V, VGS = 0 to -4 V		12		20
Rise Time ^{*2}	tr	ID = -0.5 A		6		ns
Turn-off Delay Time *2	td(off)	VDD = -15 V, VGS = -4 to 0 V		17		ns
Fall Time *2	tf	ID = -0.5 A		10		

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Pulse test

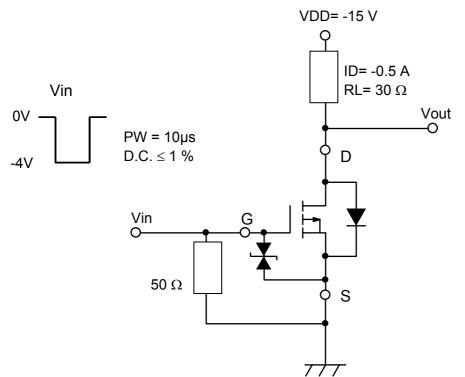
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

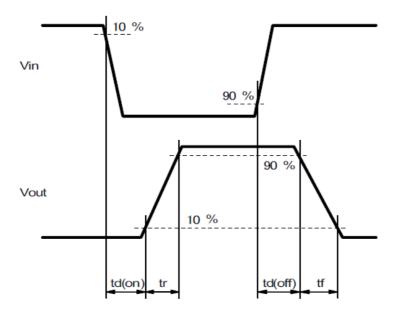
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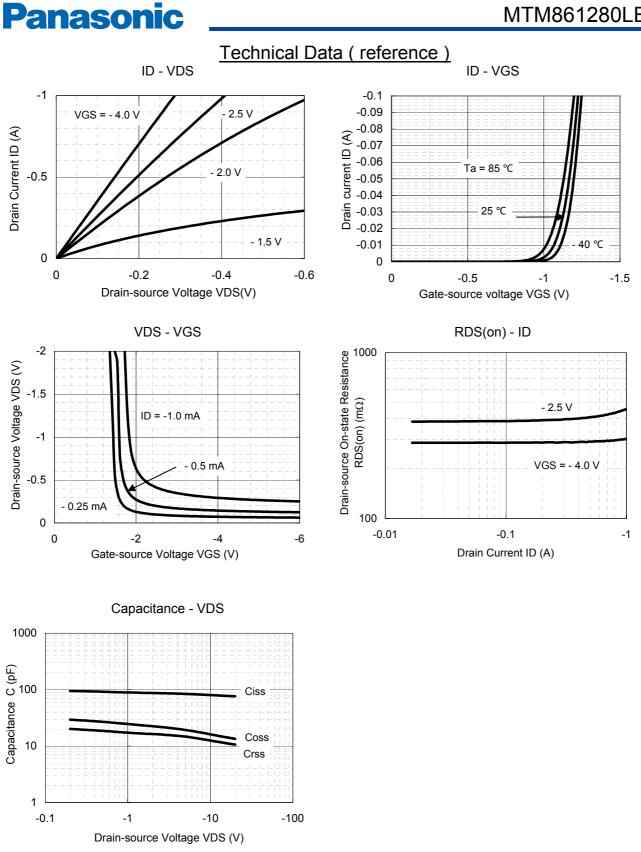
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time





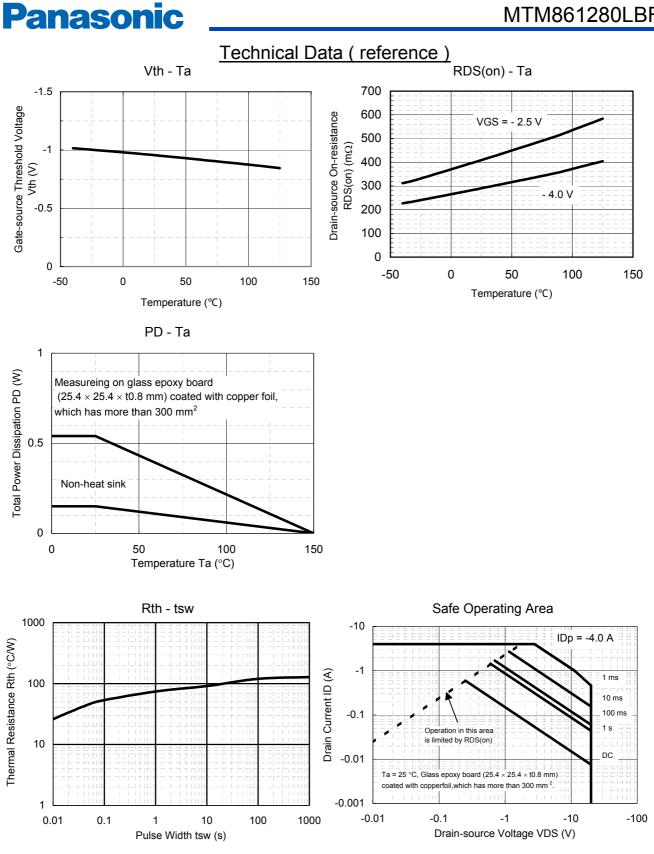
Established : 2010-02-04 Revised : 2013-10-17

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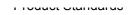
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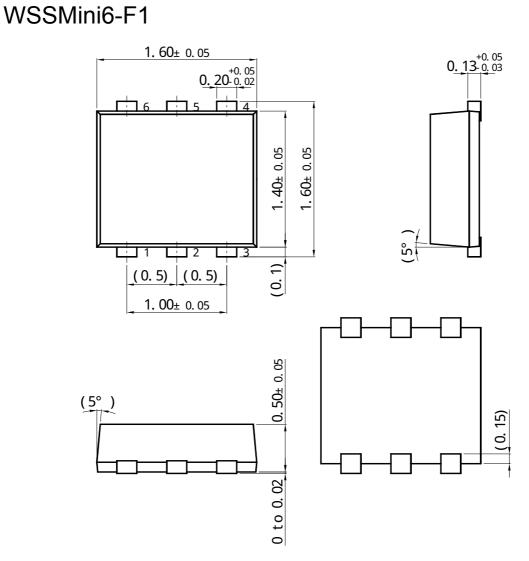
Established : 2010-02-04 Revised : 2013-10-17



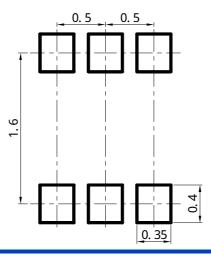
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Unit : mm



■ Land Pattern (Reference) (Unit : mm)



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