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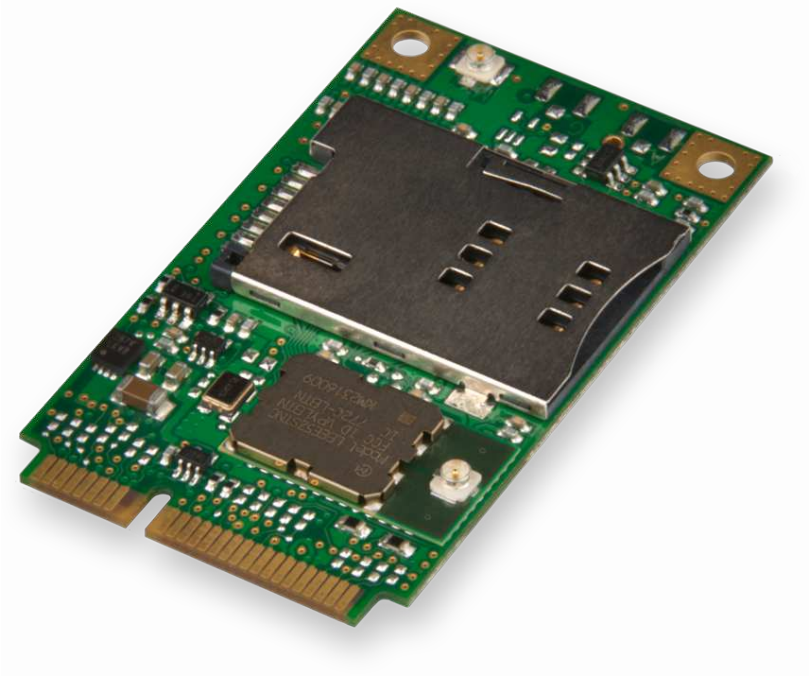

MultiConnect® PCIe

MTPCIE-H5/MTPCIE-BW Developer Guide

MultiConnect PCIe Developer Guide

Models: MTPCIE-H5-xx, MTPCIE-H5-V-BW, MTPCIE-BW

Part Number: S000572, Version 1.4 European Edition

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Knowledge Base

The Knowledge Base provides immediate access to support information and resolutions for all MultiTech products. Visit http://www.multitech.com/kb.go.

Support Portal

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Support

Business Hours: M-F, 8am to 5pm CT

Country	By Email	By Phone
Europe, Middle East, Africa:	support@multitech.co.uk	+(44) 118 959 7774
U.S., Canada, all others:	support@multitech.com	(800) 972-2439 or (763) 717-5863

Warranty

To read the warranty statement for your product, visit www.multitech.com/warranty.go. For other warranty options, visit www.multitech.com/es.go.

World Headquarters

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Fax (763) 785-9874

Contents

Chapter 1 – Product Overview

About MultiConnect PCIe

The MultiConnect™ PCIe embedded cellular modem is a complete, ready-to-integrate communications device that offers standard-based seven-band HSPA+ 21 CDMA performance. This quick-to-market communications device allows developers to add wireless communication and GPS tracking to products with a minimum of development time and expense. The MultiConnect PCIe embedded cellular modem is based on industry-standard open interfaces and utilizes a PCI Express Mini Card form factor.

Documentation

Download the following documentation at www.multitech.com/setup/product.go.

Document	Description
MultiConnect PCIe Developer Guide	This document. Provides an overview, safety and regulatory information, developer board schematics and pinouts, and device.
USB Driver Installation Guide	Provides instructions for installing USB drivers on Linux and Windows systems (part number S000553)(part number S000569).
HSPA+ AT Commands Reference Guide	Configure the MTPCIE-H5 with HSPA+ AT Commands (part number S000574).
EV-DO and CDMA AT Commands Reference Guide	Configure the MTPCIE-C2 with CDMA AT Commands (part number S000546).

Documentation

The following documentation is available by email to oemsales@multitech.com ,

- **MultiConnect PCIe Developer Guide** - Provides an overview, safety and regulatory information, design considerations, schematics, and device information.
- **AT Command Guide** - Use S000528, HSPA+ H5 AT Command Reference Guide.

Product Build Options

Product	Description
MTPCIE-H5-V-BW-EU	HSPA+ Embedded Cellular Modem with digital voice, GPS, Wi-Fi and Bluetooth
MTPCIE-H5-EU	HSPA+ Embedded Cellular Modem
MTPCIE-BW	Wi-Fi and Bluetooth
Developer Kit	
MTPCIE-DK	Developer Kit

Note:

- These units ship without network activation.
- To connect them to the cellular network, you need a cellular account. For more information, refer to Account Activation.

- GP devices have a dedicated GPS receiver.
- The complete product code may end in .Rx. For example, MTPCIE-H5.Rx, where R is revision and x is the revision number.
- All builds can be ordered individually or in 50-packs.

Developer Kit Contents

Your Developer Kit (MTPCIE-DK1) includes the following:

Developer Board	1 - MTPCIE-DK1 Developer Board
Power Supply	1 - 100-240V 9V-1.7A power supply with removable blades, 1 - US blade/plug, 1 - EURO blade/plug, 1 - UK blade/plug
Cables	1 - RS-232 DE9F-DE9M serial cable, 1 - RJ-45 Ethernet cable, 2 -USB cable 2 - SMA-to-UFL antenna cables (1 - for cellular, 1 - for GPS) 1 - RSMA-to-UFL antenna cable for Bluetooth/Wi-Fi.
Antennas	1 - 3.3V magnetic GPS antenna , 1 - HEPTA band SMA antenna, 1 - 2.4GHz, dipole Wi-Fi antenna
Customer Notices	Legal and Support information
Additional	One promotional screwdriver

Chapter 2 – Pinout

Multi-Tech Mini PCIe Pinout

Note:

Some modems do not include all the pins.

SDIO can operate up to 25Mhz. Treat the SDIO traces to Host like a bus and keep the bus length as short as possible. Multi-Tech recommends adding series termination resistors on all the SDIO traces.

Pin #	Name	I/O	Function	MTPCIE-H5	MTPCIE-H5-V-BW	MTPCIE-BW
1	SDIO_D0	I/O	Wi-Fi SDIO_D0		X	X
2	3.3Vaux	I	3.3Vaux	X	X	X
3	SDIO_D1	I/O	Wi-Fi SDIO_D1		X	X
4	GND		Ground	X	X	X
5	SDIO_D2	I/O	Wi-Fi SDIO_D2		X	X
6	BT_TXD	I	Bluetooth Transmit data		X	X
7	SDIO_D3	I/O	Wi-Fi SDIO_D3		X	X
8	BT_RTS	I	Bluetooth RTS		X	X
9	GND		Ground	X	X	X
10	BT_CTS	O	Bluetooth CTS		X	X
11	SDIO_CMD	I/O	Wi-Fi SDIO_CMD		X	X
12	BT_RXD	O	Bluetooth Receive data		X	X
13	SDIO_CLK	I	Wi-Fi SDIO_CLK		X	X
14	BT_EN	I	Bluetooth enable (low disable)		X	X
15	GND		Ground	X	X	X
16	GPIO_2	I/O	3G Cellular General purpose I/O		X	
17	WLAN_EN	I	Wi-Fi enable (low disable)		X	X
18	GND		Ground	X	X	X
19	WLAN_IRQ	O	Wi-Fi interrupt (low active)		X	X
20	3G_ONOFF	I	3G Cellular On/Off (low active)	X	X	
21	GND		Ground	X	X	X

Pin #	Name	I/O	Function	MTPCIE-H5	MTPCIE-H5-V-BW	MTPCIE-BW
22	3G_RST	I	3G Cellular Reset line (low active)	X	X	
23	1.8V	O	1.8V output		X	X
24	3.3Vaux	I	3.3Vaux	X	X	X
25	GPIO_1	I/O	Bluetooth General purpose I/O		X	X
26	GND		Ground	X	X	X
27	GND		Ground	X	X	X
28	3G_DVI_WA0	I/O	3G Cellular digital voice control line		X	
29	GND		Ground	X	X	X
30	3G_DVI_CLK	I/O	3G Cellular digital voice clock		X	
31	3G_DVI_RX	I	3G Cellular digital voice receive		X	
32	RI	O	3G Cellular UART RI		X	
33	3G_DVI_TX	O	3G Cellular digital voice transmit		X	
34	GND		Ground	X	X	X
35	GND		Ground	X	X	X
36	USB_D-	I/O	3G USB Negative Data	X	X	
37	GND		Ground	X	X	X
38	USB_D+	I/O	3G USB Positive Data	X	X	
39	3.3Vaux	I	3.3Vaux	X	X	X
40	GND		Ground	X	X	X
41	3.3Vaux	I	3.3Vaux	X	X	X
42	LED_WWAN#	O	3G Cellular STAT LED Output	X	X	
43	GND		Ground	X	X	X
44	DCD	O	3G Cellular UART DCD		X	
45	CTS	O	3G Cellular UART CTS		X	
46	GPIO_3	I/O	3G Celllular General purpose I/O		X	
47	RTS	I	3G Cellular UART RTS		X	
48	DTR	I	3G Cellular UART DTR		X	

Pin #	Name	I/O	Function	MTPCIE-H5	MTPCIE-H5-V-BW	MTPCIE-BW
49	RXD	O	3G Cellular UART Receive data		X	
50	GND		Ground	X	X	X
51	TXD	I	3G Cellular UART transmit data		X	
52	3.3Vaux	I	3.3Vaux	X	X	X

Standard Mini-PCI Express Pinout

For reference only.

Pin #	Function	I/O	Description
1	WAKE#	O	WAKE
2	3.3Vaux	I	3.3Vaux
3	COEX1	I	Co-existence pin, not defined
4	GND		GND
5	COEX2	I	Co-existence pin, not defined
6	1.5V	I	1.5V
7	CLKREQ#	O	CLKREQ#
8	UIM_PWR	I	UIM_PWR
9	GND		GND
10	UIM_DATA	I/O	UIM_DATA
11	REFCLK+	I	PCI Express reference clock
12	UIM_CLK	I	UIM_CLK
13	REFCLK-	I	PCI Express reference clock
14	UIM_RESET	I	UIM_RESET
15	GND		GND
16	UIM_VPP	0	UIM_VPP
17	Reserved		Reserved
18	GND		GND
19	Reserved		Reserved
20	W_DISABLE#	I	W_DISABLE#
21	GND		GND
22	PERST#	I	PERST#
23	PERn0	O	PCI Express receiver differential pair signal
24	3.3Vaux	I	3.3Vaux
25	PERp0	O	PCI Express receiver differential pair signal
26	GND		GND
27	GND		GND
28	1.5V	I	1.5V
29	GND		GND
30	SMB_CLK	I	SMB_CLK
31	PETn0	I	PCI Express transmitter differential pair signal

Pin #	Function	I/O	Description
32	SMB_DATA	I/O	SMB_DATA
33	PETp0	I	PCI Express transmitter differential pair signal
34	GND		GND
35	GND		GND
36	USB_D-	I/O	USB Negative Data
37	GND		GND
38	USB_D+	I/O	USB Positive Data
39	3.3Vaux	I	3.3Vaux
40	GND		GND
41	3.3Vaux	I	3.3Vaux
42	LED_WWAN#	O	LED Output
43	GND		GND
44	LED_WLAN#	O	LED Output
45	Reserved		Reserved
46	LED_WPAN#	O	LED Output
47	Reserved		Reserved
48	1.5V	I	1.5V
49	Reserved		Reserved
50	GND		GND
51	Reserved		Reserved
52	3.3Vaux	I	3.3Vaux

Pinout for Cellular USB Only

Pin #	Name	I/O	Description
2	3.3 Vaux	I	3.3 Vaux
4	GND		Ground
9	GND		Ground
15	GND		Ground
18	GND		Ground
20	3G_ONOFF	I	3G cellular on/off
21	GND		Ground
22	3G_RST	I	3G cellular reset line
24	3.3 Vaux	I	3.3 Vaux
26	GND		Ground
27	GND		Ground
29	GND		Ground
35	GND		Ground
36	USB_D-	I/O	3G USB Negative Data
37	GND		Ground
38	USB_D+	I/O	3G USB Positive Data
39	3.3 Vaux	I	3.3 Vaux
40	GND		Ground
41	3.3 Vaux	I	3.3 Vaux
42	LED_WWAN	O	3G Cellular STAT LED Output
43	GND		Ground
50	GND		Ground
52	3.3 Vaux	I	3.3 Vaux

Chapter 3 – Design Considerations

Design Consideration

When using the Multi-Tech MiniPCIe form factor:

- Consult your modem's device guide for device dimensions. With the modem, the Multi-Tech Mini PCIe form factor exceeds the standard Mini PCIe maximum component height for top and bottom.
- If you need to install components under the module, use taller connectors to avoid conflict. Multi-Tech recommends not installing components under the module.
- Check the Pinout table for pins that differ from the MiniPCIe spec.

Noise Suppression Design

Adhere to engineering noise-suppression practices when designing a printed circuit board (PCB). Noise suppression is essential to the proper operation and performance of the modem and surrounding equipment.

Any OEM board design must consider both on-board and off-board generated noise that can affect digital signal processing. Both on-board and off-board generated noise that is coupled on-board can affect interface signal levels and quality. Noise in frequency ranges that affect modem performance is of particular concern.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is equally important. This type of noise can affect the operation of surrounding equipment. Most local government agencies have certification requirements that must be met for use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, and so on) component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

Other aspects of proper noise-suppression engineering practices are beyond the scope of this guide. Consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes.

PC Board Layout Guideline

In a 4-layer design, provide adequate ground plane covering the entire board. In 4-layer designs, power and ground are typically on the inner layers. Ensure that all power and ground traces are 0.05 inches wide.

The recommended hole size for the device pins is 0.036 in. +/-0.003 in. in diameter. Use spacers to hold the device vertically in place during the wave solder process.

All creepages and clearances for the device meet requirements of safety standards listed in the technical specifications. The requirements are based on a working voltage of 125V or 250V. When implementing the recommended DAA* circuit interface in a third party design, strictly follow all creepage and clearance requirements to meet safety standards. The third party safety design must be evaluated by the appropriate national agency according to the required specification.

User Accessible Areas

Based on where the third party design is marketed, sold, or used, it may be necessary to provide an insulating cover over all TNV exposed areas. Consult with the recognized safety agency to determine the requirements.

Note: Even if the recommended design considerations are followed, there are no guarantees that a particular system complies with all the necessary regulatory requirements. Make sure a qualified and recognized agency evaluates specific designs. .

*DAA stands for Data Access Arrangement. DAA is the device's telephone line interface.

Electromagnetic Interference

The following guidelines are offered specifically to help minimize EMI generation. Some of these guidelines are the same as, or similar to, the general guidelines. To minimize the contribution of device-based design to EMI, you must understand the major sources of EMI and how to reduce them to acceptable levels.

- Keep traces carrying high frequency signals as short as possible.
- Provide a good ground plane or grid. In some cases, a multilayer board may be required with full layers for ground and power distribution.
- Decouple power from ground with decoupling capacitors as close to the device's power pins as possible.
- Eliminate ground loops, which are unexpected current return paths to the power source and ground.
- Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.
- Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
- Locate cables and connectors to avoid coupling from high frequency circuits.
- Lay out the highest frequency signal traces next to the ground grid.
- If using a multilayer board design, make no cuts in the ground or power planes and be sure the ground plane covers all traces.
- Minimize the number of through-hole connections on traces carrying high frequency signals.
- Avoid right angle turns on high frequency traces. Forty-five degree corners are good; however, radius turns are better.
- On 2-layer boards with no ground grid, provide a shadow ground trace on the opposite side of the board to traces carrying high frequency signals. This will be effective as a high frequency ground return if it is three times the width of the signal traces.
- Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

Electrostatic Discharge Control

Handle all electronic devices with precautions to avoid damage due to the static charge accumulation.

See the ANSI/ESD Association Standard (ANSI/ESD S20.20-1999) – a document “for the Development of an Electrostatic Discharge Control for Protection of Electrical and Electronic Parts, Assemblies and Equipment.” This document covers ESD Control Program Administrative Requirements, ESD Training, ESD Control Program Plan Technical Requirements (grounding/bonding systems, personnel grooming, protected areas, packaging, marking, equipment, and handling), and Sensitivity Testing.

MultiTech strives to follow these recommendations. Input protection circuitry is incorporated in MultiTech devices to minimize the effect of static buildup. Take precautions to avoid exposure to electrostatic discharge during handling.

MultiTech uses and recommends that others use anti-static boxes that create a faraday cage (packaging designed to exclude electromagnetic fields). MultiTech recommends that you use our packaging when returning a product and when you ship your products to your customers.

USB Design

MultiTech recommends that you review Intel's High Speed USB Platform Design Guidelines for information about USB signal routing, impedance, and layer stacking. Also:

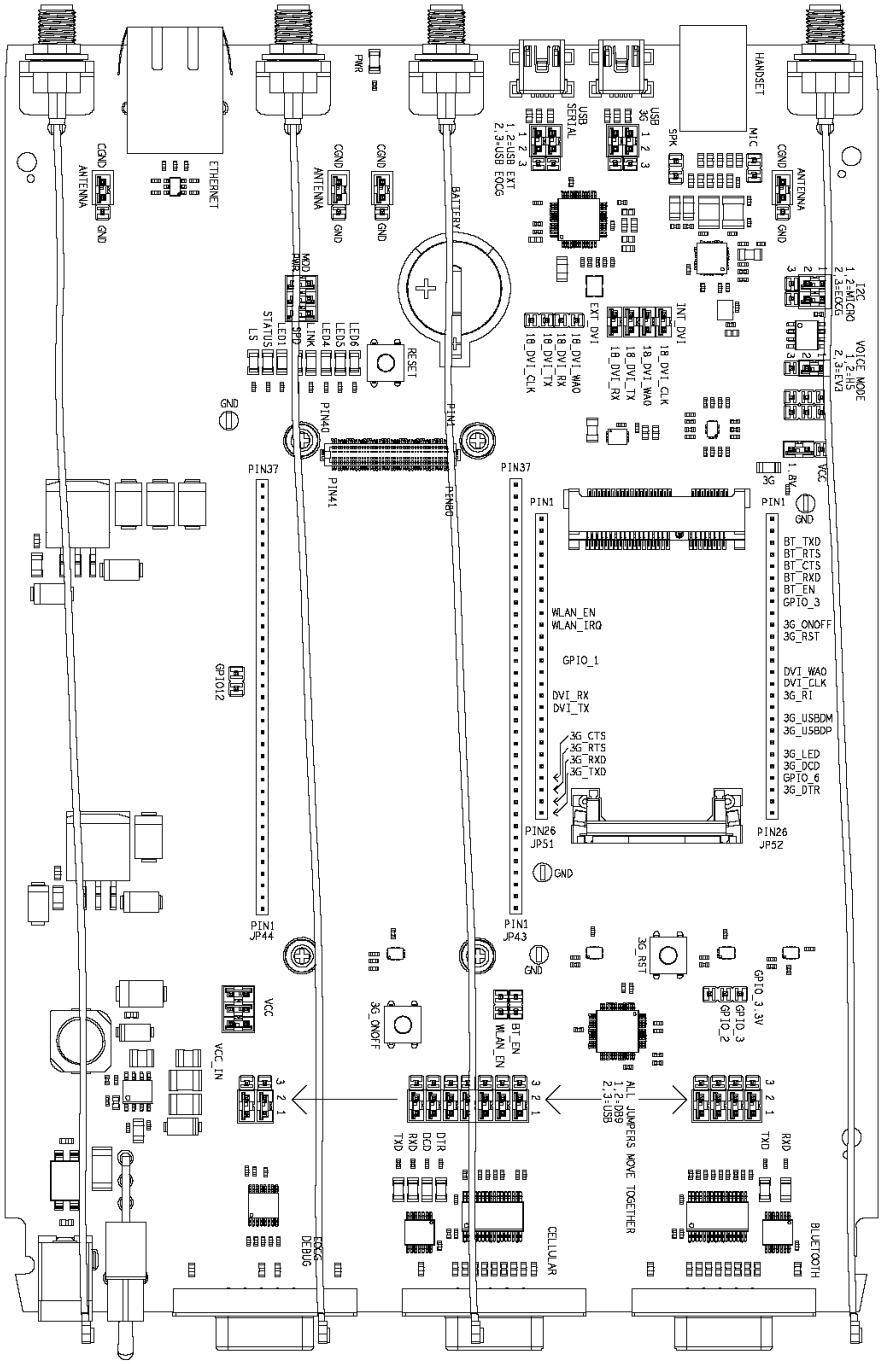
- Shield USB cables with twisted pairs (especially those containing D+/D-).
- Use a single 5V power supply for USB devices. See Power Draw for current (ampere) requirements.
- Route D+/D- together in parallel with the trace spacing needed to achieve 90 ohms differential impedance for the USB pair and to maintain a 20 mil space from the USB pair and all other signals.
- If power is provided externally, use a common ground between the carrier board and the device.

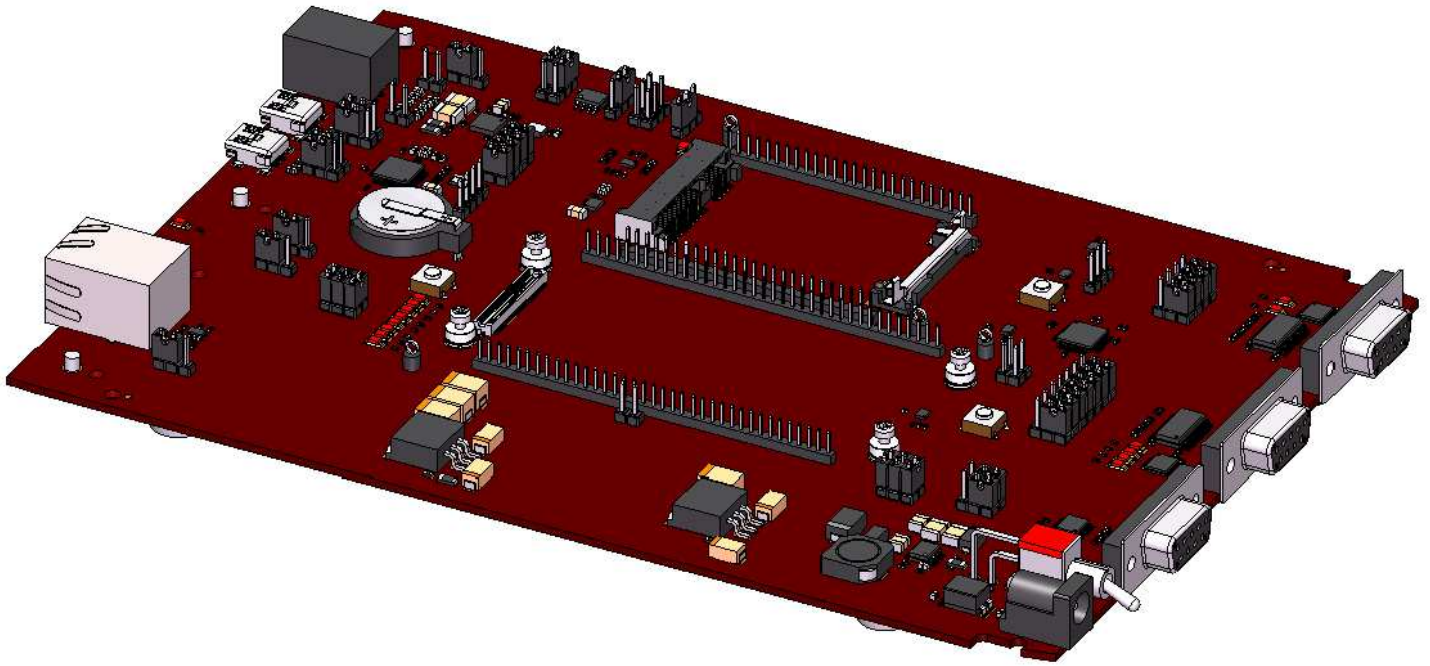
Chapter 4 – Developer Board and Schematics

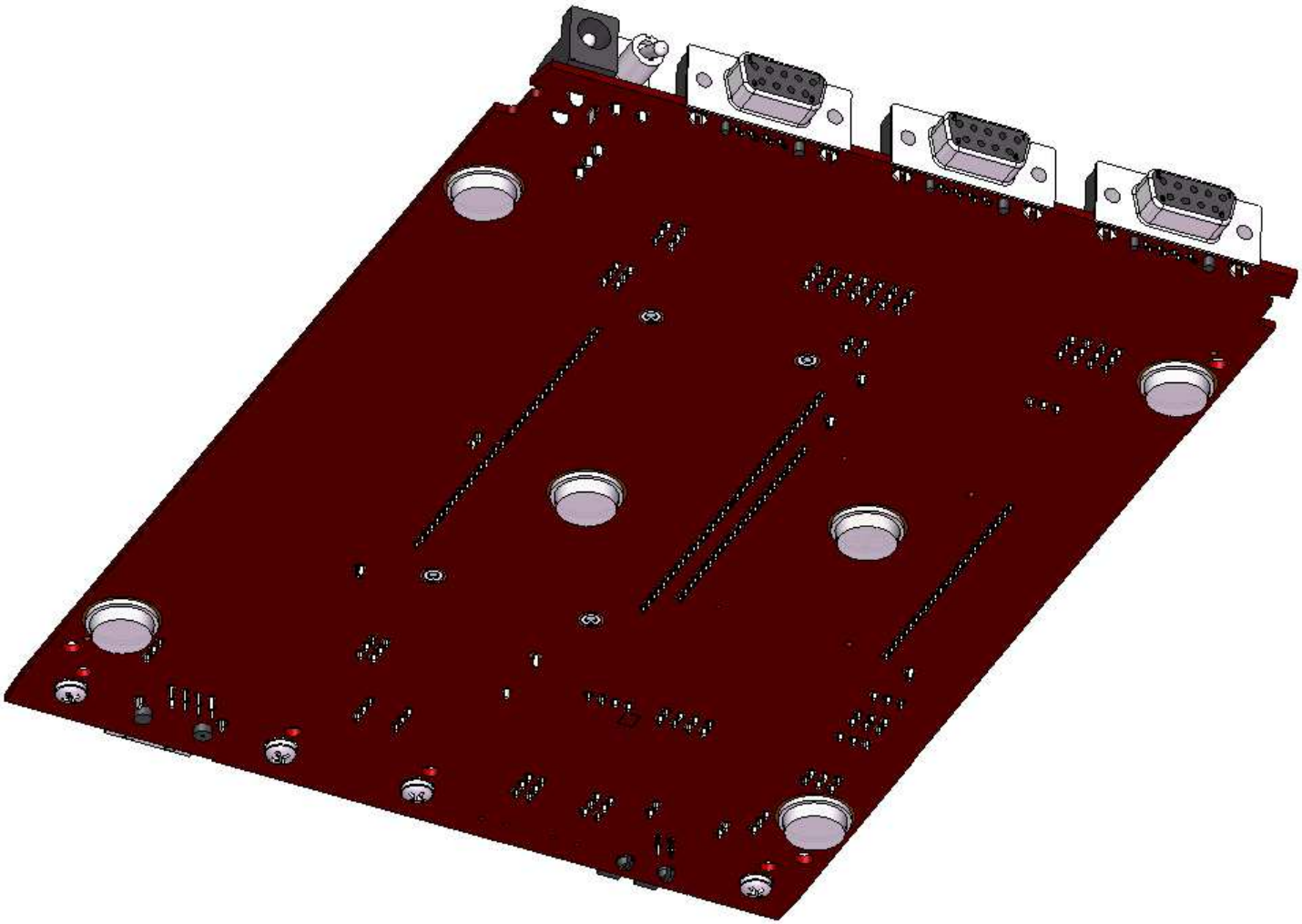
Note: Third-party components shown in the following drawings are included as examples only.

Developer Board

This developer board drawing shows the major board components.

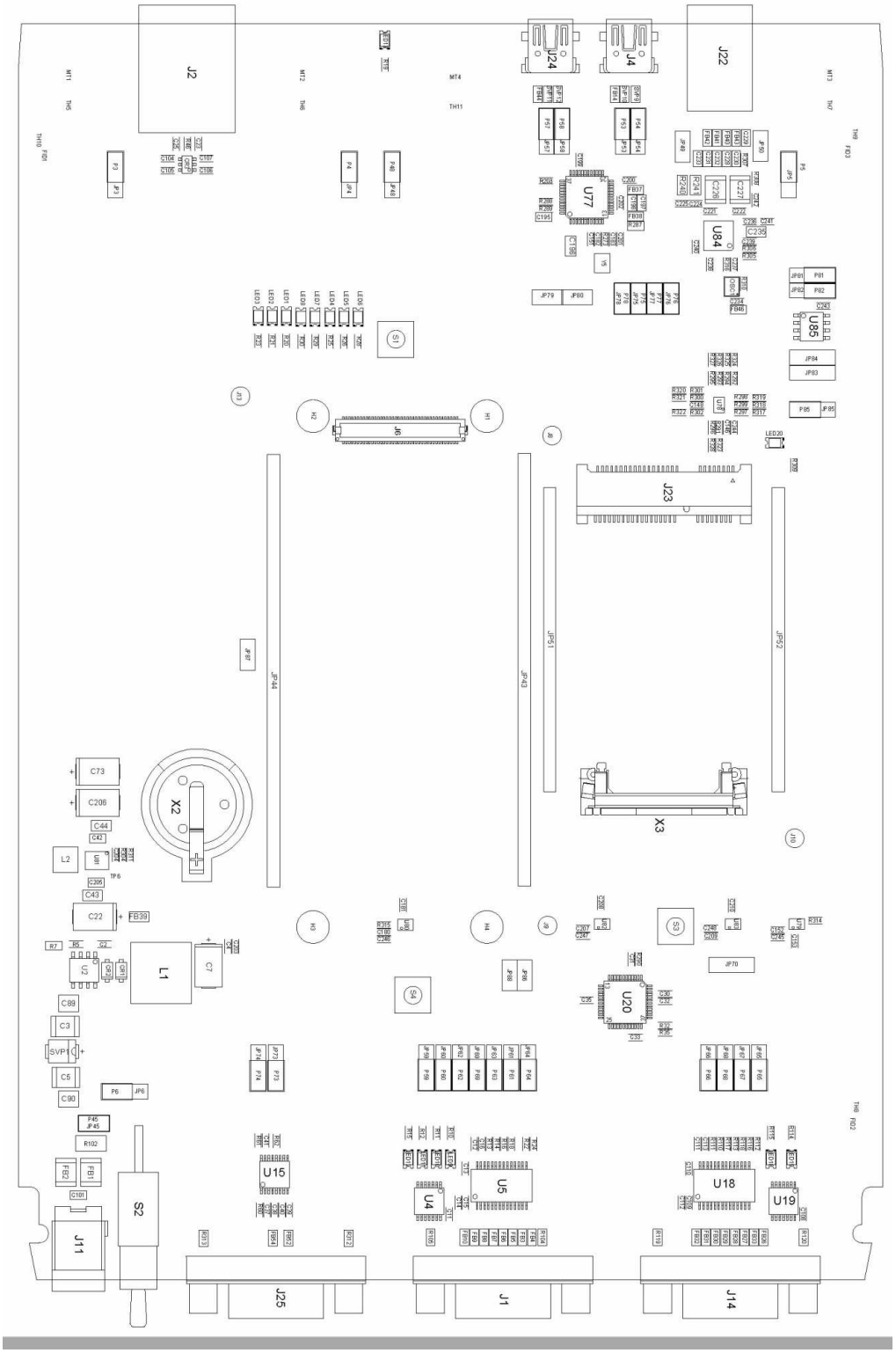




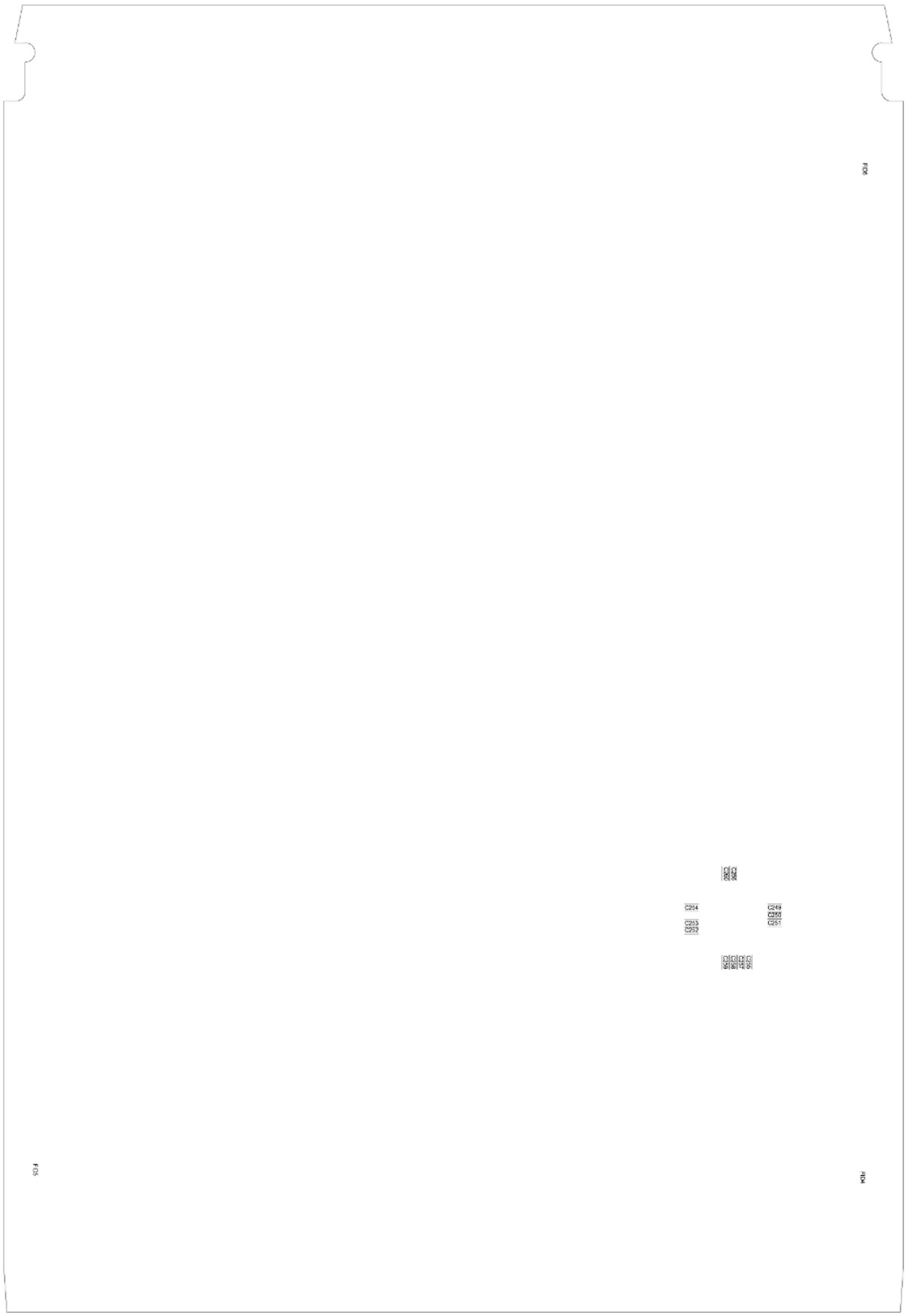


Assembly Diagram

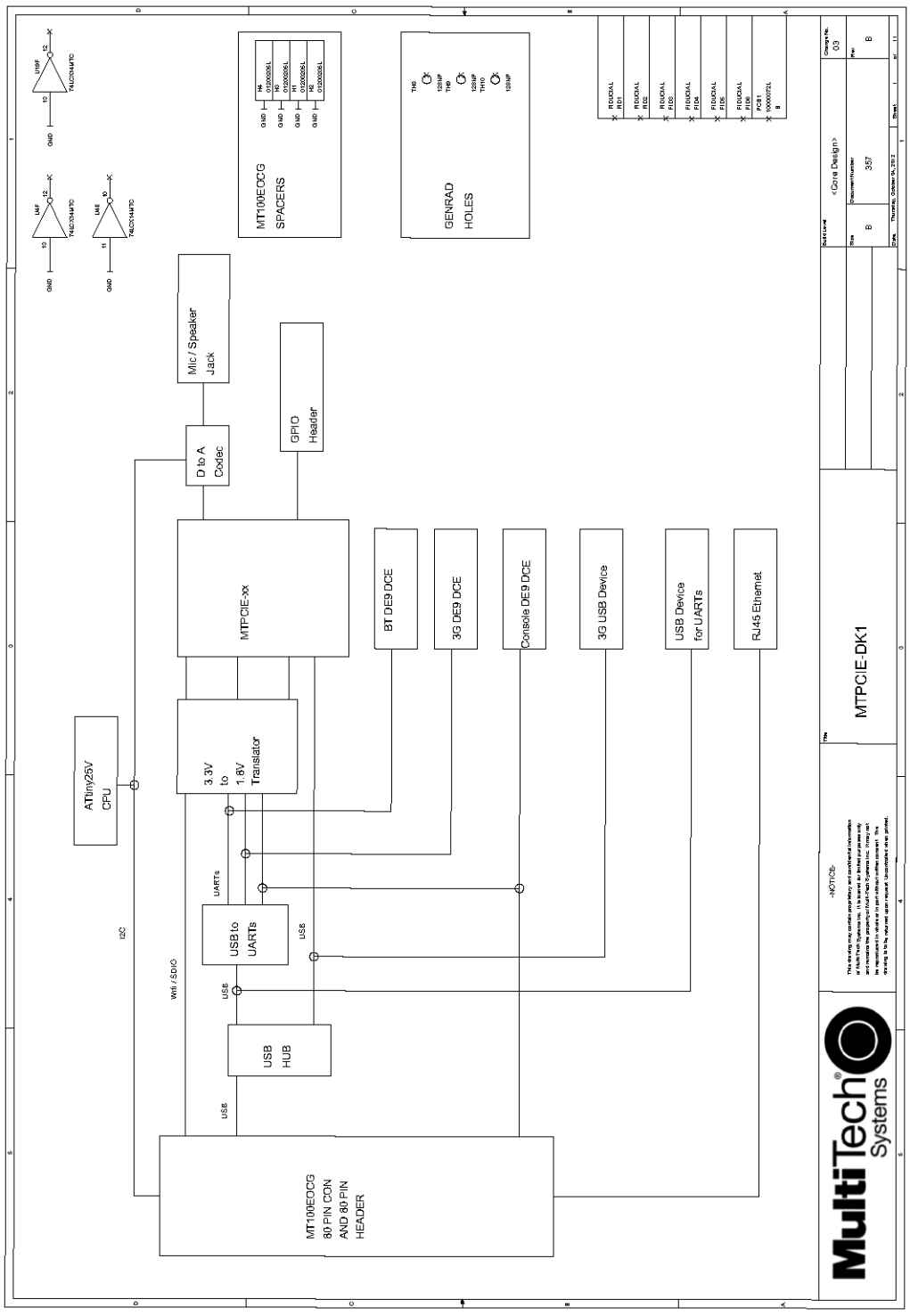
Top



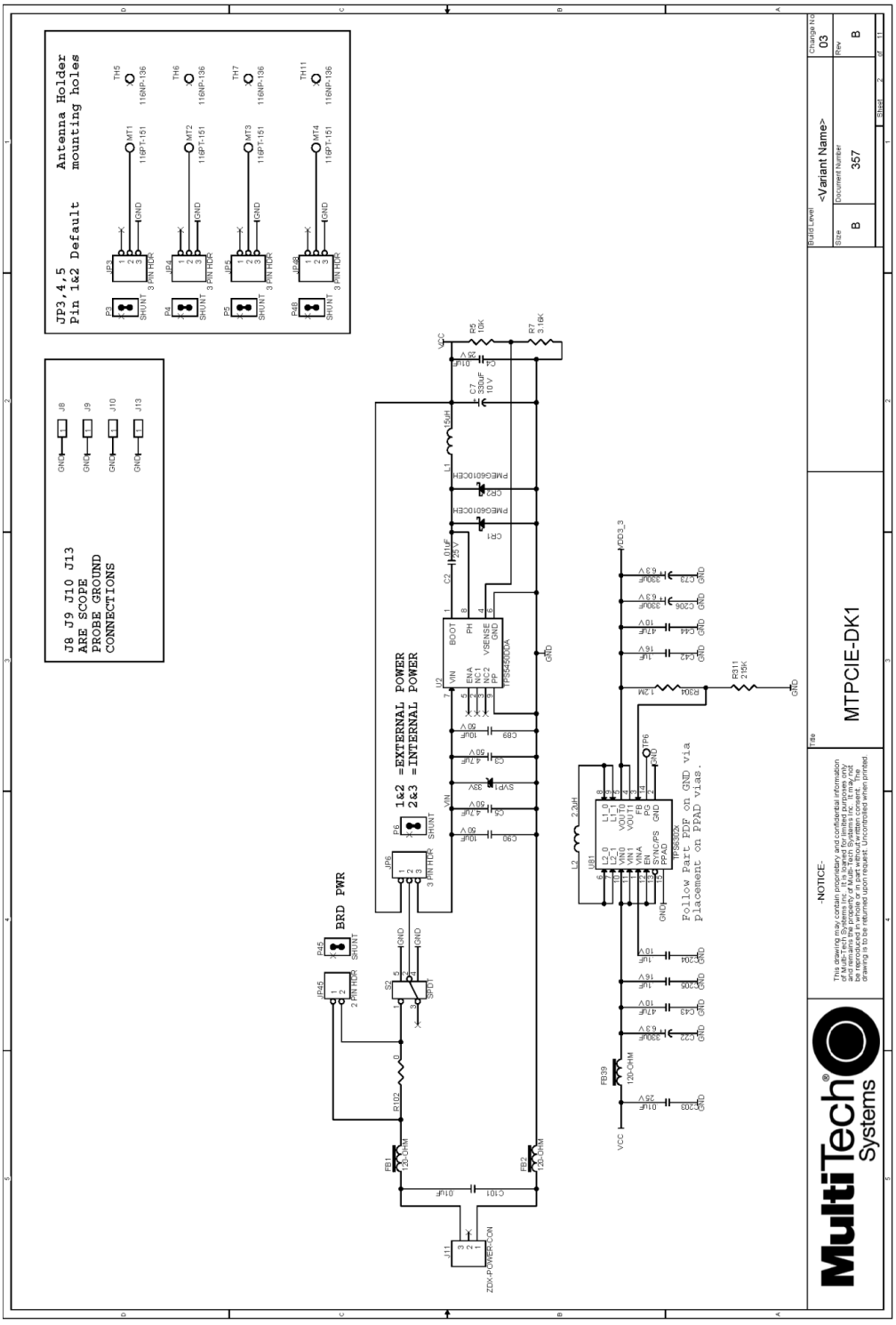
Bottom

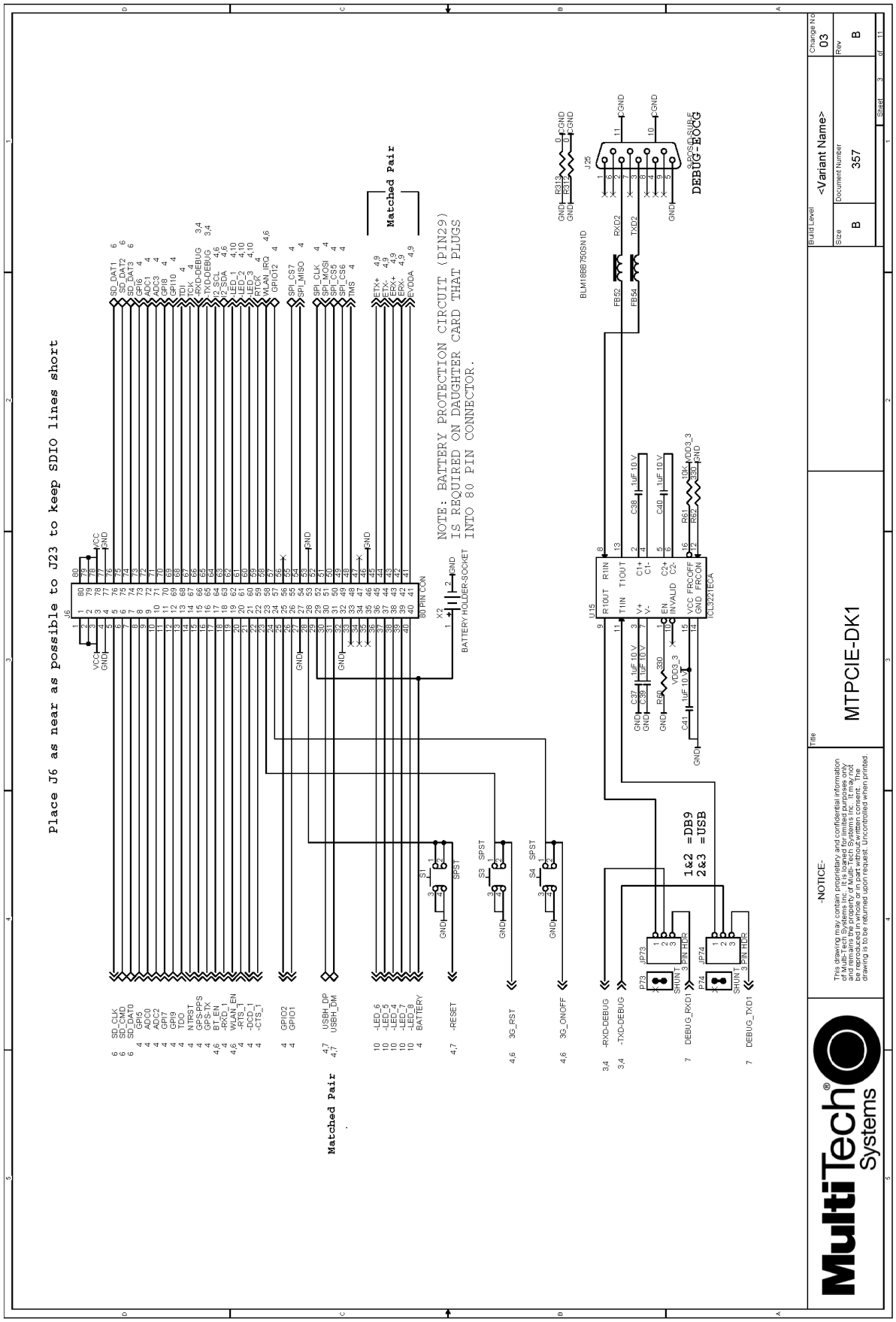


Developer Board Block Diagram



Developer Board Schematics




Place J6 as near as possible to J23 to keep SDIO lines short
NOTE: BATTERY PROTECTION CIRCUIT (PIN29)
IS REQUIRED ON DAUGHTER CARD THAT PLUGS
INTO 80 PIN CONNECTOR.
Matched Pair
Matched Pair
1&2 =DB9
2&3 =USB
DEBUG-EOCG
MTPCIE-DK1
MultiTech Systems
-NOTICE-
Title
Build Level
<Variant Name>
Change No
03
Size
B
Document Number
357
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