Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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MUN5311DW1T1 Series

Preferred Devices

Dual Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base–emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the MUN5311DW1T1 series, two complementary BRT devices are housed in the SOT–363 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	187 (Note 1.) 256 (Note 2.) 1.5 (Note 1.) 2.0 (Note 2.)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1.) 490 (Note 2.)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	250 (Note 1.) 385 (Note 2.) 2.0 (Note 1.) 3.0 (Note 2.)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1.) 325 (Note 2.)	°C/W
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	188 (Note 1.) 208 (Note 2.)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 x 1.0 inch Pad

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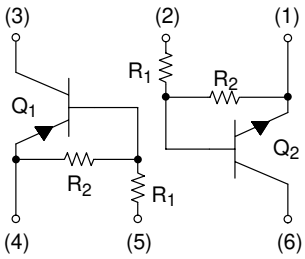
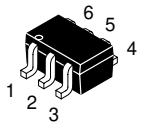
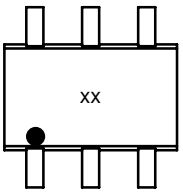




SOT–363
CASE 419B
STYLE 1

MARKING DIAGRAM



xx = Device Marking
(See Page 2)

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (K)	R2 (K)	Shipping
MUN5311DW1T1	SOT–363	11	10	10	3000/Tape & Reel
MUN5312DW1T1	SOT–363	12	22	22	3000/Tape & Reel
MUN5313DW1T1	SOT–363	13	47	47	3000/Tape & Reel
MUN5314DW1T1	SOT–363	14	10	47	3000/Tape & Reel
MUN5315DW1T1 (Note 3.)	SOT–363	15	10	∞	3000/Tape & Reel
MUN5316DW1T1 (Note 3.)	SOT–363	16	4.7	∞	3000/Tape & Reel
MUN5330DW1T1 (Note 3.)	SOT–363	30	1.0	1.0	3000/Tape & Reel
MUN5331DW1T1 (Note 3.)	SOT–363	31	2.2	2.2	3000/Tape & Reel
MUN5332DW1T1 (Note 3.)	SOT–363	32	4.7	4.7	3000/Tape & Reel
MUN5333DW1T1 (Note 3.)	SOT–363	33	4.7	47	3000/Tape & Reel
MUN5334DW1T1 (Note 3.)	SOT–363	34	22	47	3000/Tape & Reel
MUN5335DW1T1 (Note 3.)	SOT–363	35	2.2	47	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	MUN5311DW1T1	I_{EBO}	–	–	0.5	mAdc
	MUN5312DW1T1		–	–	0.2	
	MUN5313DW1T1		–	–	0.1	
	MUN5314DW1T1		–	–	0.2	
	MUN5315DW1T1		–	–	0.9	
	MUN5316DW1T1		–	–	1.9	
	MUN5330DW1T1		–	–	4.3	
	MUN5331DW1T1		–	–	2.3	
	MUN5332DW1T1		–	–	1.5	
	MUN5333DW1T1		–	–	0.18	
	MUN5334DW1T1		–	–	0.13	
	MUN5335DW1T1		–	–	0.2	
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 4.) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	–	–	Vdc

3. New resistor combinations. Updated curves to follow in subsequent data sheets.
4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5.)						
DC Current Gain	MUN5311DW1T1	h_{FE}	35	60	–	
(V_{CE} = 10 V, I_C = 5.0 mA)	MUN5312DW1T1		60	100	–	
	MUN5313DW1T1		80	140	–	
	MUN5314DW1T1		80	140	–	
	MUN5315DW1T1		160	350	–	
	MUN5316DW1T1		160	350	–	
	MUN5330DW1T1		3.0	5.0	–	
	MUN5331DW1T1		8.0	15	–	
	MUN5332DW1T1		15	30	–	
	MUN5333DW1T1		80	200	–	
	MUN5334DW1T1		80	150	–	
	MUN5335DW1T1		80	140	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	–	0.25	Vdc
(I_C = 10 mA, I_B = 0.3 mA)						
(I_C = 10 mA, I_B = 5 mA) MUN5330DW1T1/MUN5331DW1T1						
(I_C = 10 mA, I_B = 1 mA) MUN5315DW1T1/MUN5316DW1T1						
MUN5332DW1T1/MUN5333DW1T1/MUN5334DW1T1						
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	MUN5311DW1T1		–	–	0.2	
	MUN5312DW1T1		–	–	0.2	
	MUN5314DW1T1		–	–	0.2	
	MUN5315DW1T1		–	–	0.2	
	MUN5316DW1T1		–	–	0.2	
	MUN5330DW1T1		–	–	0.2	
	MUN5331DW1T1		–	–	0.2	
	MUN5332DW1T1		–	–	0.2	
	MUN5333DW1T1		–	–	0.2	
	MUN5334DW1T1		–	–	0.2	
	MUN5335DW1T1		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	MUN5313DW1T1		–	–	0.2	
Output Voltage (off)		V_{OH}	4.9	–	–	Vdc
(V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)						
(V_{CC} = 5.0 V, V_B = 0.050 V, R_L = 1.0 kΩ)	MUN5330DW1T1					
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	MUN5315DW1T1					
	MUN5316DW1T1					
	MUN5333DW1T1					
Input Resistor	MUN5311DW1T1	R1	7.0	10	13	k Ω
	MUN5312DW1T1		15.4	22	28.6	
	MUN5313DW1T1		32.9	47	61.1	
	MUN5314DW1T1		7.0	10	13	
	MUN5315DW1T1		7.0	10	13	
	MUN5316DW1T1		3.3	4.7	6.1	
	MUN5330DW1T1		0.7	1.0	1.3	
	MUN5331DW1T1		1.5	2.2	2.9	
	MUN5332DW1T1		3.3	4.7	6.1	
	MUN5333DW1T1		3.3	4.7	6.1	
	MUN5334DW1T1		15.4	22	28.6	
	MUN5335DW1T1		1.54	2.2	2.86	
Resistor Ratio MUN5311DW1T1/MUN5312DW1T1/MUN5313DW1T1		R1/R2	0.8	1.0	1.2	
MUN5314DW1T1			0.17	0.21	0.25	
MUN5315DW1T1/MUN5316DW1T1			–	–	–	
MUN5330DW1T1/MUN5331DW1T1/MUN5332DW1T1			0.8	1.0	1.2	
MUN5333DW1T1			0.055	0.1	0.185	
MUN5334DW1T1			0.38	0.47	0.56	
MUN5335DW1T1			0.038	0.047	0.056	

5. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

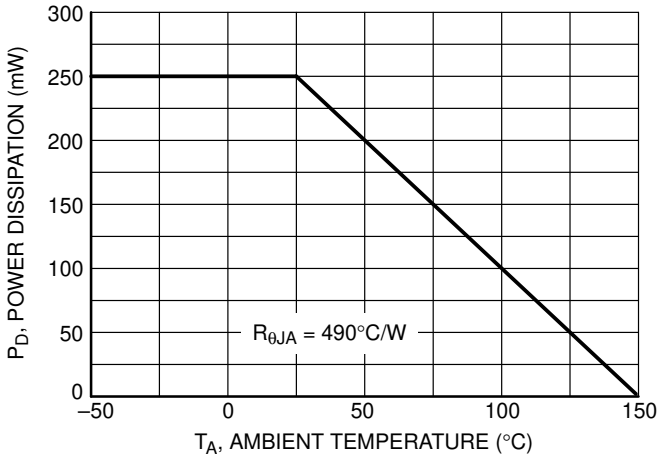


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5311DW1T1 NPN TRANSISTOR

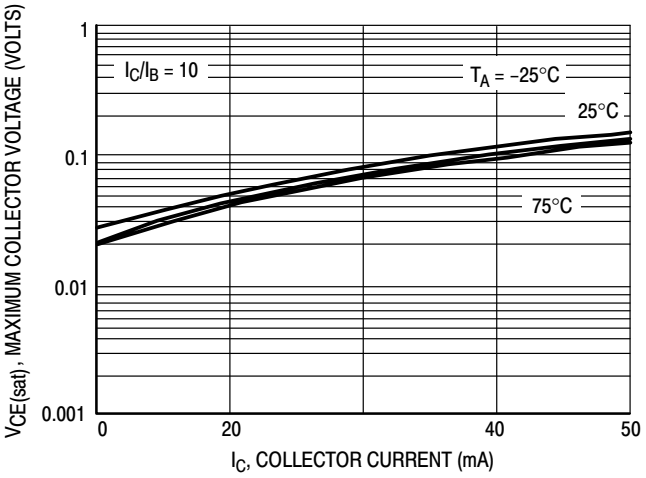


Figure 2. $V_{CE(sat)}$ versus I_C

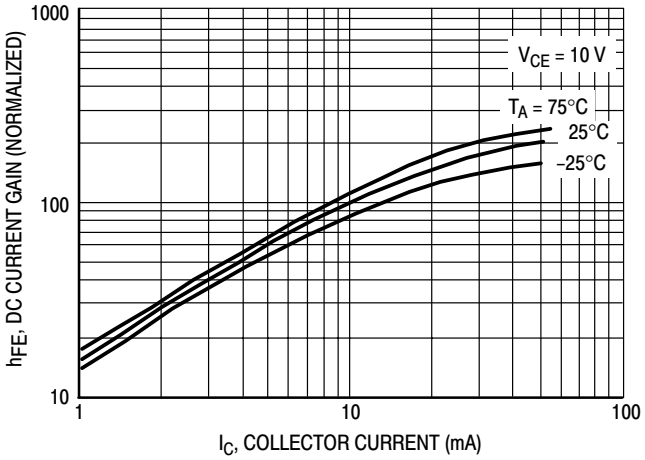


Figure 3. DC Current Gain

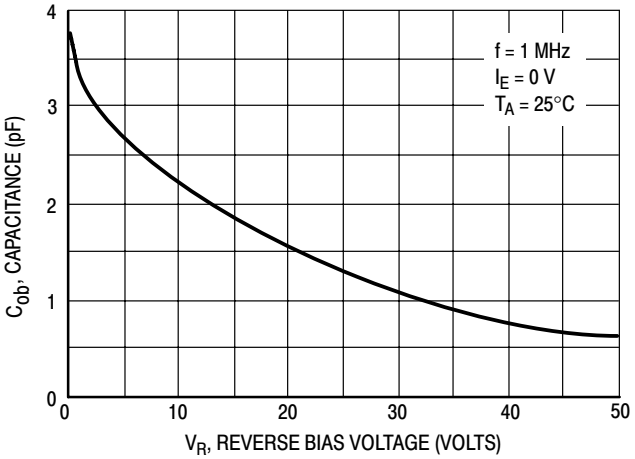


Figure 4. Output Capacitance

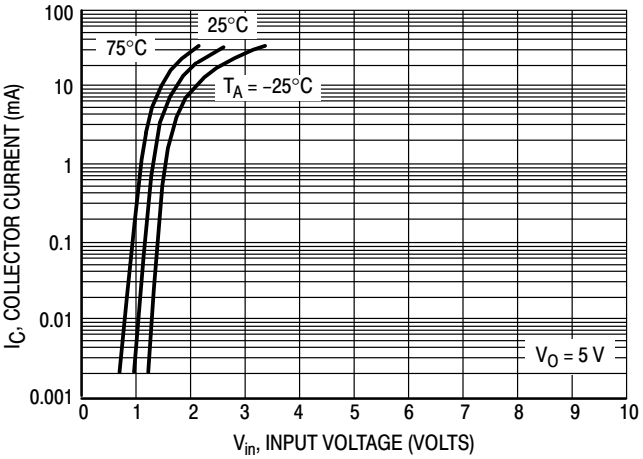


Figure 5. Output Current versus Input Voltage

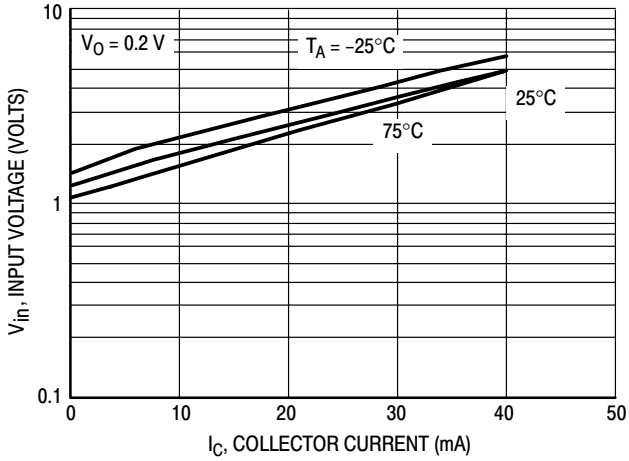


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5311DW1T1 PNP TRANSISTOR

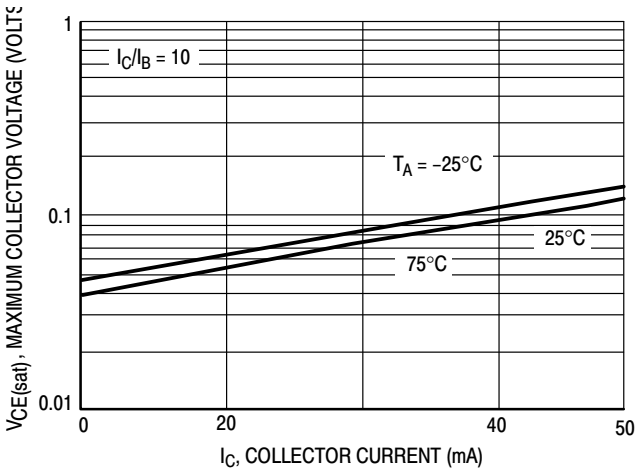


Figure 7. $V_{CE(sat)}$ versus I_C

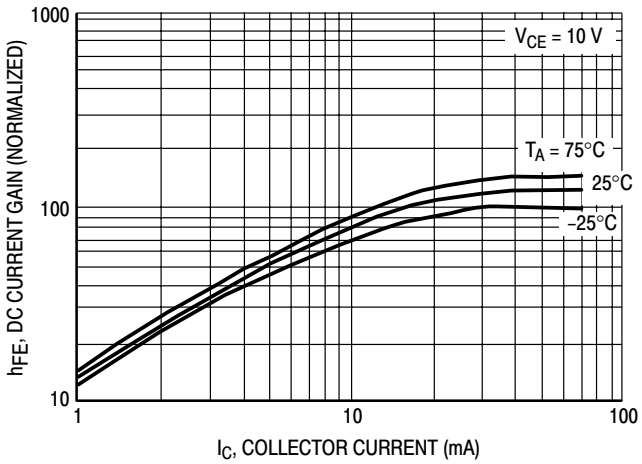


Figure 8. DC Current Gain

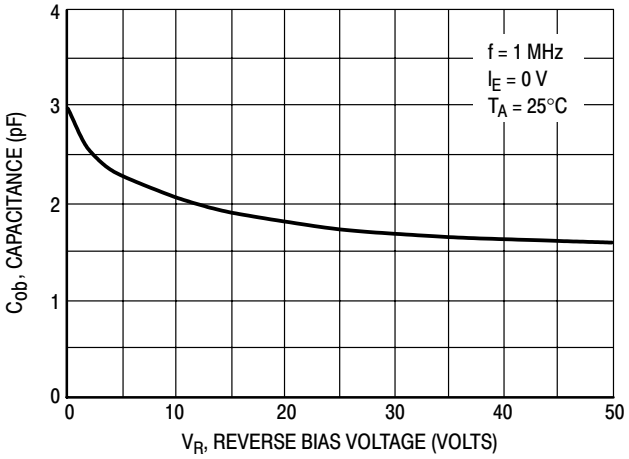


Figure 9. Output Capacitance

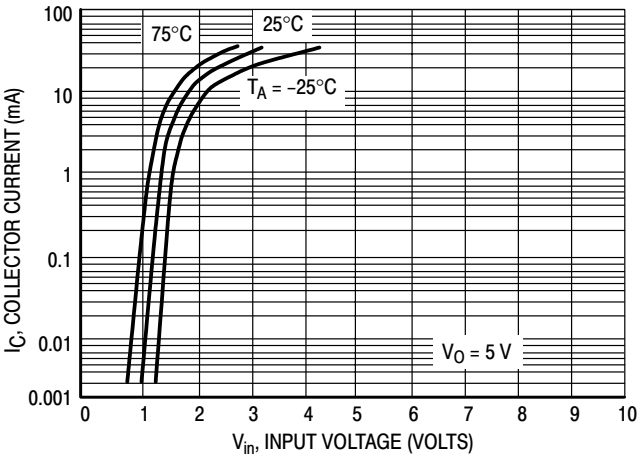


Figure 10. Output Current versus Input Voltage

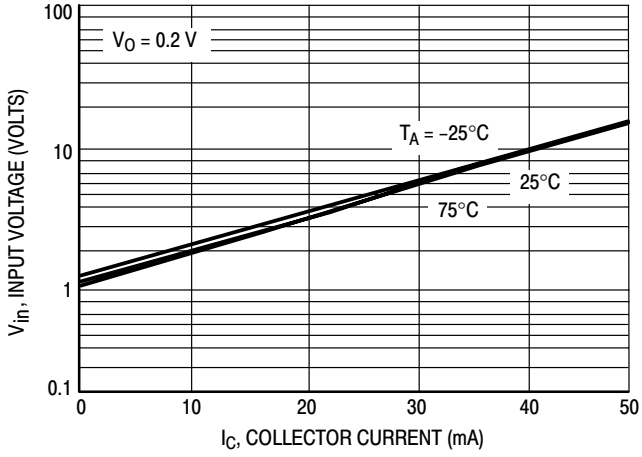


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5312DW1T1 NPN TRANSISTOR

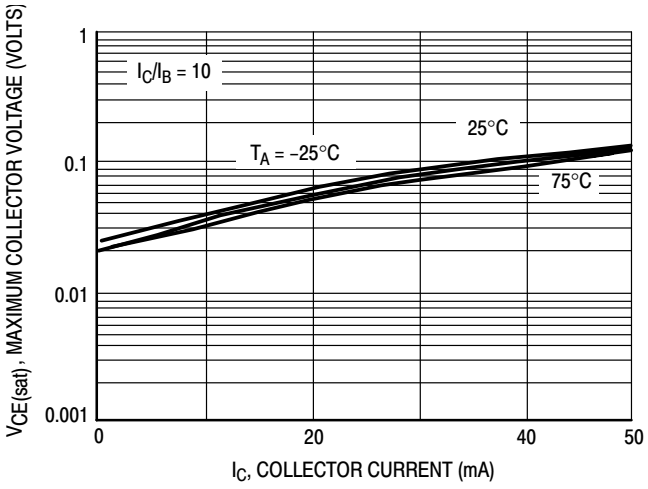


Figure 12. $V_{CE(sat)}$ versus I_C

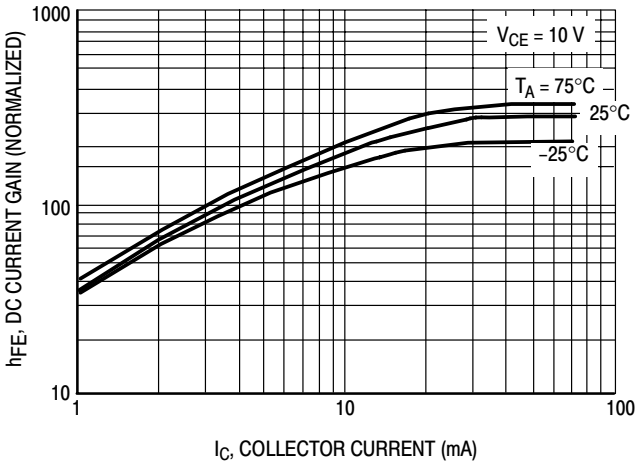


Figure 13. DC Current Gain

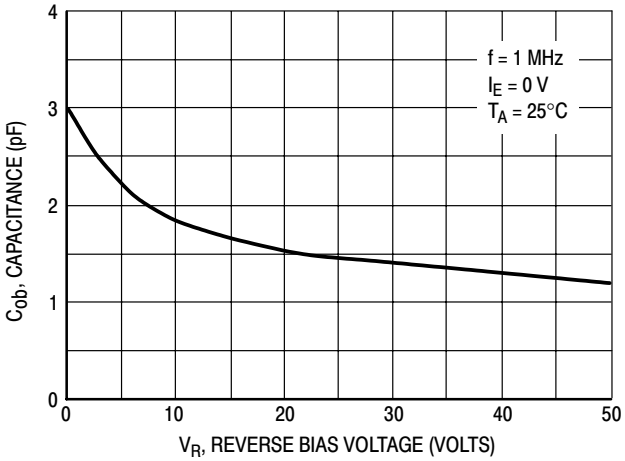


Figure 14. Output Capacitance

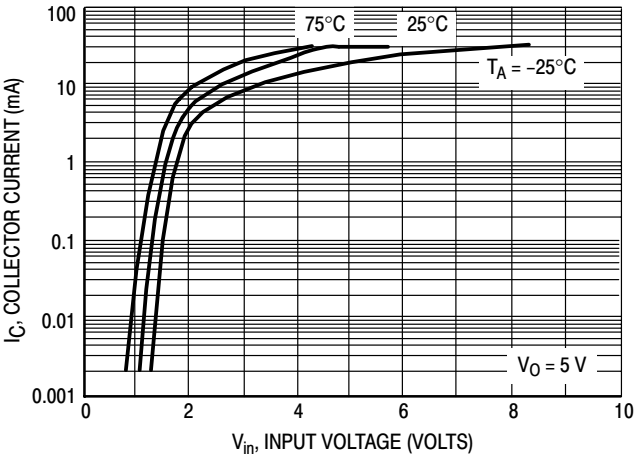


Figure 15. Output Current versus Input Voltage

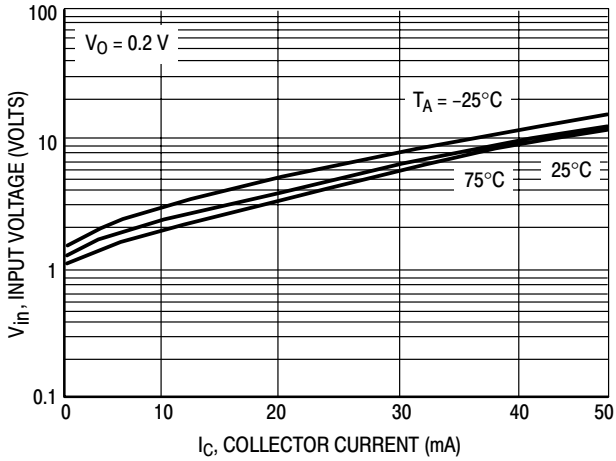


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5312DW1T1 PNP TRANSISTOR

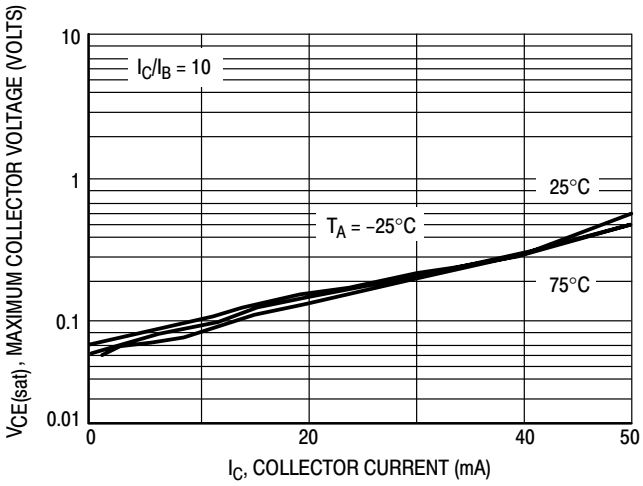


Figure 17. $V_{CE(sat)}$ versus I_C

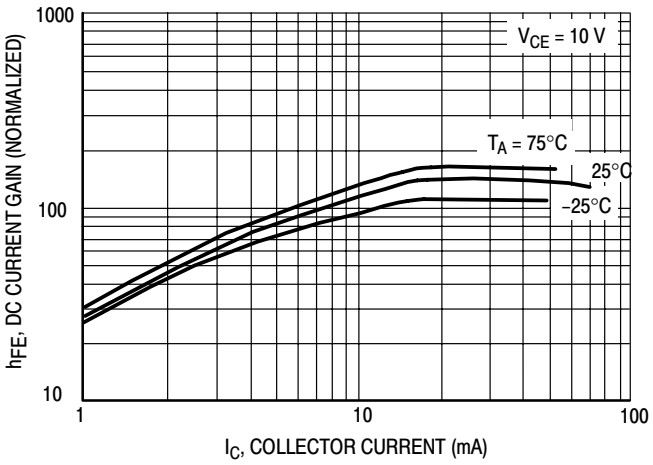


Figure 18. DC Current Gain

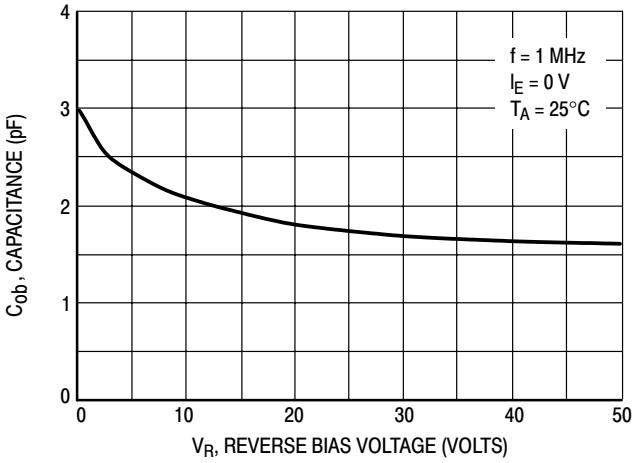


Figure 19. Output Capacitance

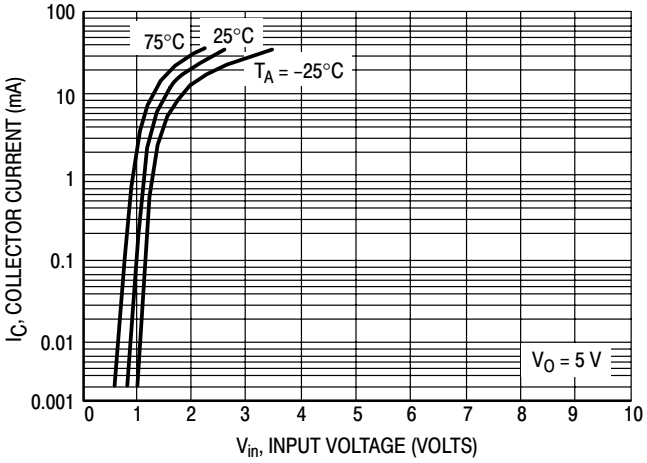


Figure 20. Output Current versus Input Voltage

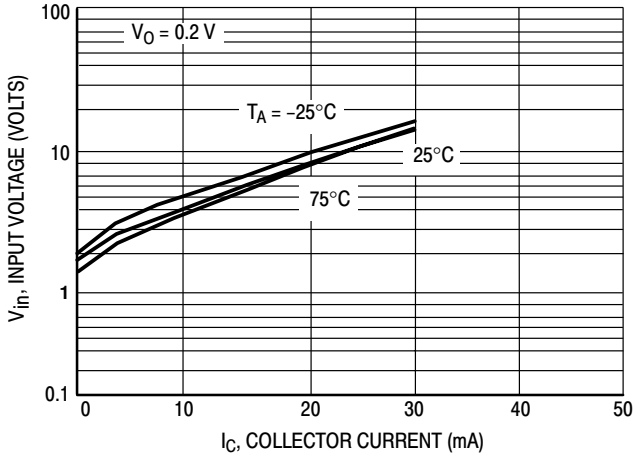


Figure 21. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5313DW1T1 NPN TRANSISTOR

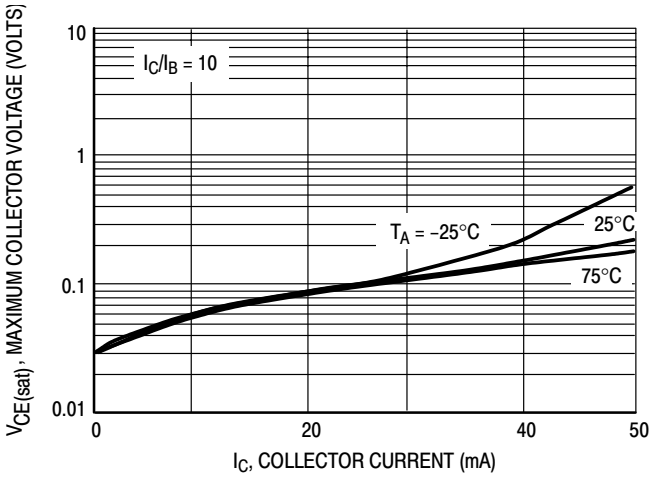


Figure 22. $V_{CE(sat)}$ versus I_C

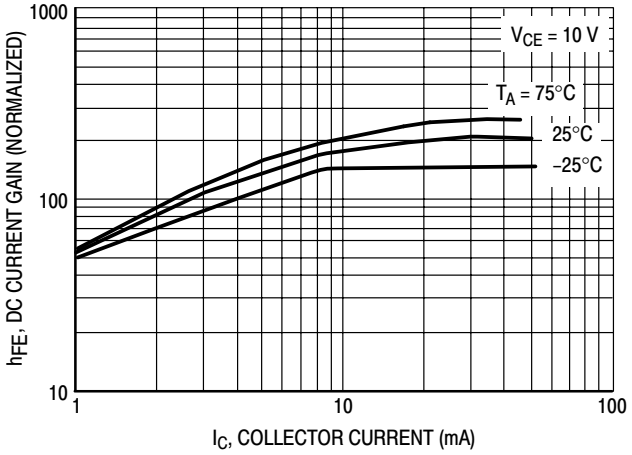


Figure 23. DC Current Gain

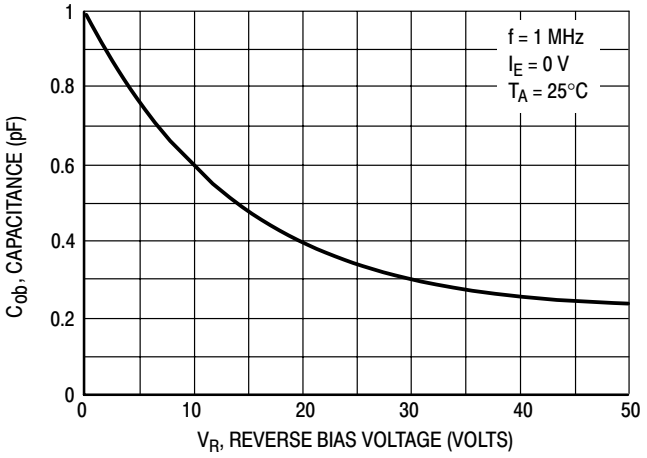


Figure 24. Output Capacitance

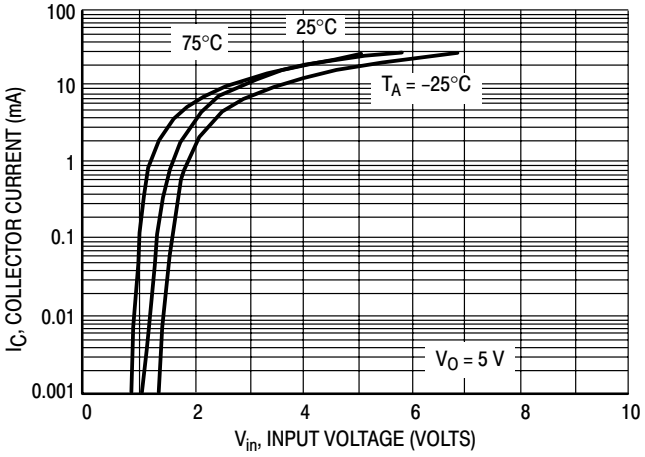


Figure 25. Output Current versus Input Voltage

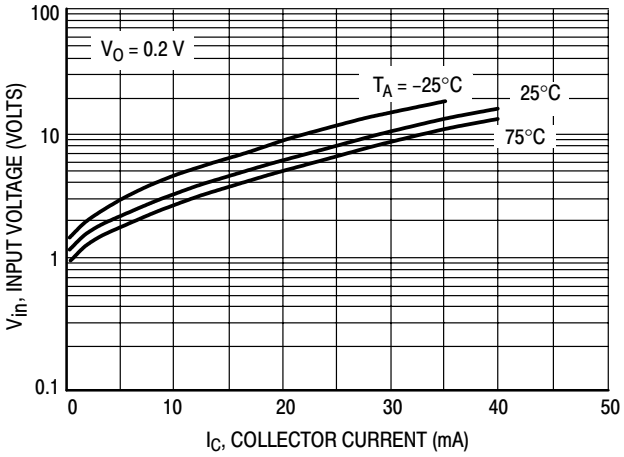


Figure 26. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5313DW1T1 PNP TRANSISTOR

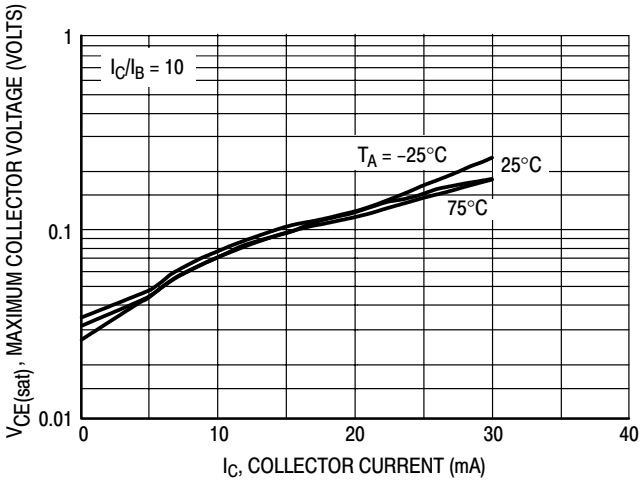


Figure 27. $V_{CE(sat)}$ versus I_C

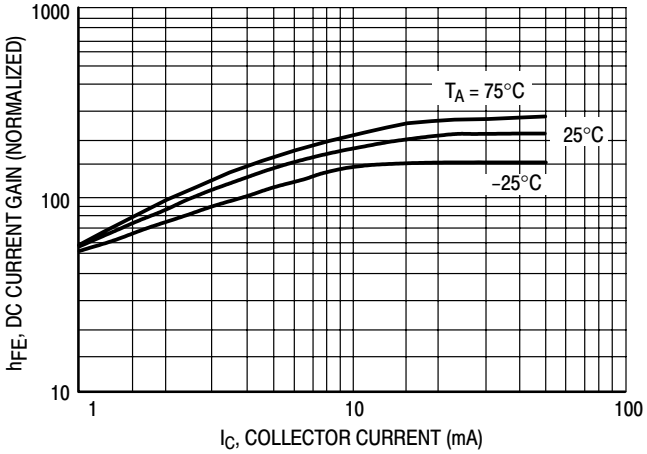


Figure 28. DC Current Gain

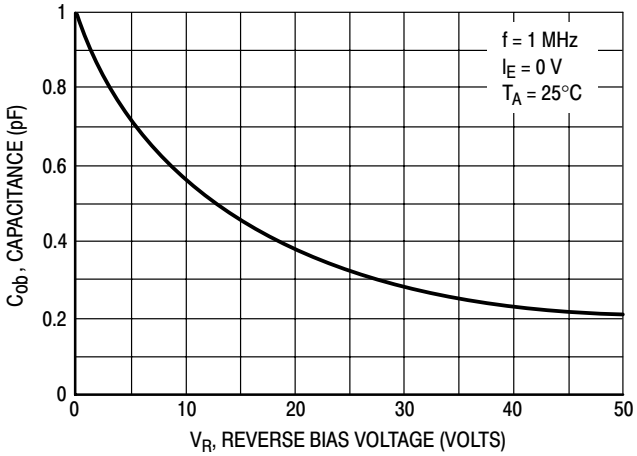


Figure 29. Output Capacitance

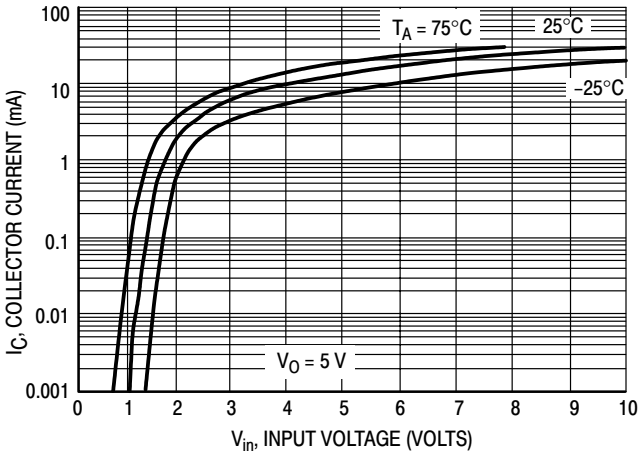


Figure 30. Output Current versus Input Voltage

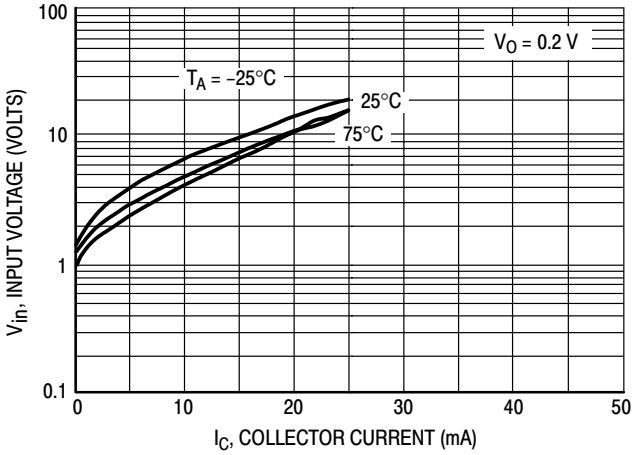


Figure 31. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5314DW1T1 NPN TRANSISTOR

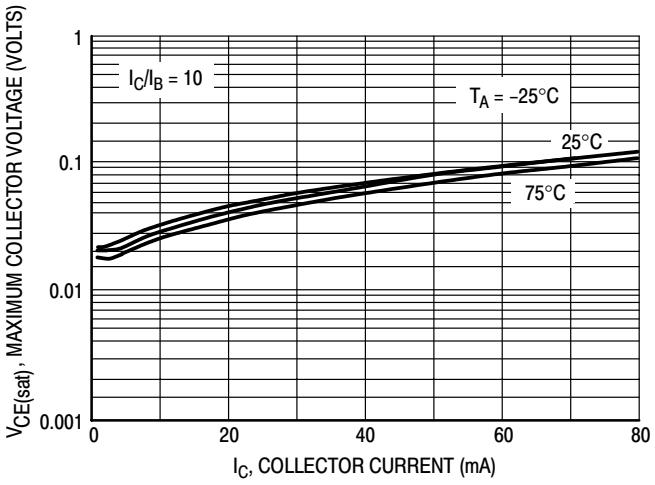


Figure 32. $V_{CE(sat)}$ versus I_C

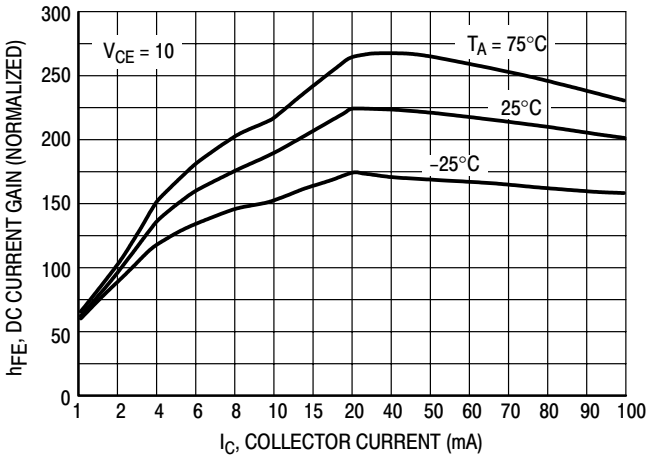


Figure 33. DC Current Gain

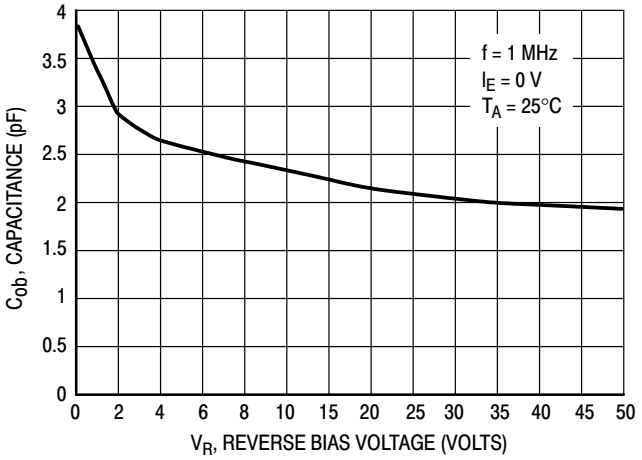


Figure 34. Output Capacitance

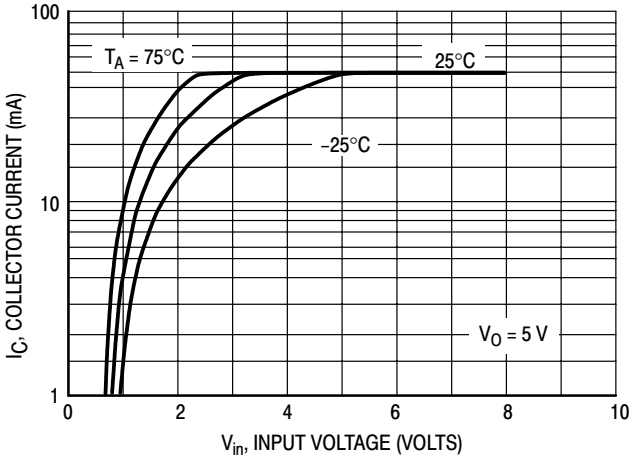


Figure 35. Output Current versus Input Voltage

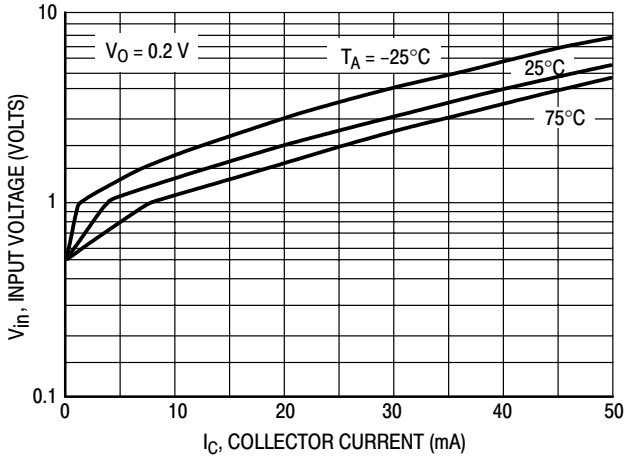


Figure 36. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5314DW1T1 PNP TRANSISTOR

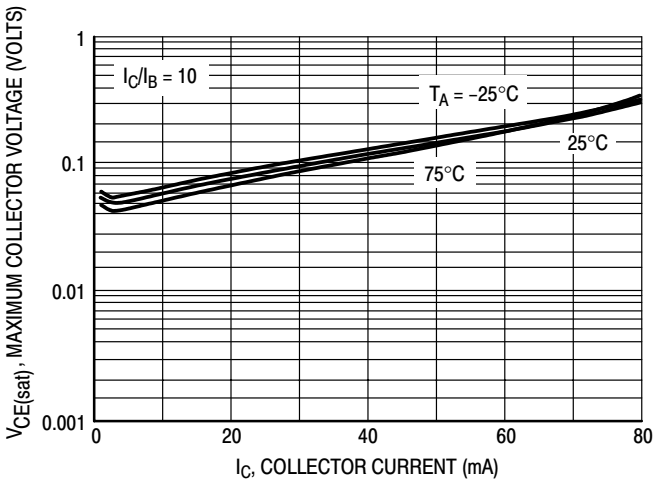


Figure 37. $V_{CE(sat)}$ versus I_C

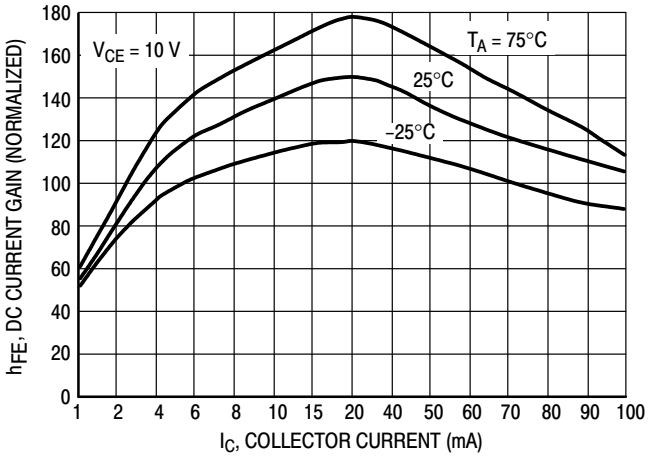


Figure 38. DC Current Gain

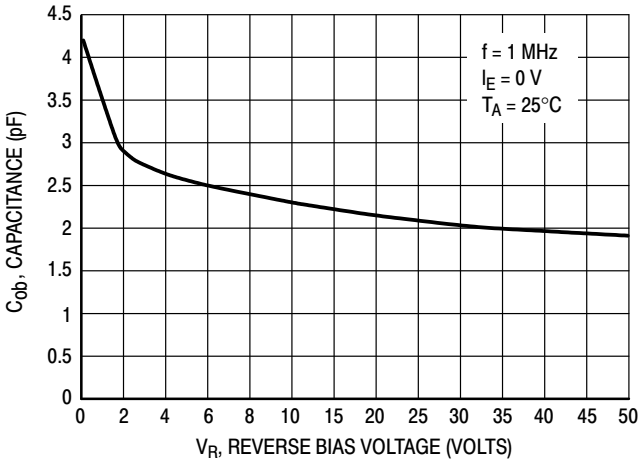


Figure 39. Output Capacitance

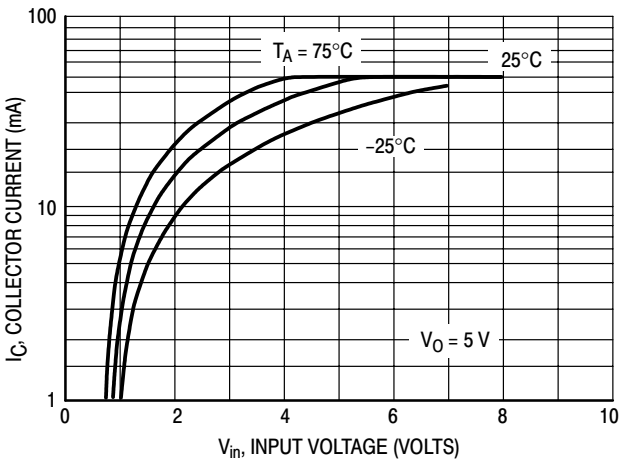


Figure 40. Output Current versus Input Voltage

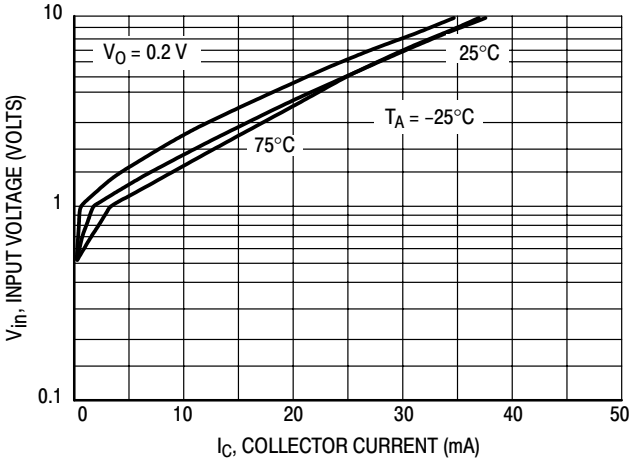


Figure 41. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5315DW1T1

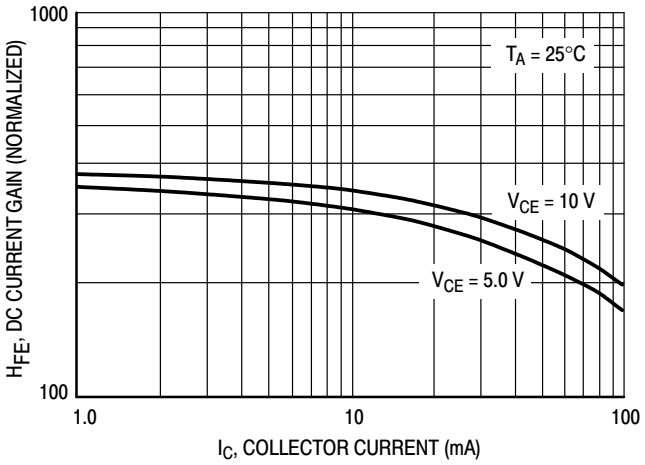


Figure 42. DC Current Gain – PNP

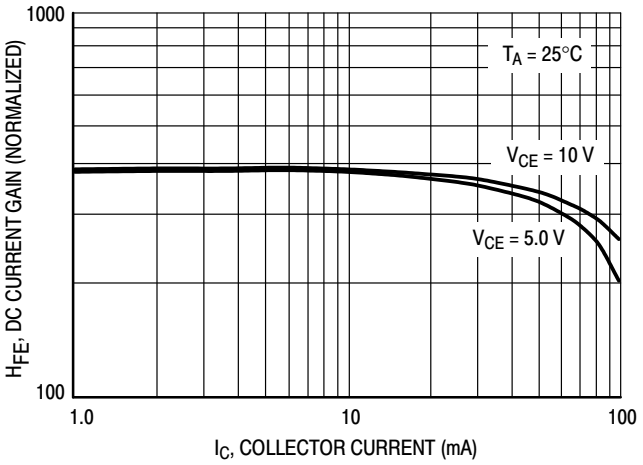


Figure 43. DC Current Gain – NPN

TYPICAL ELECTRICAL CHARACTERISTICS – MUN5316DW1T1

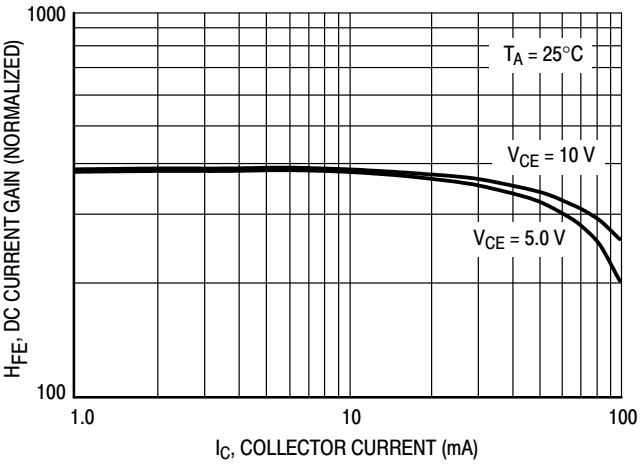


Figure 44. DC Current Gain – PNP

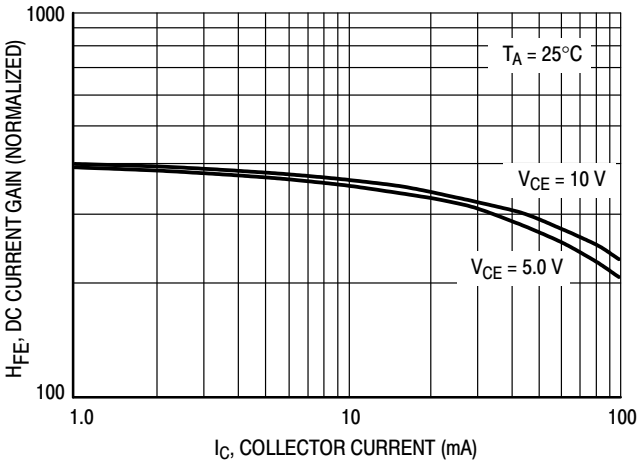


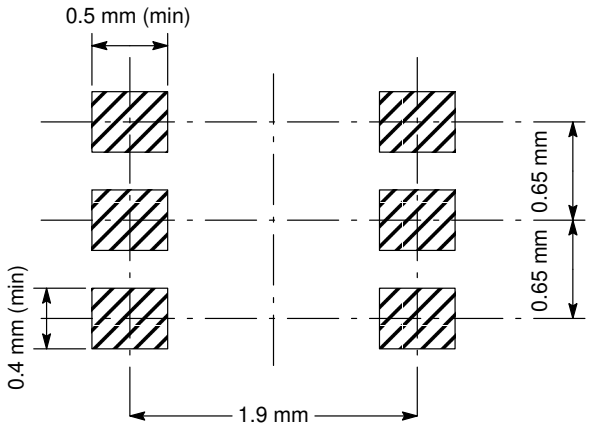
Figure 45. DC Current Gain – NPN

INFORMATION FOR USING THE SOT–363 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

SOT–363



SOT–363 POWER DISSIPATION

The power dissipation of the SOT–363 is a function of the pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 256 milliwatts.

$$P_D = \frac{150°C - 25°C}{490°C/W} = 256 \text{ milliwatts}$$

The 490°C/W for the SOT–363 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 256 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–363 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 46 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

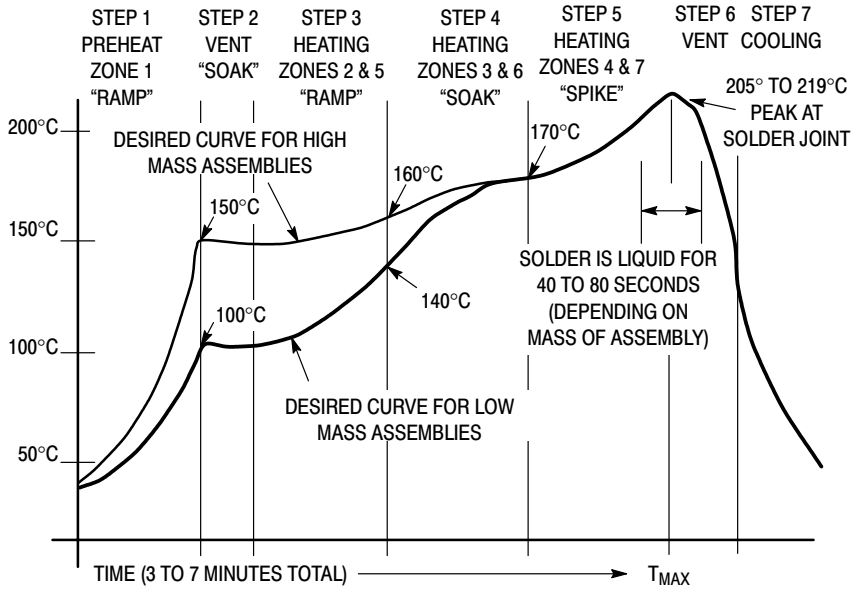
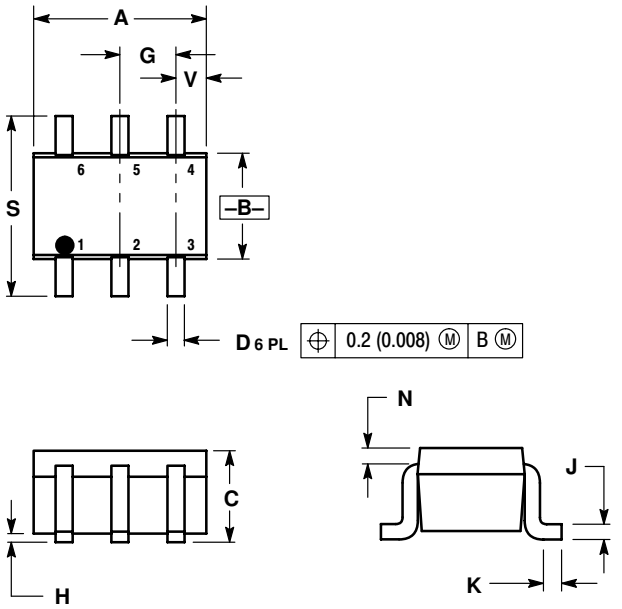


Figure 46. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOT–363
CASE 419B–01
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

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