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MCF51QM128

MCF51QM128

Supports the MCF51QM128VLH, MCF51QM128VHS, MCF51QM64VLF, MCF51QM64VHS, MCF51QM32VHS, MCF51QM32VFM

Features

- Operating characteristics
  - Voltage range: 1.71 V to 3.6 V
  - Flash write voltage range: 1.71 V to 3.6 V
  - Temperature range (ambient): -40°C to 105°C
- Core
  - Up to 50 MHz V1 ColdFire CPU
  - Dhrystone 2.1 performance: 1.10 DMIPS per MHz when executing from internal RAM, 0.99 DMIPS per MHz when executing from flash memory
- System
  - DMA controller with four programmable channels
  - Integrated ColdFire DEBUG_Rev_B+ interface with single-wire BDM connection
- Power management
  - 10 low power modes to provide power optimization based on application requirements
  - Low-leakage wakeup unit (LLWU)
  - Voltage regulator (VREG)
- Clocks
  - Crystal oscillators (two, each with range options): 1 kHz to 32 kHz (low), 1 MHz to 8 MHz (medium), 8 MHz to 32 MHz (high)
  - Multipurpose clock generator (MCG)
- Memories and memory interfaces
  - Flash memory, FlexNVM, FlexRAM, and RAM
  - Serial programming interface (EzPort)
  - Mini-FlexBus external bus interface
- Security and integrity
  - Hardware CRC module to support fast cyclic redundancy checks
  - Hardware random number generator (RNGB)
  - Hardware cryptographic acceleration unit (CAU)
  - 128-bit unique identification (ID) number per chip
- Analog
  - 16-bit SAR ADC
  - 12-bit DAC
  - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference (VREF)
- Timers
  - Programmable delay block (PDB)
  - Motor control/general purpose/PWM timers (FTM)
  - 16-bit low-power timers (LPTMRs)
  - 16-bit modulo timer (MTIM)
  - Carrier modulator transmitter (CMT)
- Communication interfaces
  - UARTs with Smart Card support and FIFO
  - SPI modules, one with FIFO
  - Inter-Integrated Circuit (I2C) modules
- Human-machine interface
  - Up to 48 EGPIO pins
  - Up to 16 rapid general purpose I/O (RGPIO) pins
  - Low-power hardware touch sensor interface (TSI)
  - Interrupt request pin (IRQ)

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device:

1. Go to http://www.freescale.com.
2. Perform a part number search for the following partial device numbers: PCF51QM and MCF51QM.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
CCCC	Core code	CF51 = ColdFire V1
DD	Device number	JF, JU, QF, QH, QM, QU

Table continues on the next page...

Field	Description	Values
MMM	Memory size (program flash memory)[1]	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB
T	Temperature range, ambient (°C)	V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • HS = 44 Laminate QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)

1. All parts also have FlexNVM, FlexRAM, and RAM.

2.4 Example

This is an example part number:

MCF51QM128VLH

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

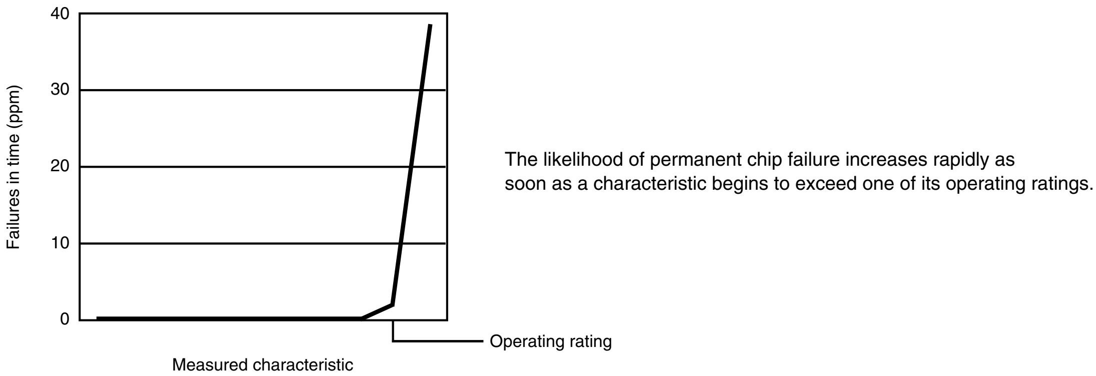
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

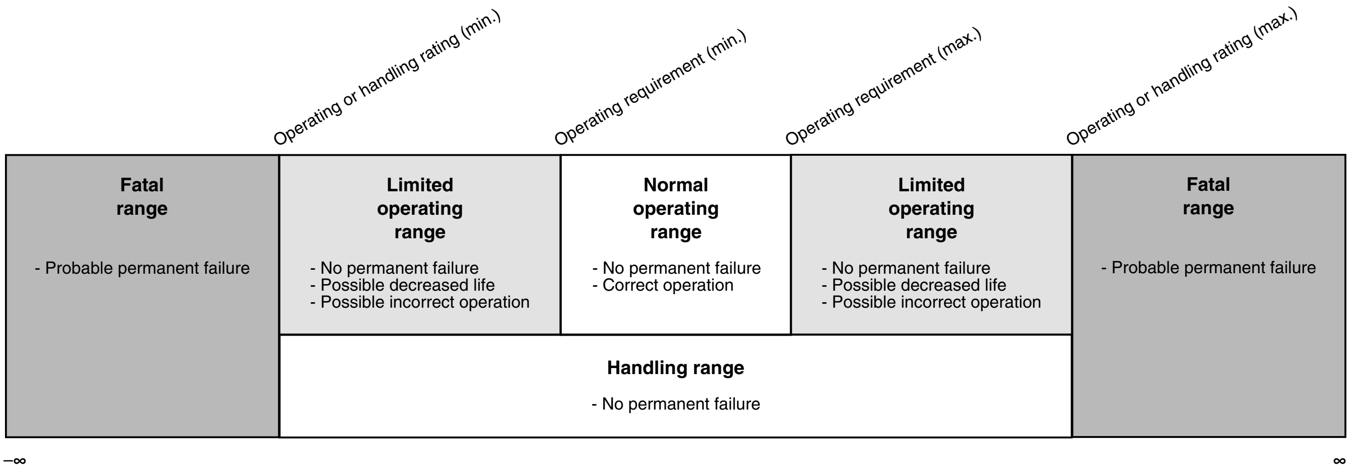
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

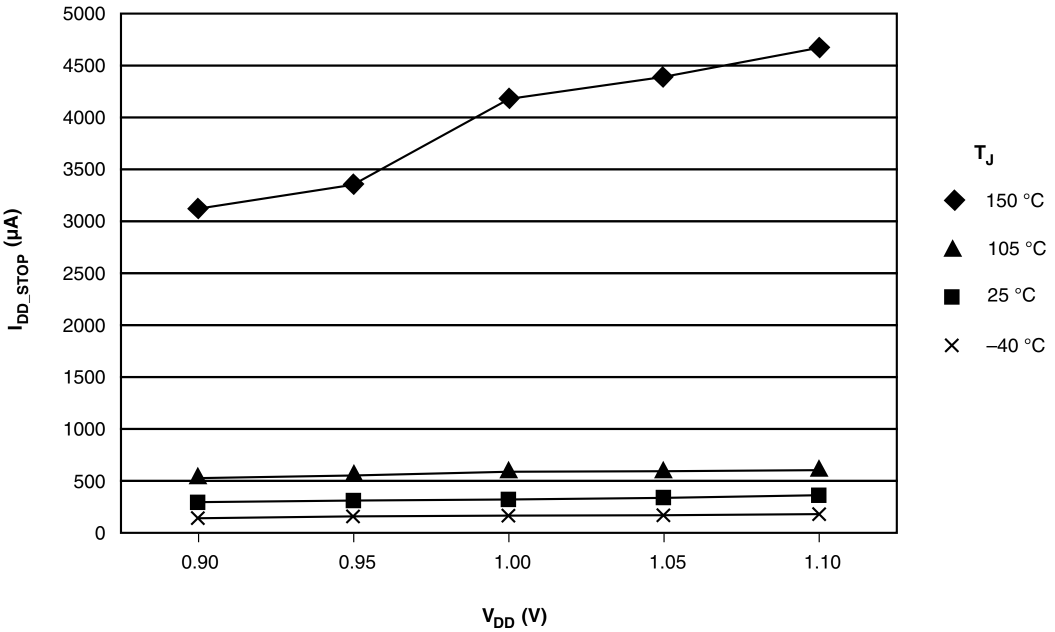
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog, $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
VREGIN	Regulator input	–0.3	6.0	V

5 General

5.1 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

5.2 Nonswitching electrical specifications

5.2.1 Voltage and Current Operating Requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage				1
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$	$0.7 \times V_{DD}$	—	V	
	• $1.7\ V \leq V_{DD} \leq 2.7\ V$	$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage				2
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$	—	$0.35 \times V_{DD}$	V	
	• $1.7\ V \leq V_{DD} \leq 2.7\ V$	—	$0.3 \times V_{DD}$	V	
I_{IC}	DC injection current — single pin				3
	• $V_{IN} > V_{DD}$	0	2	mA	
	• $V_{IN} < V_{SS}$	0	–0.2	mA	
	DC injection current — total MCU limit, includes sum of all stressed pins				3
	• $V_{IN} > V_{DD}$	0	25	mA	
	• $V_{IN} < V_{SS}$	0	–5	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. The device always interprets an input as a 1 when the input is greater than or equal to V_{IH} (min.) and less than or equal to V_{IH} (max.), regardless of whether input hysteresis is turned on.
2. The device always interprets an input as a 0 when the input is less than or equal to V_{IL} (max.) and greater than or equal to V_{IL} (min.), regardless of whether input hysteresis is turned on.
3. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (VIn > VDD) is greater than IDD, the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

5.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = - 9 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	 — —	 0.5 0.5	 V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) • @ full temperature range • @ 25 °C	 — —	 1.0 0.1	 μA μA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and Mini-FlexBus clocks) = 25 MHz

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS1 → RUN	—	150	μs	1, 2
	• VLLS2 → RUN	—	75	μs	1, 2
	• VLLS3 → RUN	—	75	μs	1, 2
	• LLS → RUN	—	6.5	μs	2
	• VLPS → RUN	—	4.6	μs	2
	• STOP → RUN	—	4.6	μs	2

1. Normal boot (FTFL_FOPT[LPBOOT] is 1)
2. The wakeup time includes the execution time for a small amount of firmware used to produce a GPIO clear event. Wakeup time is measured from the falling edge of the external wakeup event to the falling edge of a GPIO clear performed by software.

5.2.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from RAM					2
	• @ 1.8 V	—	13	—	mA	
	• @ 3.0 V	—	13	16	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash memory with page buffering disabled					2
	• @ 1.8 V	—	14.3	—	mA	
	• @ 3.0 V	—	14.5	17.9	mA	

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from RAM, exercising flash memory • @ 1.8 V • @ 3.0 V	 — —	 20 20	 23.5 25	 mA mA	3
I_{DD_WAIT}	Wait mode current at 3.0 V — all peripheral clocks disabled	—	5.8	6.8	mA	4
I_{DD_STOP}	Stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	 — —	 0.34 0.90	 0.41 1.8	 mA mA	
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.63	1.32	mA	5
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.78	1.46	mA	6
I_{DD_VLPW}	Very low-power wait mode current at 3.0 V	—	0.15	0.62	mA	7
I_{DD_VLPS}	Very low-power stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	 — —	 19 145	 45 312	μA	8
I_{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	 — —	 3.0 53.3	 4.8 157	 μA μA	8,9,10
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	 — —	 1.8 39.2	 3.3 115	 μA μA	8,9,10
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	 — —	 1.6 22.2	 2.8 65	 μA μA	8,9
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	 — —	 1.4 17.6	 2.6 50	 μA μA	8,9
I_{DD_RTC}	Average current adder for real-time clock function • @ –40 to 25 °C	—	0.7	—	μA	11

1. The analog supply current is the sum of the active current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode.

5. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash memory.
6. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash memory.
7. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. OSC clocks disabled.
9. All pads disabled.
10. Data reflects devices with 32 KB of RAM. For devices with 16 KB of RAM, power consumption is reduced by 500 nA. For devices with 8 KB of RAM, power consumption is reduced by 750 nA.
11. RTC function current includes LPTMR with OSC enabled with 32.768 kHz crystal at 3.0 V

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode, except for 50 MHz core (FEI mode)
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL
- For the ALLON curve, all peripheral clocks are enabled, but peripherals are not in active operation
- Voltage Regulator disabled
- No GPIOs toggled
- Code execution from flash memory with cache enabled

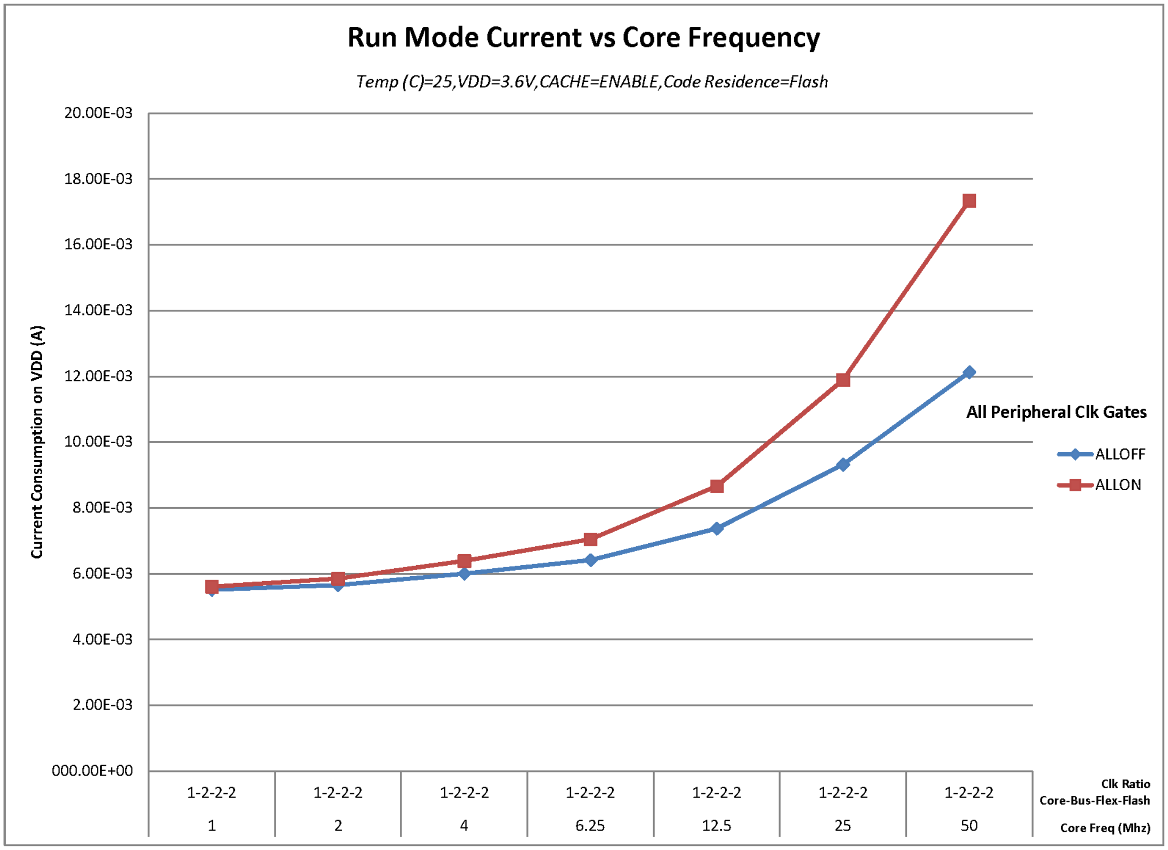


Figure 1. Run mode supply current vs. core frequency

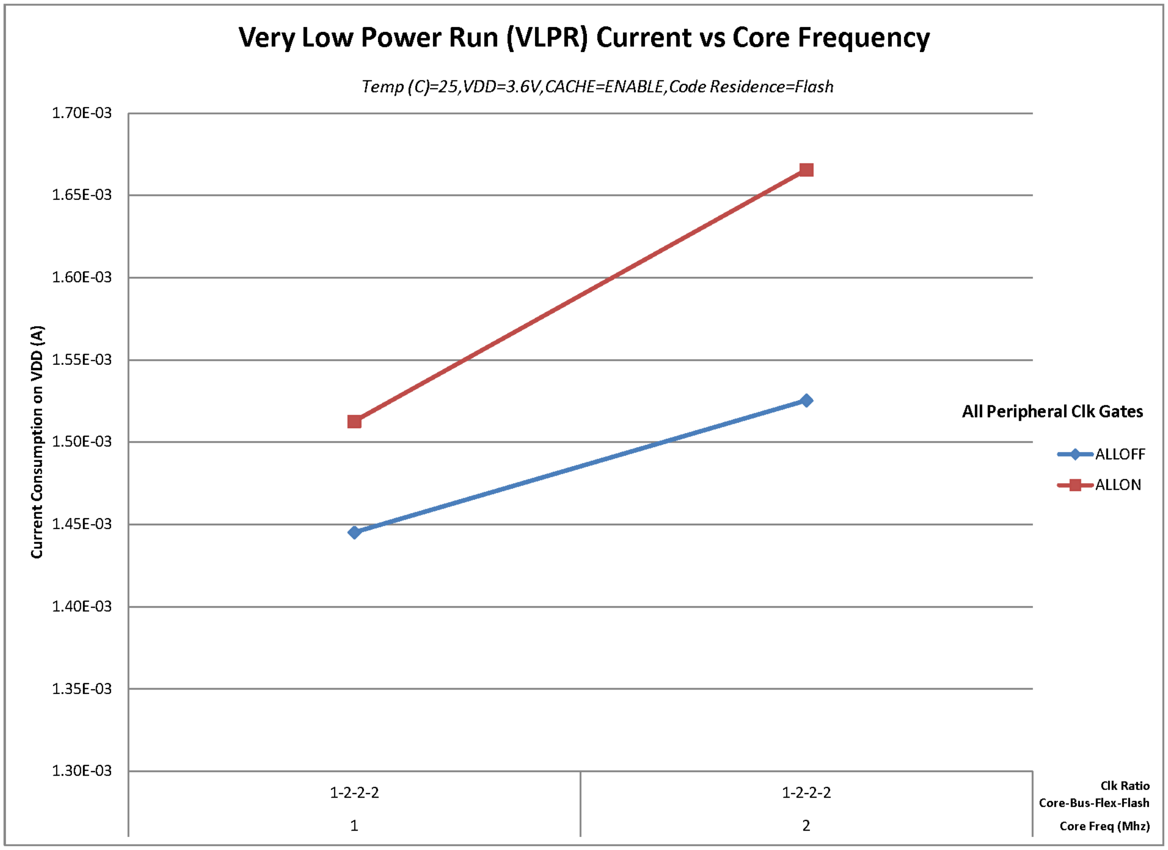


Figure 2. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBμV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	19		
V_{RE3}	Radiated emissions voltage, band 3	150–500	17		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16		
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

2. V_{DD} = 3 V, T_A = 25 °C, f_{OSC} = 32 kHz (crystal), f_{BUS} = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching electrical specifications

Table 8. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus clock	—	25	MHz	
FB_CLK	Mini-FlexBus clock	—	25	MHz	1
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	2	MHz	
f_{BUS}	Bus clock	—	1	MHz	
FB_CLK	Mini-FlexBus clock	—	1	MHz	1
f_{LPTMR}	LPTMR clock[2]	—	25	MHz	

1. When the Mini-FlexBus is enabled, its clock frequency is always the same as the bus clock frequency.
2. A maximum frequency of 25 MHz for the LPTMR in VLPR mode is possible when the LPTMR is configured for pulse counting mode and is driven externally via the LPTMR_ALT1, LPTMR_ALT2, or LPTMR_ALT3 pin.

5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and I^2C signals. The conditions are 50 pf load, V_{DD} = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 9. EGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
G1	Bus clock from CLK_OUT pin high to GPIO output valid	—	32	ns
G2	Bus clock from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
G3	GPIO input valid to bus clock high	28	—	ns
G4	Bus clock from CLK_OUT pin high to GPIO input invalid	—	4	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	Bus clock cycles
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) Asynchronous path[2]	100	—	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) Asynchronous path[2]	50	—	ns
	External reset pulse width (digital glitch filter disabled)	100	—	ns
	Mode select (MS) hold time after reset deassertion	2	—	Bus clock cycles

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

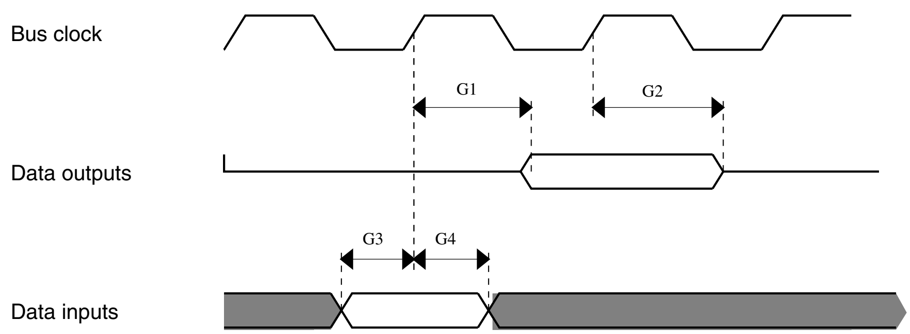


Figure 3. EGPIO timing diagram

The following general purpose specifications apply to all signals configured for RGPIO, FTM, and UART. The conditions are 25 pf load, V_{DD} = 3.6 V to 1.71 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 10. RGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
R1	CPUCLK from CLK_OUT pin high to GPIO output valid	—	16	ns
R2	CPUCLK from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
R3	GPIO input valid to bus clock high	17	—	ns
R4	CPUCLK from CLK_OUT pin high to GPIO input invalid	—	2	ns

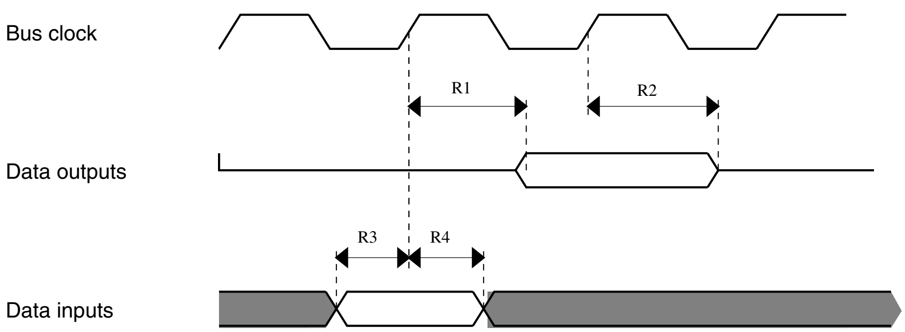


Figure 4. RGPIO timing diagram

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	115	°C
T_A	Ambient temperature	–40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	44 Laminate QFN	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	73	79	108	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	54	55	69	33	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	61	66	91	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	48	63	28	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	37	34	44	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	20	31	2.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5.0	4.0	6.0	6.0	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug specifications

Table 12. Background debug mode (BDM) timing

Number	Symbol	Description	Min.	Max.	Unit
1	t_{MSSU}	BKGD/MS setup time after issuing background debug force reset to enter user mode or BDM	500	—	ns
2	t_{MSH}	BKGD/MS hold time after issuing background debug force reset to enter user mode or BDM[1]	100	—	μs

1. To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

6.2 System modules

6.2.1 VREG electrical specifications

Table 13. VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	μA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	1.54	μA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA μA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.3 Clock modules

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 10	—	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 1.0	± 4.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	3.3	4	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll\_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fll\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 50	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	1350 600	— —	ps ps	8
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.

6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3

Table continues on the next page...