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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# RF LDMOS Wideband Integrated Power Amplifiers

The MW4IC2020 wideband integrated circuit is designed with on-chip matching that makes it usable from 1600 to 2400 MHz. This multi-stage structure is rated for 26 to 28 Volt operation and covers all typical cellular base station modulation formats.

### Final Application

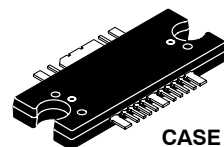
- Typical Two-Tone Performance:  $V_{DD} = 26$  Volts,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 200$  mA,  $I_{DQ3} = 300$  mA,  $P_{out} = 20$  Watts PEP, Full Frequency Band  
 Power Gain — 29 dB  
 IMD — -32 dBc  
 Drain Efficiency — 26% (at 1805 MHz) and 20% (at 1990 MHz)

### Driver Applications

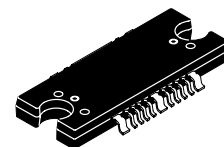
- Typical GSM EDGE Performance:  $V_{DD} = 26$  Volts,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 230$  mA,  $I_{DQ3} = 230$  mA,  $P_{out} = 5$  Watts Avg., Full Frequency Band  
 Power Gain — 29 dB  
 Spectral Regrowth @ 400 kHz Offset = -66 dBc  
 Spectral Regrowth @ 600 kHz Offset = -77 dBc  
 EVM — 1% rms
- Typical CDMA Performance:  $V_{DD} = 26$  Volts,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 240$  mA,  $I_{DQ3} = 250$  mA,  $P_{out} = 1$  Watt Avg., Full Frequency Band, IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13), Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.  
 Power Gain — 30 dB  
 ACPR @ 885 kHz Offset = -61 dBc in 30 kHz Bandwidth  
 ALT1 @ 1.25 MHz Offset = -69 dBc in 12.5 kHz Bandwidth  
 ALT2 @ 2.25 MHz Offset = -59 dBc in 1 MHz Bandwidth
- Capable of Handling 3:1 VSWR, @ 26 Vdc, 1990 MHz, 8 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 8 W CW  $P_{out}$ .
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror  $g_m$  Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- 200°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

**MW4IC2020MBR1**  
**MW4IC2020GMBR1**

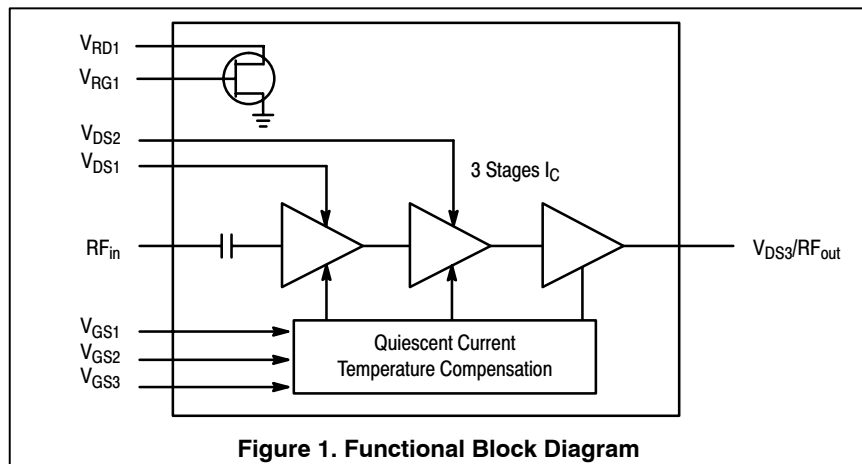
**1805-1990 MHz, 20 W, 26 V**  
**GSM/GSM EDGE, CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**



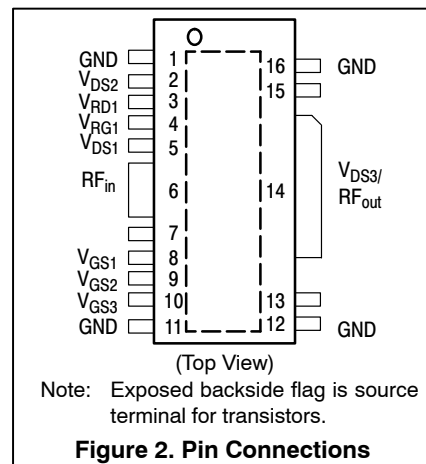
**CASE 1329-09**  
**TO-272 WB-16**  
**PLASTIC**  
**MW4IC2020MBR1**



**CASE 1329A-03**  
**TO-272 WB-16 GULL**  
**PLASTIC**  
**MW4IC2020GMBR1**



**Figure 1. Functional Block Diagram**



(Top View)  
 Note: Exposed backside flag is source terminal for transistors.

**Figure 2. Pin Connections**

1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1987.

ARCHIVE INFORMATION

ARCHIVE INFORMATION



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +175	°C
Operating Junction Temperature	$T_J$	200	°C
Input Power	$P_{in}$	20	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10.5 5.1 2.3	°C/W
		Stage 1	
		Stage 2	
		Stage 3	

**Table 3. ESD Protection Characteristics**

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C5 (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> (In Freescale Wideband 1805-1990 MHz Test Fixture, 50 ohm system) $V_{DD} = 26$ Vdc, $I_{DQ1} = 80$ mA, $I_{DQ2} = 200$ mA, $I_{DQ3} = 300$ mA, $P_{out} = 20$ W PEP, $f_1 = 1990$ MHz, $f_2 = 1990.1$ MHz and $f_1 = 1805$ MHz, $f_2 = 1805.1$ MHz, Two-Tone CW					
Power Gain	$G_{ps}$	27	29	—	dB
Drain Efficiency	$\eta_D$	24 18	26 20	—	%
		$f_1 = 1805$ MHz, $f_2 = 1805.1$ MHz			
		$f_1 = 1990$ MHz, $f_2 = 1990.1$ MHz			
Input Return Loss	IRL	—	—	-10	dB
Intermodulation Distortion	IMD	—	-32	-27	dBc

**Typical Performances** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 26$  Vdc,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 200$  mA,  $I_{DQ3} = 300$  mA, 1805 MHz < Frequency < 1990 MHz, 1-Tone

Saturated Pulsed Output Power ( $f = 1$ kHz, Duty Cycle 10%)	$P_{sat}$	—	33	—	W
Quiescent Current Accuracy over Temperature (-10 to 85°C) (2)	$\Delta I_{QT}$	—	±5	—	%
Gain Flatness in 30 MHz Bandwidth @ $P_{out} = 1$ W CW	$G_F$	—	0.15	—	dB
Deviation from Linear Phase in 30 MHz Bandwidth @ $P_{out} = 1$ W CW 1805-1880 MHz 1930-1990 MHz	$\Phi$	—	±0.5 ±0.2	—	°
Delay @ $P_{out} = 1$ W CW Including Output Matching	Delay	—	1.8	—	ns
Part-to-Part Phase Variation @ $P_{out} = 1$ W CW	$\Phi\Delta$	—	±10	—	°

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977.

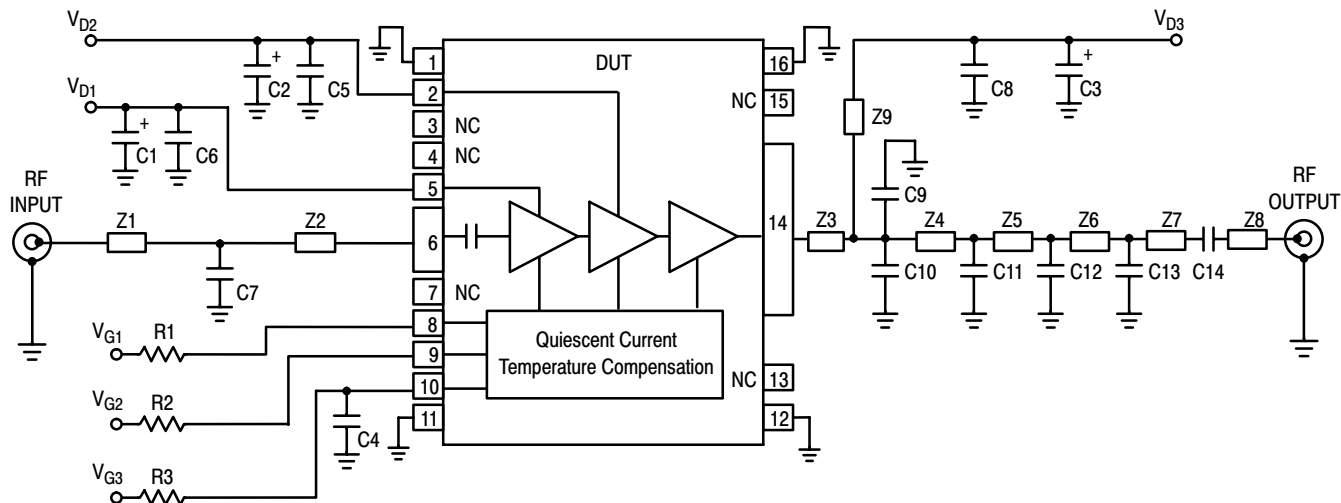
(continued)

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical CDMA Performances</b> (In Modified CDMA Test Fixture, 50 ohm system) $V_{DD} = 26\text{ Vdc}$ , $I_{DQ1} = 80\text{ mA}$ , $I_{DQ2} = 240\text{ mA}$ , $I_{DQ3} = 250\text{ mA}$ , $P_{out} = 1\text{ W Avg.}$ , 11930 MHz < Frequency < 1990 MHz, 1-Tone, 9 Channel Forward Model (Pilot, Paging, Sync, Traffic Codes 8 through 13). Peak/Avg. Ratio 9.8 dB @ 0.01% Probability on CCDF.					
Power Gain	$G_{ps}$	—	30	—	dB
Drain Efficiency	$\eta_D$	—	5	—	%
Adjacent Channel Power Ratio ( $\pm 885\text{ kHz}$ in 30 kHz Bandwidth)	ACPR	—	-61	—	dBc
Alternate 1 Channel Power Ratio ( $\pm 1.25\text{ MHz}$ in 12.5 kHz Bandwidth)	ALT1	—	-69	—	dBc
Alternate 2 Channel Power Ratio ( $\pm 2.25\text{ MHz}$ in 1 MHz Bandwidth)	ALT2	—	-59	—	dBc

**Typical GSM EDGE Performances** (In Modified GSM EDGE Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ1} = 80\text{ mA}$ ,  $I_{DQ2} = 230\text{ mA}$ ,  $I_{DQ3} = 230\text{ mA}$ ,  $P_{out} = 5\text{ W Avg.}$ , 1805 MHz < Frequency < 1990 MHz

Power Gain	$G_{ps}$	—	29	—	dB
Drain Efficiency	$\eta_D$	—	15	—	%
Error Vector Magnitude	EVM	—	1	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-66	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-77	—	dBc

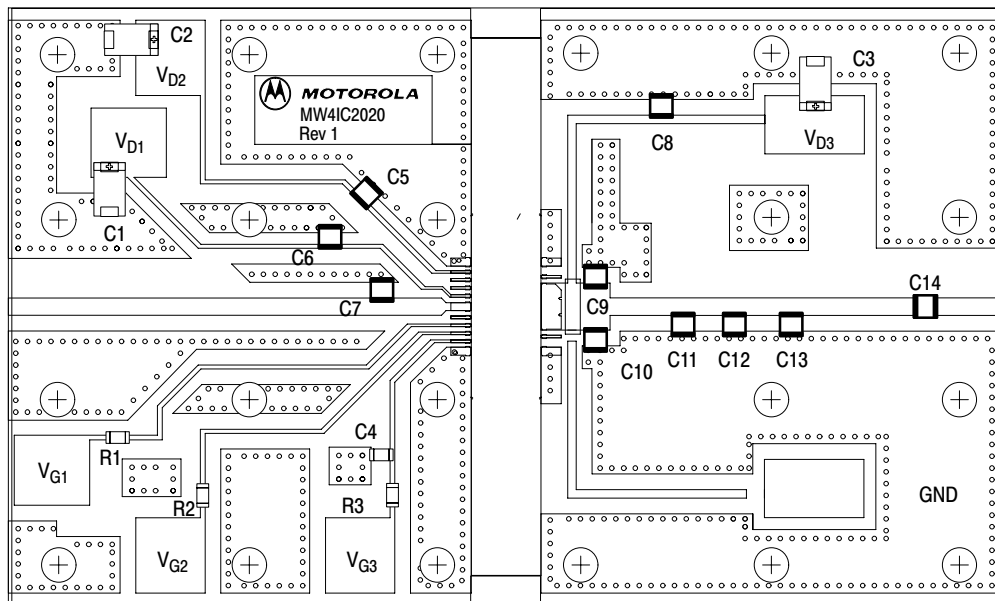


Z1	1.820" x 0.087" Microstrip	Z6	0.303" x 0.087" Microstrip
Z2	0.245" x 0.087" Microstrip	Z7	0.640" x 0.087" Microstrip
Z3	0.345" x 0.236" Microstrip	Z8	0.334" x 0.087" Microstrip
Z4	0.327" x 0.087" Microstrip	Z9	1.231" x 0.043" Microstrip
Z5	0.271" x 0.087" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$

Figure 3. MW4IC2020MBR1(GMBR1) Test Circuit Schematic

Table 6. MW4IC2020MBR1(GMBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3	10 $\mu$ F, 35 V Tantalum Capacitors	TAJE226M035	AVX
C4	220 nF Chip Capacitor (1206)	12065C224K28	AVX
C5, C6, C8	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C7	0.5 pF 100B Chip Capacitor	100B0R5BW	ATC
C9, C11	1.8 pF 100B Chip Capacitors	100B1R8BW	ATC
C10	2.2 pF 100B Chip Capacitor	100B2R2BW	ATC
C12	1 pF 100B Chip Capacitor	100B1R0BW	ATC
C13	0.3 pF 100B Chip Capacitor	100B0R3BW	ATC
C14	10 pF 100B Chip Capacitor	100B100GW	ATC
R1, R2, R3	1.8 k $\Omega$ Chip Resistors (1206)		



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

**Figure 4. MW4IC2020MBR1(GMBR1) Test Circuit Component Layout**

## TYPICAL CHARACTERISTICS

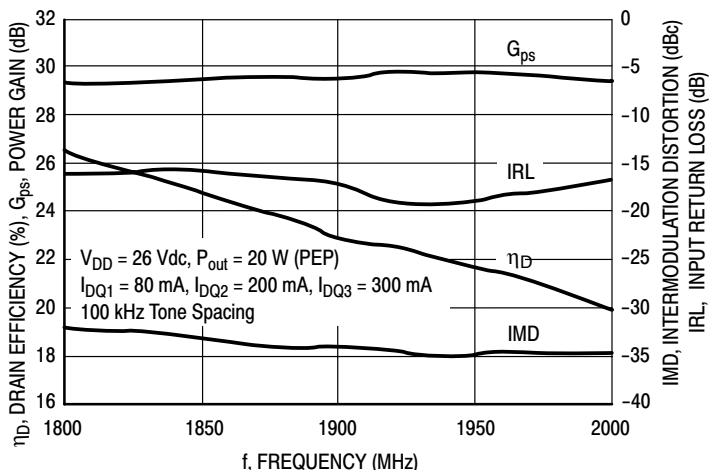


Figure 5. Two-Tone Wideband Performance

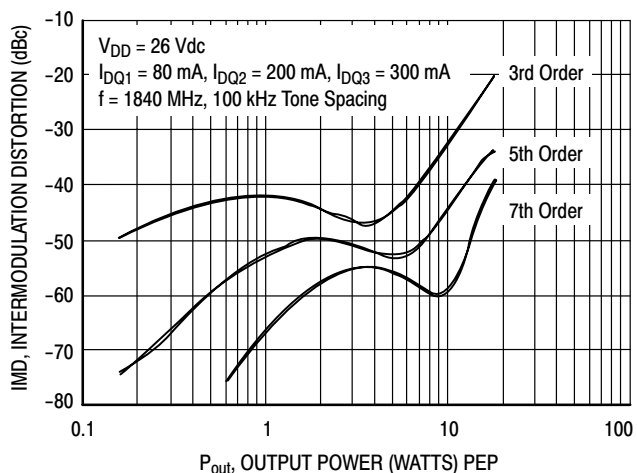


Figure 6. Intermodulation Distortion Products versus Output Power @ 1840 MHz

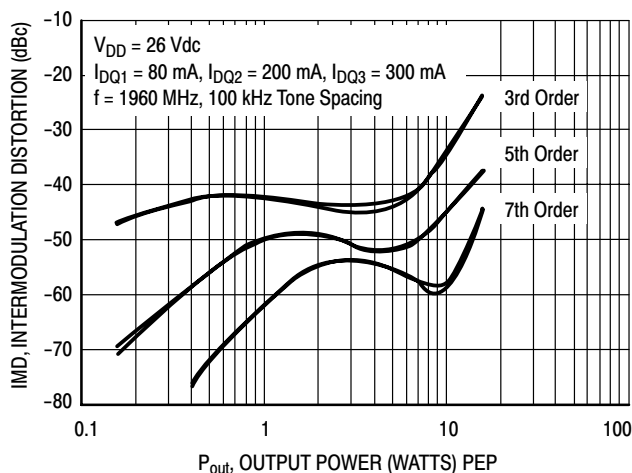


Figure 7. Intermodulation Distortion Products versus Output Power @ 1960 MHz

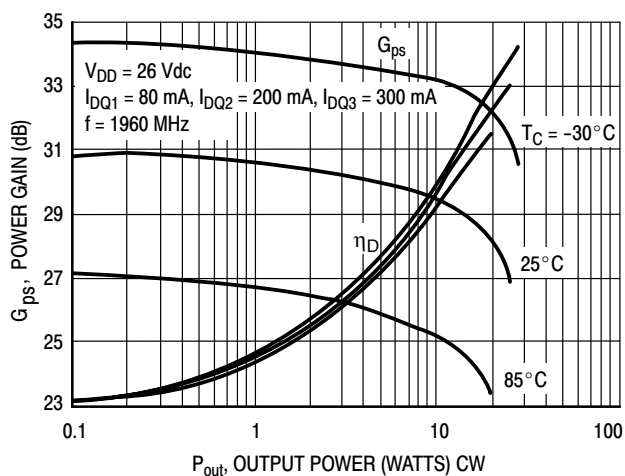


Figure 8. Power Gain and Drain Efficiency versus Output Power

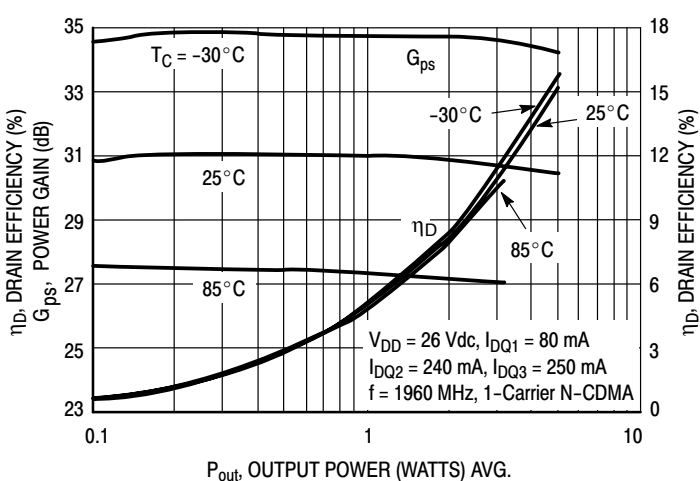
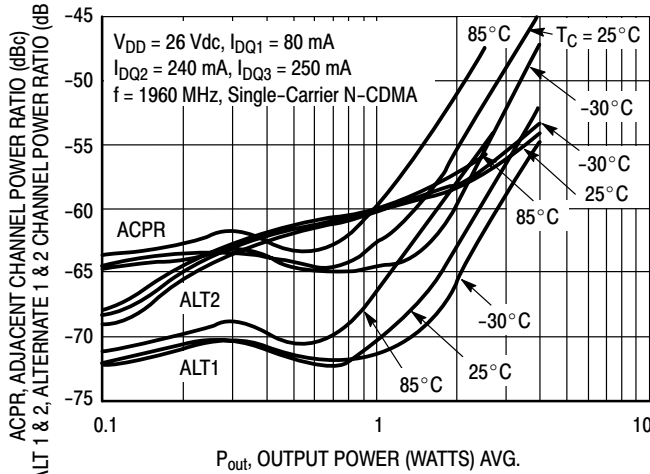
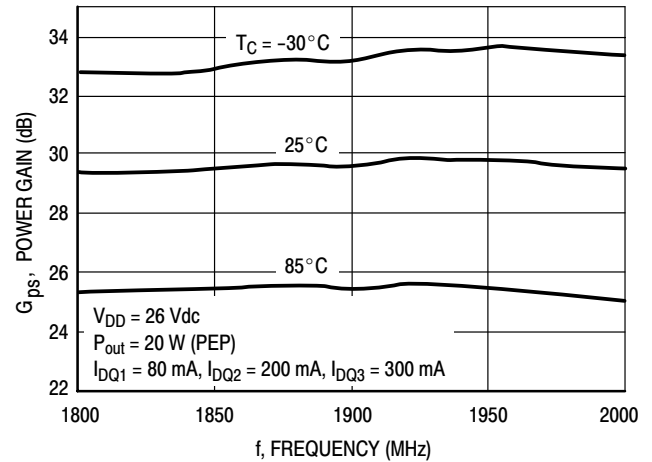


Figure 9. Power Gain and Drain Efficiency versus Output Power

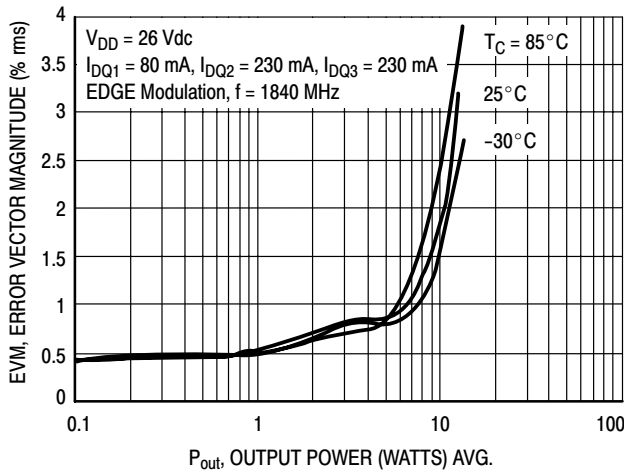
## TYPICAL CHARACTERISTICS



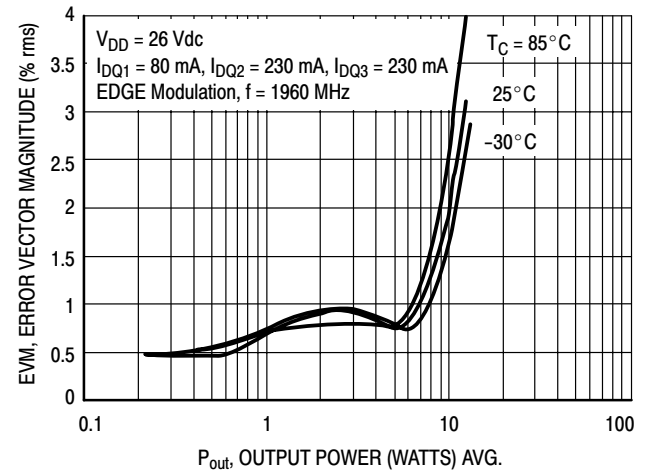
**Figure 10. Alternate Channel Power Ratio, Alternate 1 and 2 Channel Power Ratio versus Output Power**



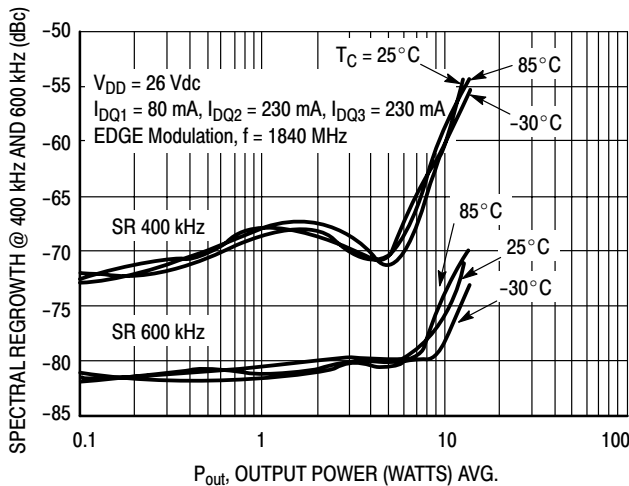
**Figure 11. Power Gain versus Frequency**



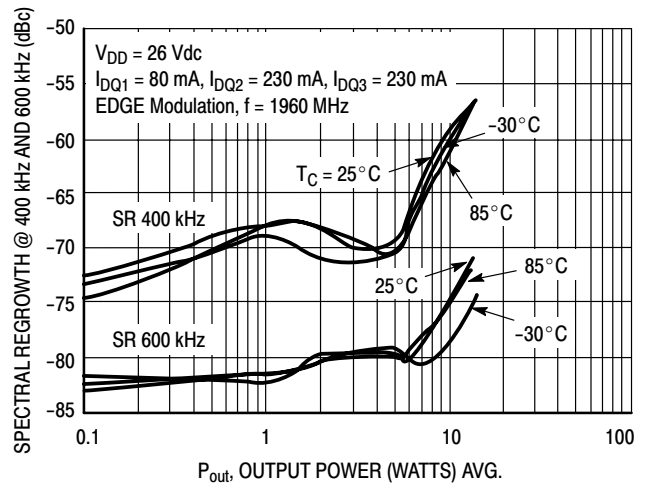
**Figure 12. EVM versus Output Power @ 1840 MHz**



**Figure 13. EVM versus Output Power @ 1960 MHz**



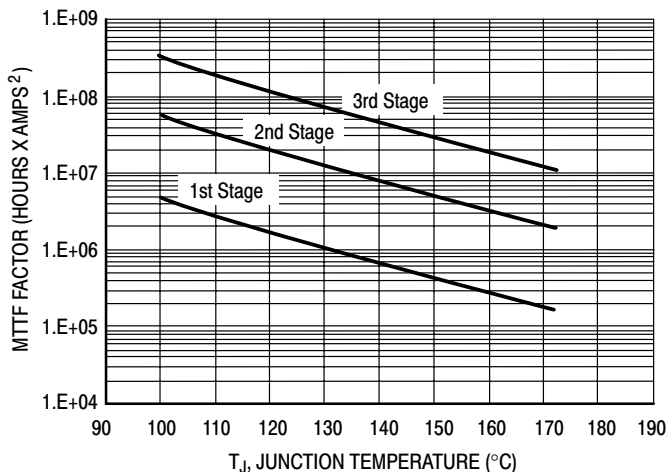
**Figure 14. Spectral Regrowth at 400 and 600 kHz versus Output Power @ 1840 MHz**



**Figure 15. Spectral Regrowth at 400 and 600 kHz versus Output Power @ 1960 MHz**

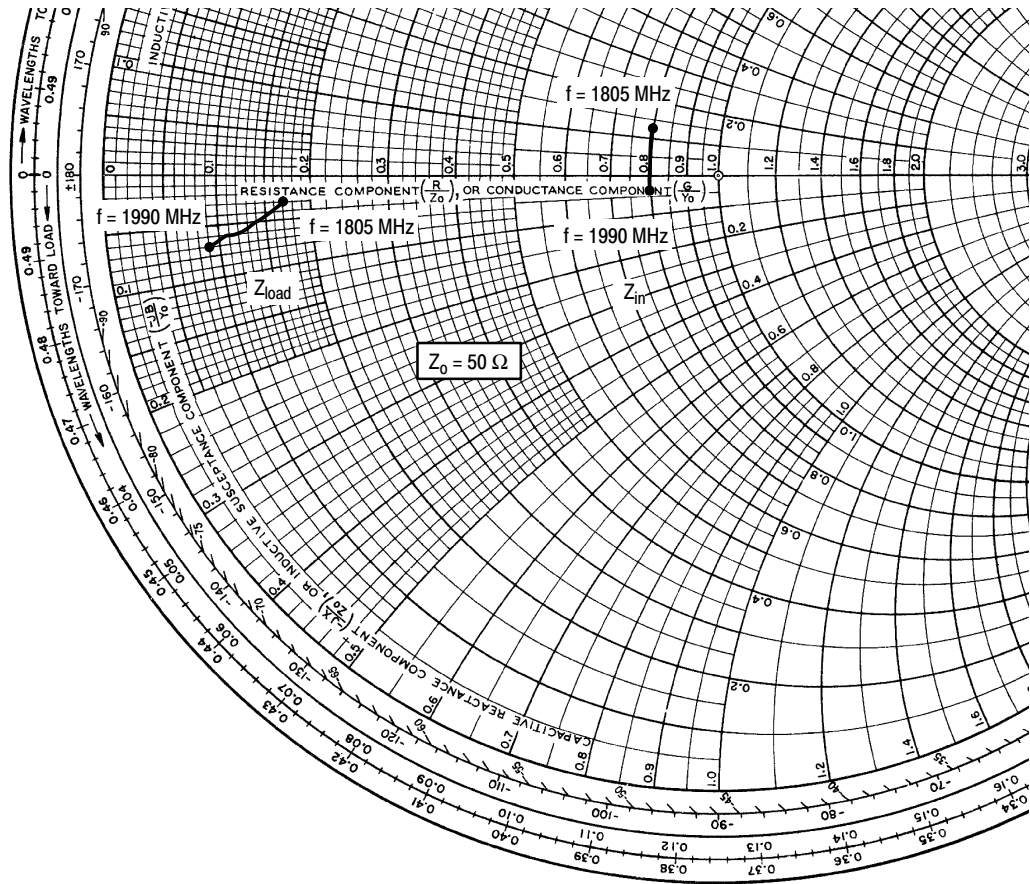


### TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x amperes<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 16. MTTF Factor versus Junction Temperature**



$V_{DD} = 26\text{ V}$ ,  $I_{DQ1} = 80\text{ mA}$ ,  $I_{DQ2} = 200\text{ mA}$ ,  $I_{DQ3} = 300\text{ mA}$ ,  $P_{out} = 20\text{ W PEP}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
1805	$40.00 + j6.50$	$8.75 - j1.42$
1842	$40.00 + j2.00$	$7.00 - j2.70$
1880	$40.00 - j1.50$	$5.90 - j2.97$
1930	$40.00 - j1.80$	$5.46 - j3.20$
1960	$40.00 - j2.10$	$4.30 - j3.35$
1990	$40.00 - j2.60$	$4.45 - j3.30$

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

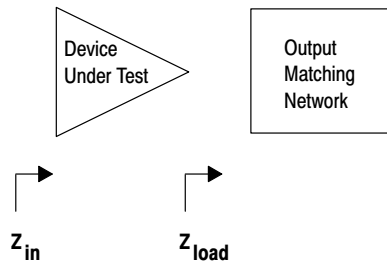
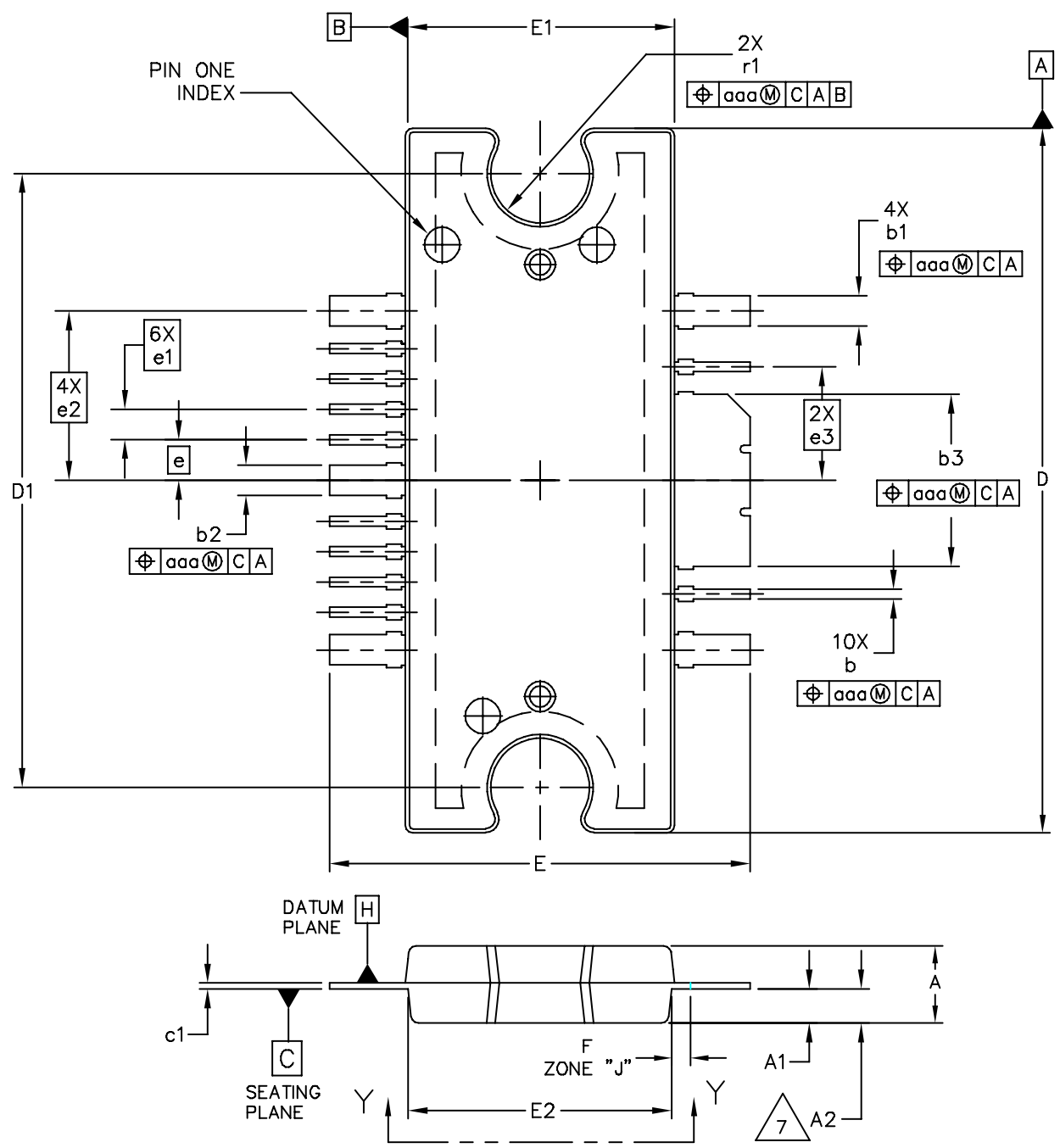
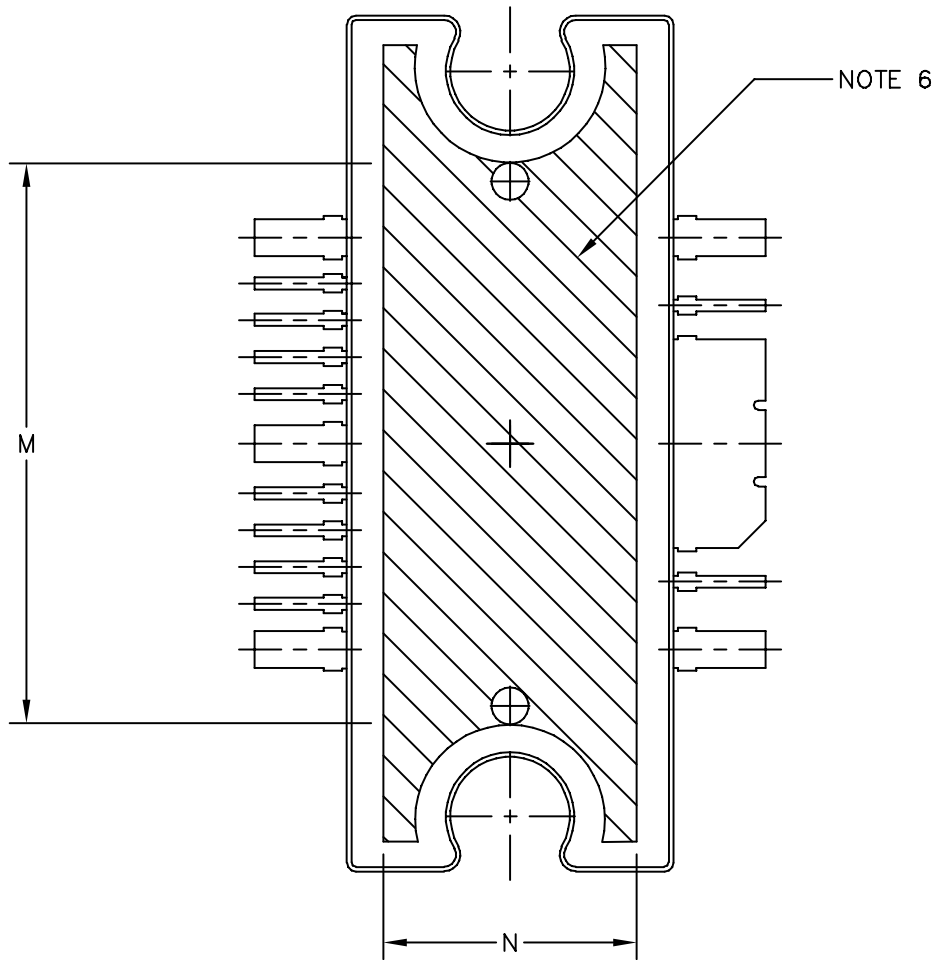


Figure 17. Series Equivalent Input and Load Impedance

**PACKAGE DIMENSIONS**



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	CASE NUMBER: 1329-09	13 MAR 2006	
	STANDARD: NON-JEDEC		



VIEW Y-Y

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	CASE NUMBER: 1329-09	13 MAR 2006	
	STANDARD: NON-JEDEC		

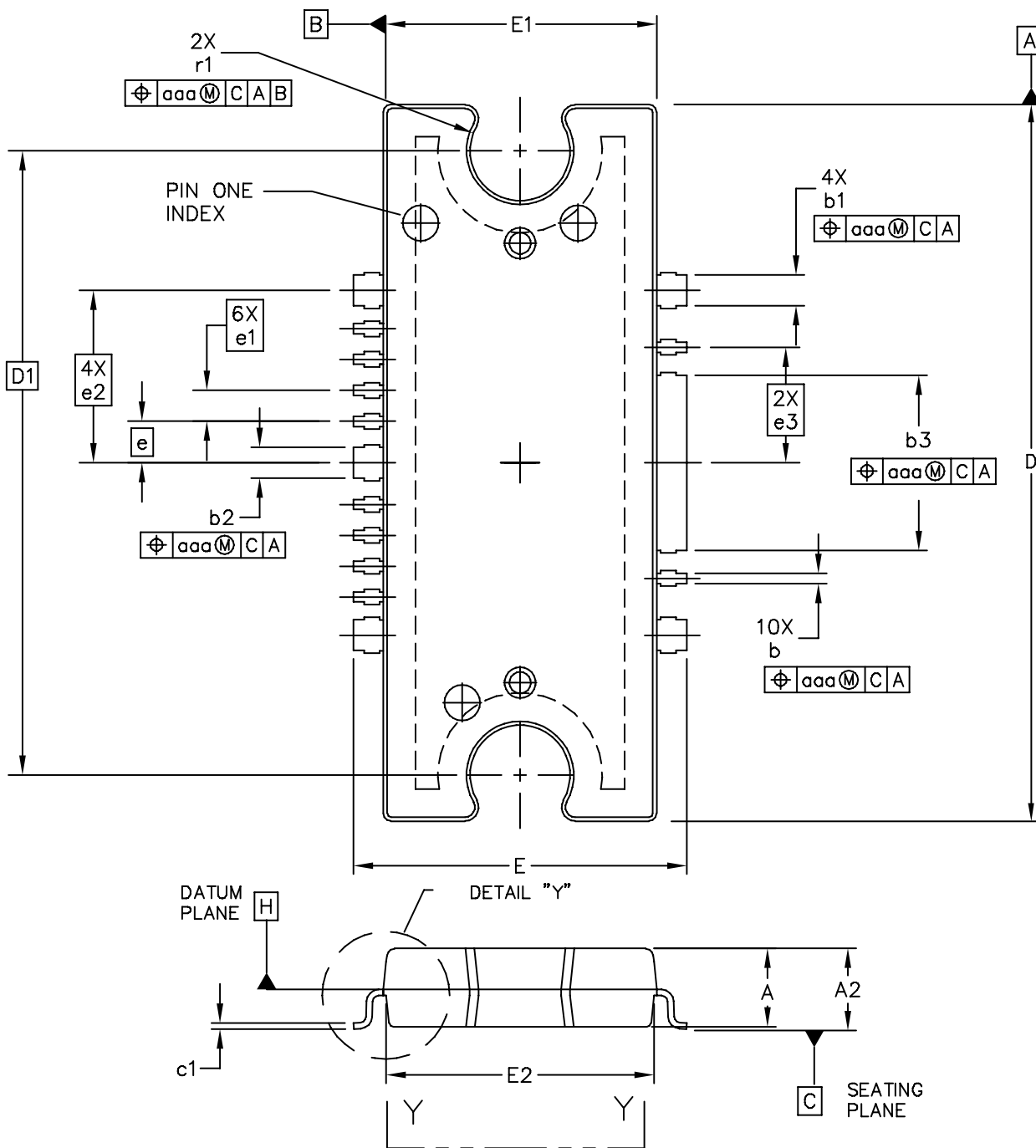
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

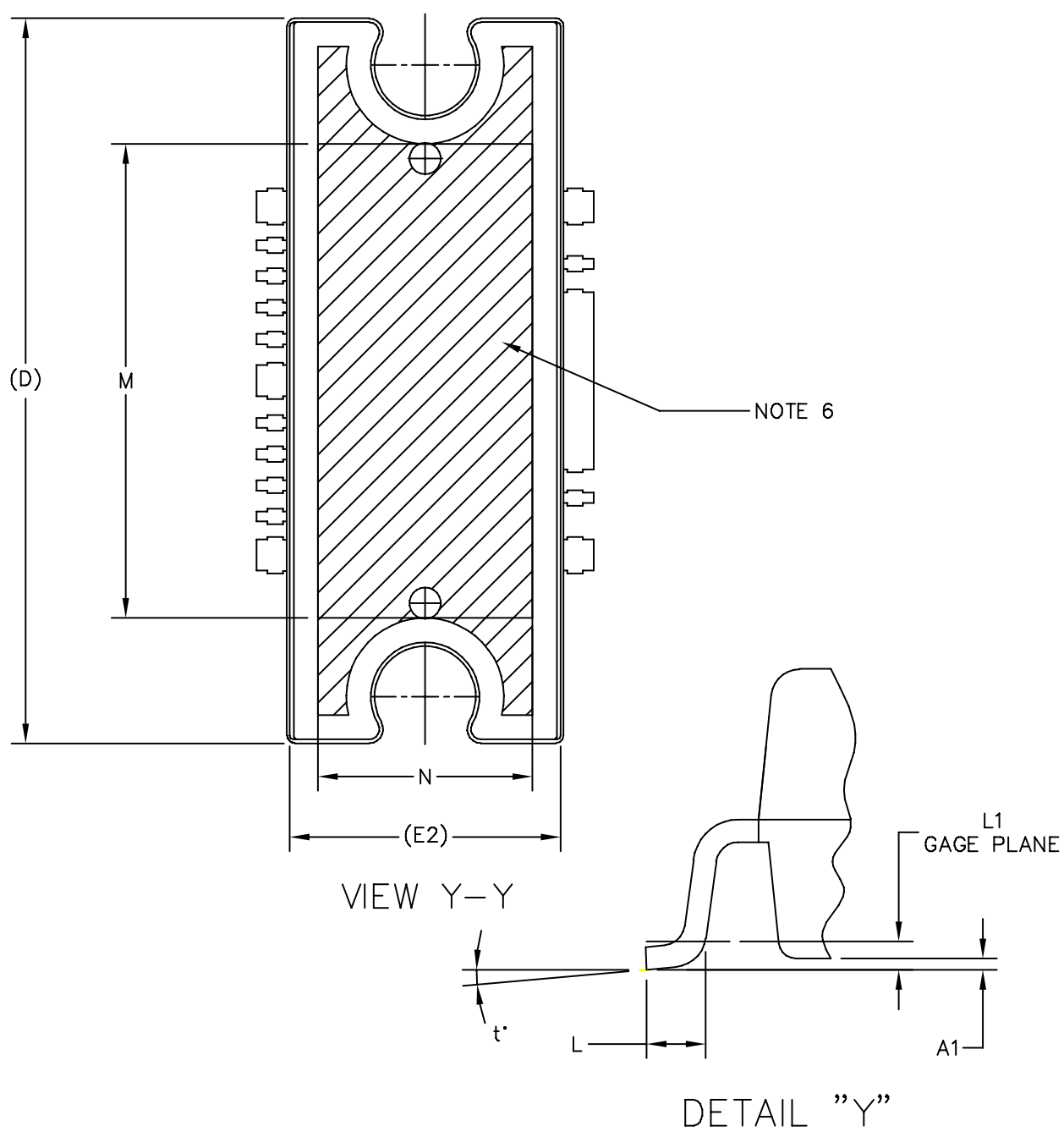
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	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	

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		CASE NUMBER: 1329-09		13 MAR 2006	
		STANDARD: NON-JEDEC			





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	CASE NUMBER: 1329A-03	3 APR 2006	
	STANDARD: NON-JEDEC		



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	CASE NUMBER: 1329A-03	3 APR 2006	
	STANDARD: NON-JEDEC		

NOTES:

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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	4.90	5.06	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		.025 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2'	8'	2'	8'
N	.270	----	6.86	----	aaa	.004		.10	

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			CASE NUMBER: 1329A-03		3 APR 2006
			STANDARD: NON-JEDEC		

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Technical Information Center  
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+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
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Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
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