Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Freescale Semiconductor
Data Sheet

Document Number: MWCT1000DS
Rev. 1.0, 02/2014

MWCT1000DS

Features

- Low power (5 W) solution for Wireless Power Consortium (WPC) compliant transmitter design
- Conforms to the latest version low power WPC specifications
- Supports wide DC input voltage range starting from 4.2 V, typically 5 V, 12 V and 19 V
- Integrated digital demodulation on chip
- Supports all types of receiver modulation strategies (AC capacitor, AC resistor and DC resistor)
- Supports Foreign Object Detection (FOD)
- Dynamic input power limit for limited input power supply, like USB power.
- Super low standby power (less than 25 mW) by Freescale Touch technology
- Supports any guided positioning single coil power transmitter solutions using frequency and duty cycle control
- LED & buzzer for system status indication
- Over-voltage/current/temperature protection
- Software based solution to provide maximum design freedom and product differentiation
- FreeMASTER GUI tool to enable configuration, calibration and debugging

Applications

- Low Power Wireless Power Transmitter
  Any guided positioning single coil solution with frequency & duty cycle control (WPC A types or customer properties)

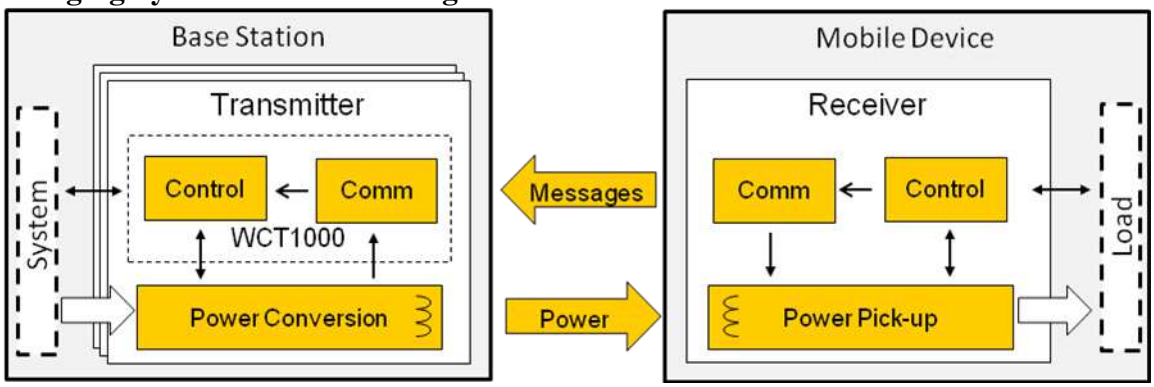
Overview Description

The WCT1000 is a wireless power transmitter controller that integrates all required functions for WPC “Qi” compliant wireless power transmitter design. It’s an intelligent device to work with Freescale touch sensing technology or use periodically analog PING (configurable by user) to detect a mobile device for charging while gaining super low standby power. Once the mobile device is detected, the WCT1000 controls the power transfer by adjusting operation frequency of power stage according to message packets sent by mobile device.

In order to maximize the design freedom and product differentiation, WCT1000 supports any low power guided positioning single coil power transmitter design (WPC types or customization) using operation frequency and duty cycle control by software based solutions. Besides, easy-to-use FreeMASTER GUI tool with configuration, calibration and debugging functions provides user-friendly design experience and speed time-to-market.

The WCT1000 includes digital demodulation module to reduce external components, over-voltage/current/ temperature protection and FOD method to protect from overheating by misplaced metallic foreign objects. It also handles any abnormal condition and operational status, and provides comprehensive indicator outputs for robust system design.

Wireless Charging System Functional Diagram



Contents

1 Absolute Maximum Ratings

1.1 Electrical Operating Ratings

Table 1. Absolute Maximum Electrical Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min.	Max.	Unit
Supply Voltage Range	V_{DD}		–0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		–0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		–0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		–0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	–0.3	5.5	V
RESET Input Voltage Range	V_{IN_RESET}	Pin Group 2	–0.3	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	–0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		–	–5.0	mA
Output clamp current, per pin[4]	V_{OC}		–	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		–25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1,2	–0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	–0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	–0.3	4.0	V
Ambient Temperature	T_A		–40	85	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		–55	150	°C

1. Default Mode:
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
2. Continuous clamp current.
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through an ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (= VSS–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

1.2 Thermal Handling Ratings

Table 2. Thermal Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	–	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life.*
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

1.3 ESD Handling Ratings

Table 3. ESD Handling Ratings

Characteristic[1]	Min.	Max.	Unit
ESD for Human Body Model (HBM)	-2000	+2000	V
ESD for Machine Model (MM)	-200	+200	V
ESD for Charge Device Model (CDM)	-500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	-100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

1.4 Moisture Handling Ratings

Table 4. Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

2 Electrical Characteristics

2.1 General Characteristics

Table 5. General Electrical Characteristics

Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)							
Characteristic	**Symbol**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Supply Voltage[2]	V_{DD} ,V_{DDA}		2.7	3.3	3.6	V	-
ADC Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA} -0.6		V_{DDA}	V	-
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V	-
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		-0.1	0	0.1	V	-
Input Voltage High (digital inputs)	V_{IH}	1 (Pin Group 1)	0.7×V_{DD}		5.5	V	-
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	1 (Pin Group 2)	0.7×V_{DD}	-	V_{DD}	V	-
Input Voltage Low (digital inputs)	V_{IL}	1 (Pin Group 1,2)			0.35×V_{DD}	V	-
Output Source Current High (at V_{OH} min.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	 1 (Pin Group 1) 1 (Pin Group 1)	 - -		 -2 -9	mA	
Output Source Current High (at V_{OL} max.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	 1 (Pin Group 1,2) 1 (Pin Group 1,2)	 - -		 2 9	mA	-
Output Voltage High	V_{OH}	1 (Pin Group 1)	V_{DD} -0.5	-	-	V	I_{OH} = I_{OHmax}
Output Voltage Low	V_{OL}	1 (Pin Group 1,2)	-	-	0.5	V	I_{OL} = I_{OLmax}
Digital Input Current High pull-up enabled or disabled	I_{IH}	1 (Pin Group 1)	-	0	+/-2.5	µA	V_{IN} = 2.4V to 5.5V
		1 (Pin Group 2)					V_{IN} = 2.4V to V_{DD}
Comparator Input Current High	I_{IHC}	1 (Pin Group 3)		0	+/-2	µA	V_{IN} = V_{DDA}

Internal Pull-Up Resistance	$R_{Pull-Up}$		20	-	50	kΩ	-
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	-	50	kΩ	-
Comparator Input Current Low	I_{ILC}	1 (Pin Group 3)	-	0	+/-2	µA	V_{IN} = 0V
Output Current[1] High Impedance State	I_{OZ}	1 (Pin Group 1,2)	-	0	+/-1	µA	-
Schmitt Trigger Input Hysteresis	V_{HYS}	1 (Pin Group 1,2)	0.06×V_{DD}	-	-	V	-
Input capacitance	C_{IN}		-	10	-	pF	-
Output capacitance	C_{OUT}		-	10	-	pF	-
GPIO pin interrupt pulse width[5]	T_{INT_Pulse}	6	1.5	-	-	Bus clock	-
Port rise and fall time (high drive strength). Slew disabled.	$T_{Port\_H\_DIS}$	7	5.5	-	15.1	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (high drive strength). Slew enabled.	$T_{Port\_H\_EN}$	7	1.5	-	6.8	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (low drive strength). Slew disabled.	$T_{Port\_L\_DIS}$	8	8.2	-	17.8	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (low drive strength). Slew enabled.	$T_{Port\_L\_EN}$	8	3.2	-	9.2	ns	2.7 ≤ VDD ≤ 3.6V
Device (system and core) clock frequency	f_{SYSCLK}		0.001	-	100	MHz	-
Bus clock	f_{BUS}		-	-	50	MHz	-

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
2. ADC specifications are not guaranteed when VDDA is below 3.0 V.
3. Total chip source or sink current cannot exceed 75mA.
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25mA.
5. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
6. The greater synchronous and asynchronous timing must be met.
7. 75 pF load
8. 15 pF load

2.2 Device Characteristics

Table 6. General Device Characteristics

Power Mode Transition Behavior					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
T_{S2R}	STOP mode to RUN mode	6.79	7.27	µs	1
$T_{LPS2LPR}$	LPS mode to LPRUN mode	240.9	551	µs	2
Reset and Interrupt Timing					
Symbol	**Characteristic**	**Min.**	**Max.**	**Unit**	**Notes**
t_{RA}	Minimum $\overline{\text{RESET}}$ Assertion Duration	16	-	ns	3
t_{RDA}	$\overline{\text{RESET}}$ desertion to First Address Fetch	865 × T_{OSC} + 8 × T_{SYSCLK}	-	ns	4
t_{IF}	Delay from Interrupt Assertion to Fetch of first instruction (exiting STOP mode)	361.3	570.9	ns	
PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{POR_A}	POR Assert Voltage[5]	-	2.0	-	V
V_{POR_R}	POR Release Voltage[6]	-	2.7	-	V
V_{LVI_2p7}	LVI_2p7 Threshold Voltage	-	2.73	-	V
V_{LVI_2p2}	LVI_2p2 Threshold Voltage	-	2.23	-	V
JTAG Timing					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
f_{OP}	TCK frequency of operation	DC	$f_{SYSCLK}/8$	MHz	
t_{PW}	TCK clock pulse width	50	-	ns	
t_{DS}	TMS, TDI data set-up time	5	-	ns	
t_{DH}	TMS, TDI data hold time	5	-	ns	
t_{DV}	TCK low to TDO data valid	-	30	ns	
t_{TS}	TCK low to TDO tri-state	-	30	ns	
Regulator 1.2 V Parameters					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**

V_{CAP}	Output Voltage[7]	-	1.22	-	V
I_{SS}	Short Circuit Current[8]	-	600	-	mA
T_{RSC}	Short Circuit Tolerance (VCAP shorted to ground)	-	-	30	Mins
V_{REF}	Reference Voltage (after trim)	-	1.21	-	V

Phase-Locked Loop Timing

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{Ref_PLL}	PLL input reference frequency[9]	8	8	16	MHz
f_{OP_PLL}	PLL output frequency[10]	200	-	400	MHz
t_{Lock_PLL}	PLL lock time[11]	35.5	-	73.2	µs
t_{DC_PLL}	Allowed Duty Cycle of input reference	40	50	60	%

Relaxation Oscillator Electrical Specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{ROSC_8M}	8 MHz Output Frequency[12] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C	 7.84 7.76 -	 8 8 405	 8.16 8.24 -	 MHz MHz kHz
$f_{ROSC\_8M\_Delta}$	8 MHz Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
f_{ROSC_200k}	200 kHz Output Frequency[13] RUN Mode • -40°C to 105°C	 194	 200	 206	 kHz
$f_{ROSC\_200k\_Delta}$	200 kHz Output Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 85°C • -40°C to 105°C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
t_{Stab}	Stabilization Time • 8 MHz output[14] • 200 kHz output[15]	 - -	 0.12 10	 - -	 µs µs
t_{DC_ROSC}	Output Duty Cycle	48	50	52	%

Flash Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
t_{hvpgm4}	Longword Program high-voltage time	-	7.5	18	µs
$t_{hversscr}$	Sector Erase high-voltage time[16]	-	13	113	ms
$t_{hversall}$	Erase All high-voltage time[16]	-	52	452	ms

$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)[17]	-	-	60	µs
t_{pgmchk}	Program Check execution time[17]	-	-	45	µs
t_{rdrsrc}	Read Resource execution time[17]	-	-	30	µs
t_{pgm4}	Program Longword execution time	-	65	145	µs
t_{ersscr}	Erase Flash Sector execution time[18]	-	14	114	ms
t_{rd1all}	Read 1s All Blocks execution time	-	-	0.9	ms
t_{rdonce}	Read Once execution time[17]	-	-	25	µs
$t_{pgmonce}$	Program Once execution time	-	65	-	µs
t_{ersall}	Erase All Blocks execution time[18]	-	70	575	ms
t_{vfykey}	Verify Backdoor Access Key execution time[17]	-	-	30	µs
$t_{flashretp10k}$	Data retention after up to 10 K cycles	5	50[19]	-	years
$t_{flashretp1k}$	Data retention after up to 1 K cycles	20	100[19]	-	years
$n_{flashcyc}$	Cycling endurance[20]	10 K	50 K[19]	-	cycles

12-bit ADC Electrical Specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage[21]	3	3.3	3.6	V
f_{ADCCLK}	ADC conversion clock[22]	0.1	-	10	MHz
R_{ADC}	Conversion range with single-ended/unipolar[23]	V_{REFL}	-	V_{REFH}	V
V_{ADCIN}	Input voltage range (per input) with internal reference[24]	0	-	V_{DDA}	V
t_{ADC}	Conversion time[25]	-	8	-	t_{ADCCLK}
t_{ADCPU}	ADC power-up time (from adc_pdn)	-	13	-	t_{ADCCLK}
I_{ADCRUN}	ADC RUN current (per ADC block)	-	1.8	-	mA
INL_{ADC}	Integral non-linearity[26]	-	+/- 1.5	+/- 2.2	LSB[27]
DNL_{ADC}	Differential non-linearity[26]	-	+/- 0.5	+/- 0.8	LSB[27]
E_{GAIN}	Gain Error	-	0.996 to 1.004	0.99 to 1.101	-
ENOB	Effective number of bits	-	10.6	-	bits
I_{INJ}	Input injection current[28]	-	-	+/-3	mA
C_{ADCI}	Input sampling capacitance	-	4.8	-	pF

Comparator and 6-bit DAC Electrical Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	-	3.6	V
I_{DDHS}	Supply current, High-speed mode(EN=1, PMODE=1)	-	300	-	µA
I_{DDLS}	Supply current, Low-speed mode(EN=1, PMODE=0)	-	36	-	µA
V_{AIN}	Analog input voltage	V_{ss}	-	V_{DD}	V

V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[29] • CR0[HYSTCTR]=00 • CR0[HYSTCTR]=01 • CR0[HYSTCTR]=10 • CR0[HYSTCTR]=11	- - - -	5 25 55 80	13 48 105 148	mV mV mV mV
V_{CMPOh}	Output high	V_{DD} -0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode(EN=1, PMODE=1)[30]	-	25	50	ns
t_{DLS}	Propagation delay, low-speed mode(EN=1, PMODE=0) [30]	-	60	200	ns
t_{DInit}	Analog comparator initialization delay[31]	-	40	-	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
R_{DAC6b}	6-bit DAC reference inputs	V_{DDA}	-	V_{DD}	V
INL_{DAC6b}	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[32]
DNL_{DAC6b}	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB

PWM Timing Parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{PWM}	PWM clock frequency[33,34]	-	100	-	MHz
S_{PWMNEP}	NanoEdge Placement (NEP) step size	-	312	-	ps
t_{DFLT}	Delay for fault input activating to PWM output deactivated	1	-	-	ns
t_{PWMPU}	Power-up time[35]	-	25	-	µs

Timer Timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
P_{IN}	Timer input period	$2T_{timer}$ + 6	-	ns	36
P_{INHL}	Timer input high/low period	$1T_{timer}$ + 3	-	ns	36
P_{OUT}	Timer output period	$2T_{timer}$ - 2	-	ns	36
P_{OUTHL}	Timer output high/low period	$1T_{timer}$ - 2	-	ns	36

SCI Timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{SCI}	Baud rate	-	(f_{MAX_SCI} /16)	Mbit/s	37
PW_{RXD}	RXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	ns	
PW_{TXD}	TXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	ns	

IIC Timing							
Symbol	Characteristic	Min.		Max.		Unit	Notes
		Min.	Max.	Min.	Max.		
f_{SCL}	SCL clock frequency	0	100	0	400	kHz	
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs	
t_{SCL_LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs	
t_{SCL_HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs	
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs	
t_{HD_DAT}	Data hold time for IIC bus devices	0[38]	3.45[39]	0[40]	0.9[38]	µs	
t_{SU_DAT}	Data set-up time	250[41]	-	100[42]	-	ns	
t_r	Rise time of SDA and SCL signals	-	1000	$20 + 0.1C_b$	300	ns	43
t_f	Fall time of SDA and SCL signals	-	300	$20 + 0.1C_b$	300	ns	42, 43
t_{SU_STOP}	Set-up time for STOP condition	4	-	0.6	-	µs	
t_{BUS_Free}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	ns	

1. Clock configuration: CPU and system clocks= 100 MHz; Bus Clock = 100 MHz.
2. CPU clock = 200 kHz and 8 MHz IRC on standby.
3. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.
4. TOSC means oscillator clock cycle; TSYSCLK means system clock cycle.
5. During 3.3 V VDD power supply ramp down
6. During 3.3 V VDD power supply ramp up (gated by LVI_2p7)
7. Value is after trim
8. Guaranteed by design
9. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
10. The frequency of the core system clock cannot exceed 50 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
11. This is the time required after the PLL is enabled to ensure reliable operation.
12. Frequency after application of 8 MHz trimmed.
13. Frequency after application of 200 kHz trimmed.
14. Standby to run mode transition.
15. Power down to run mode transition.
16. Maximum time based on expectations at cycling end-of-life.
17. Assumes 25 MHz flash clock frequency.
18. Maximum times for erase parameters based on expectations at cycling end-of-life.
19. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
20. Cycling endurance represents number of program/erase cycles at -40°C ≤ Tj ≤ 125°C.
21. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed.
22. ADC clock duty cycle is 45% ~ 55%.
23. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
24. In unipolar mode, positive input must be ensured to be always greater than negative input.
25. First conversion takes 10 clock cycles.

26. INLADC/DNLADC is measured from VADCIN = VREFL to VADCIN = VREFH using Histogram method at x1 gain setting.
27. Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 gain setting.
28. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC.
29. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD-0.6V.
30. Signal swing is 100 mV.
31. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
32. 1 LSB = Vreference/64.
33. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
34. Temperature and voltage variations do not affect NanoEdge Placement step size.
35. Powerdown to NanoEdge mode transition.
36. Ttimer = Timer input clock cycle. For 100 MHz operation, Ttimer = 10 ns.
37. fMAX_SCI is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max. 50 MHz depending on part number) or 2x bus clock (max. 100 MHz) for the device.
38. The master mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
39. The maximum tHD_DAT must be met only if the device does not stretch the LOW period (tSCL_LOW) of the SCL signal.
40. Input signal Slew = 10 ns and Output Load = 50 pF
41. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
42. A Fast mode IIC bus device can be used in a Standard mode IIC bus system, but the requirement tSU_DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU_DAT = 1000 + 250 = 1250ns (according to the Standard mode I2C bus specification) before the SCL line is released.
43. Cb = total capacitance of the one bus line in pF.

2.3 Thermal Operating Characteristics

Table 7. General Thermal Characteristics

Symbol	Description	Min	Max	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature	-40	85	°C

3 Typical Performance Characteristics

3.1 System Efficiency

The typical maximum system efficiency (Rx output power vs. Tx input power) on WCT1000 solution with standard receiver (aka Rx, bq51013AEVM-764) is more than 75%.

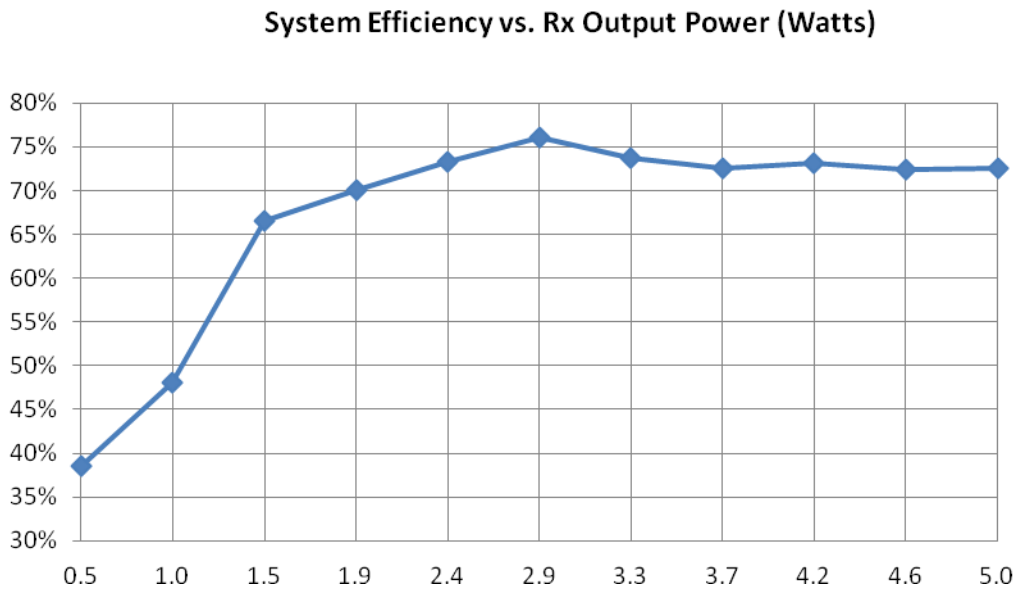


Figure 1. System Efficiency on WCT1000 Solution

Note: Power components are the main factor to determine the system efficiency, such as drivers and MOSFETs. The efficiency data in figure 1 is obtained on Freescale reference solution with A11 configuration.

3.2 Standby Power

WCT1000 solution only consumes the very low standby power with the special low power control method, and can further achieve ultra low standby power by using the touch sensor technology. (Freescale reference solution with A11 configuration uses Freescale Touch Sensor IC MPR121).

Transmitter (aka Tx) power consumption in standby mode: < 12 mA (60 mW with 5 V DC input)

Transmitter power consumption in standby mode with Touch Sensor technology: < 5 mA (25 mW with 5 V DC input)

3.3 Digital Demodulation

WCT1000 solution employs digital demodulation algorithm to communicate with Rx. This method can achieve high performance, low cost, very simple coil signal sensing circuit with less component number.

3.4 Foreign Object Detection

WCT1000 solution uses flexible, intelligent, and easy-to-use FOD algorithm to assure accurate foreign metal objects detection. With Freescale FreeMASTER GUI tool, FOD algorithm can be easily calibrated to get accurate power loss information especially for very sensitive foreign objects. On Freescale reference solution, the calculated power loss resolution between transmitted power and received power is less than 100 mW.

3.5 Dynamic Input Power Limit

When Tx is powered by a limited power supply, such as USB power, WCT1000 can limit the Tx output power and provide necessary margin relative to the input power supply capability. By monitoring the input voltage and input current of Tx, when it drops to a specified level and still positive Control Error Packet (CEP) is received, WCT1000 will stop increasing power output and control Tx operating in input power limit status. Users can know the system is in DIPL control mode by LED indication, LED1 and LED2 will be in fast blinking mode when input power is limited. WCT1000 will exit DIPL control mode and return to normal PID control mode if a negative Control Error Packet (CEP) is received to reduce output power. The input voltage level for DIPL control can be configured in the WCT1000 example project.

4 Device Information

4.1 Functional Block Diagram

From Figure 2, the low power feature with Freescale touch technology is optional according to user requirements for minimizing standby power. When this function is not deployed, its pins can be configured for other purpose of use. Besides, 11 pins (dashed) are also configurable for different design requirements to provide design freedom and differentiation.

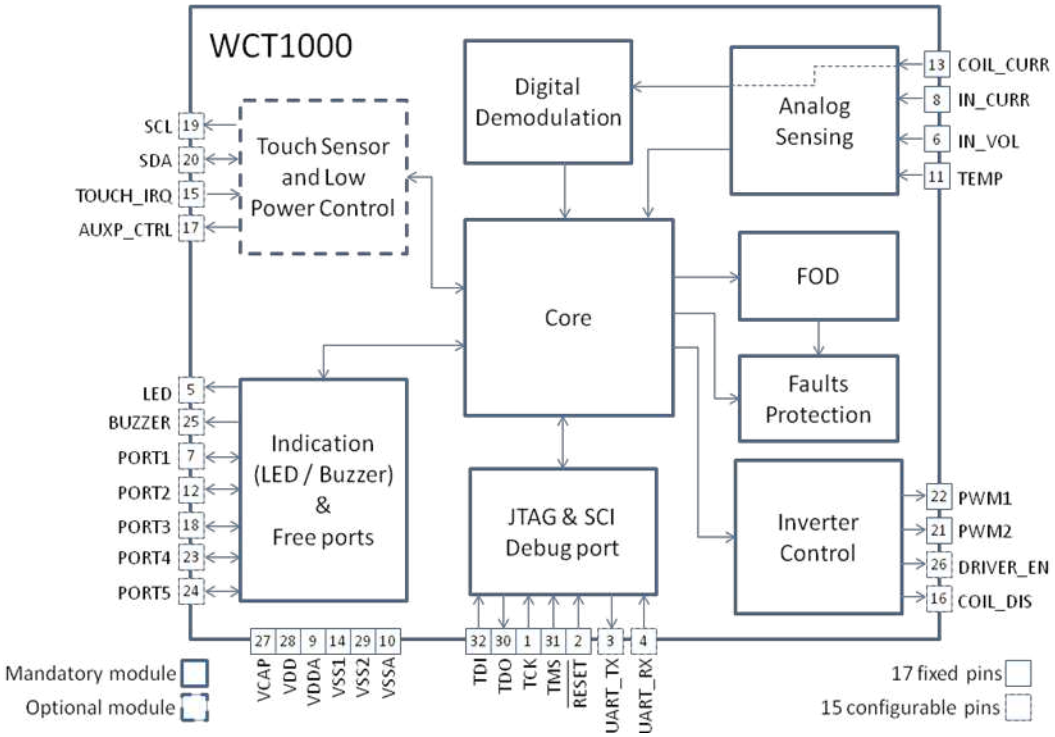


Figure 2. WCT1000 Function Block Diagram

4.2 Pinout Diagram

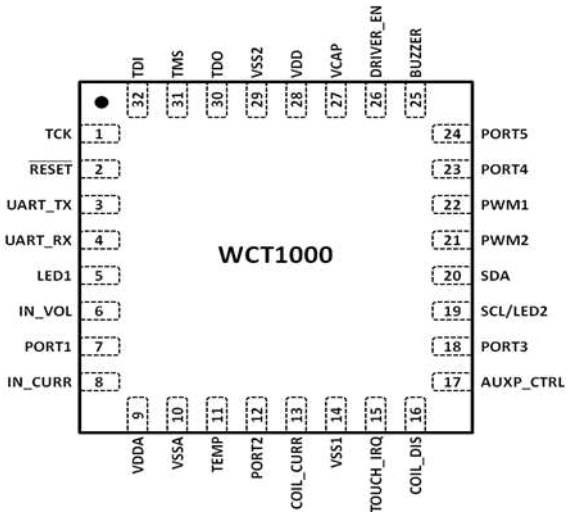


Figure 3. WCT1000 Pin Configuration (32-pin QFN)

4.3 Pin Function Description

By default, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through FreeMASTER GUI tool.

Table 8. Pin Signal Descriptions

Signal Name	Pin No.	Type	Function Description
TCK	1	Input	Test clock input, connected internally to a pull-up resistor
$\overline{\text{RESET}}$	2	Input	A direct hardware reset, when RESET is asserted low, device is initialized and placed in the reset state. Connect a pull-up resistor and decoupling capacitor
UART_TX	3	Output	UART transmit data output
		Input/Output	General purpose input/output pin
UART_RX	4	Input	UART receive data input
		Input/Output	General purpose input/output pin
LED1	5	Output	LED drive output for system status indicator
		Input/Output	General purpose input/output pin
IN_VOL	6	Input	Input voltage detection, analog input pin
PORT1	7	Input/Output	General purpose input/output pin
		Input	Analog signal detection input pin
IN_CURR	8	Input	Input current detection, analog input pin
VDDA	9	Supply	Analog power to on-chip analog module
VSSA	10	Supply	Analog ground to on-chip analog module
TEMP	11	Input	Board temperature detection, analog input pin
PORT2	12	Input/Output	General purpose input/output pin
		Input	Analog signal detection input pin
COIL_CURR	13	Input	Primary coil current detection, analog input pin
VSS1	14	Supply	Digital ground to on-chip digital module
TOUCH_IRQ	15	Input	External interrupt event input to wake up chip, active: low level; inactive: high level
		Input/Output	General purpose input/output pin
COIL_DIS	16	Output	Primary coil discharging enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
AUXP_CTRL	17	Output	Auxiliary power control pin, connect: high level; disconnect: low level
		Input/Output	General purpose input/output pin
PORT3	18	Input/Output	General purpose input/output pin

SCL/LED2	19	Input/Open-drain output	IIC serial clock
		Output	LED drive output for system status indicator
SDA	20	Input/Open-drain output	IIC serial data line
		Input/Output	General purpose input/output pin
PWM2	21	Output	PWM output 2, control one half of inverter bridge
PWM1	22	Output	PWM output 1, control another half of inverter bridge
PORT4	23	Input/Output	General purpose input/output pin
PORT5	24	Input/Output	General purpose input/output pin
BUZZER	25	Output	AC Buzzer drive control for system status indicator
		Input/Output	General purpose input/output pin
DRIVER_EN	26	Output	Pre-driver chip output enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
VCAP	27	Supply	Connect a 2.2μF or greater bypass capacitor between this pin and VSS
VDD	28	Supply	Digital power to on-chip digital module
VSS2	29	Supply	Digital ground to on-chip digital module
TDO	30	Output	Test data output
TMS	31	Input	Test mode select input, connect a pull-up resistor to VDD
TDI	32	Input	Test data input, connected internally to a pull-up resistor

4.4 Ordering Information

Table 9 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order this device.

Table 9. WCT1000 Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Ambient Temp.	Order Number
MWCT1000	2.7 to 3.6V	Quad Flat No-leaded (QFN)	32	-40 to +85°C	MWCT1000CFM

4.5 Package Outline Drawing

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number of 98ASA00473D.

5 Wireless Charging System Operation Principle

5.1 Fundamentals

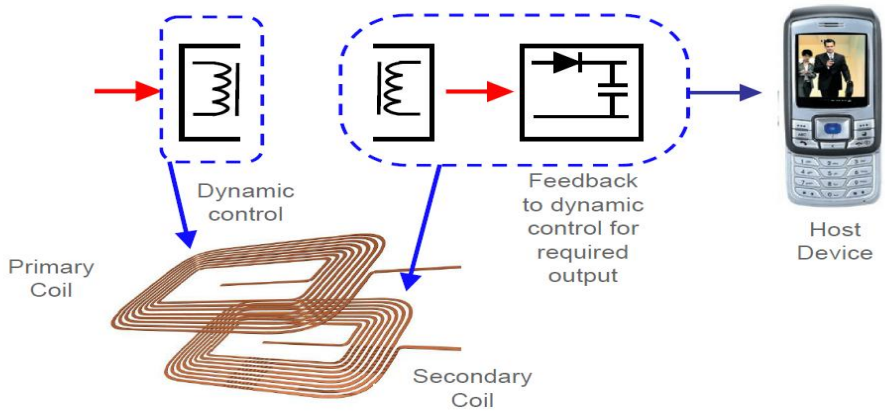


Figure 4. Working Principle of Wireless Charging System

The Wireless Charging system works as the digital switched mode power supply with the transformer, which is separated into two parts: The transformer primary coil is on the transmitter, working as the Tx coil, and the transformer secondary coil is on the receiver side as the Rx coil. The basic system working principle diagram is shown in Figure 4. As this system works based on magnetic induction, the better coupling between the Tx coil and Rx coil gain better system efficiency, so the Rx coil should be closely and center aligned with the Tx coil as possible. After the Rx coil receives the power from the Tx coil by magnetic field, it regulates the received voltage to power the load, and send its operational information to Tx according to specific protocol by the communication link. Then the system can achieve the closed-loop control, and power the load stably and wirelessly.

5.2 Power Transfer

When the wireless charging receiver is centrally placed on the transmitter coil, and, at the same time, the required conditions are met, the power transfer starts.

- The Tx coil and Rx coil meet proper specifications, such as the inductance, coil dimensions, coil materials, and magnets shielding.
- The distance is in suitable range (less than 6 mm for Z axis) between the Tx coil and Rx coil.
- The Rx coil should be in the active area of the Tx charging surface, which still means that the Tx coil and Rx coil should be coupled well. Coils' coupling will highly impact the power transfer efficiency, and good coupling can achieve high efficiency.

The coil shielding is also important, because the magnetic field leaking into the air will not transfer the power from Tx to Rx, and the shielding can contain the magnetic field as much as possible to improve the system efficiency and avoid bad effect of the nearby objects from interference. The shielding should be designed to place at the back of the Tx coil and Rx coil.

The power transfer must function correctly under the conditions when the Rx coil is on the Tx charging area during the overall system operational phases. To facilitate power transfer control, set the system operating frequency on the right side of resonant frequency of resonant network (because resonant converter works in a soft-switching mode when its operational frequency is over the resonant frequency and its output power changes monotonously with the adjustment of the operational frequency).

For WPC specification, the “Qi” defines the coil inductance and resonant capacitance, the resonant frequency is fixed as 100 kHz, then power transfer can work normally by adjusting the Tx operating frequency from 110 kHz to 205 kHz with fixed 50% duty cycle. The higher operating frequency means lower power transferred to Rx, and lower operating frequency means higher power transferred to Rx. The duty cycle will decrease when the operating frequency reaches to 205 kHz. Figure 5 shows the voltage gain (voltage on resonant inductor vs. the input voltage) change with operating frequency, as we can see voltage gain will increase when the operating frequency decreases.

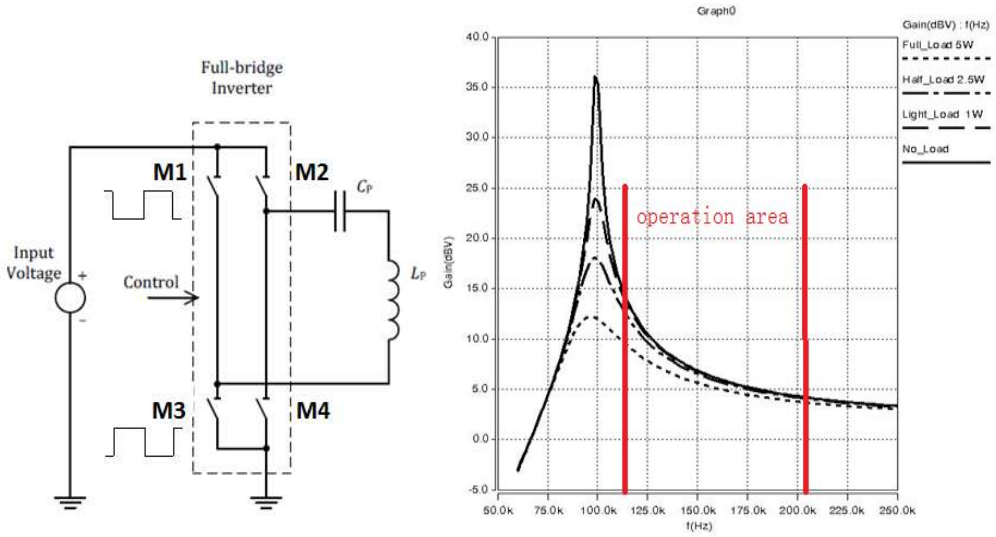


Figure 5. LC Parallel Resonant Converter Control Principle

5.3 Communication

5.3.1 Modulator

In low power wireless charging application, there is only one-way communication link between the receiver and the transmitter, and the receiver sends the information to transmitter by communication packages. The information includes the power requirements, received power, receiver ID and version, receiver power ratings, and charging end command, etc.

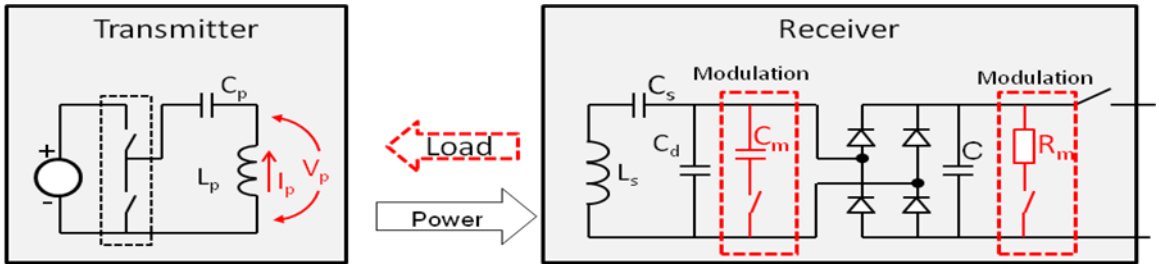


Figure 6. Load Modulation Scheme

Figure 6 shows the modulation technologies at the Rx side. Rx modulates load by switching modulation resistor (R_m, AC side or DC side), or modulation capacitor (C_m, AC side). The amplitude of voltage/current on Rx coil is modulated through connecting or disconnecting modulation load (resistor or capacitor). The amplitude of voltage/current on Tx coil is also modulated to reflect load switching through magnetic induction. Then Tx demodulates the sensed amplitude change of current (ΔI_p > 15mA), or voltage (ΔV_p > 200mV) on Tx coil. Figure 7 shows how the Rx switching modulation capacitor affects the Tx resonant characteristics (Gain vs. Frequency characteristics).

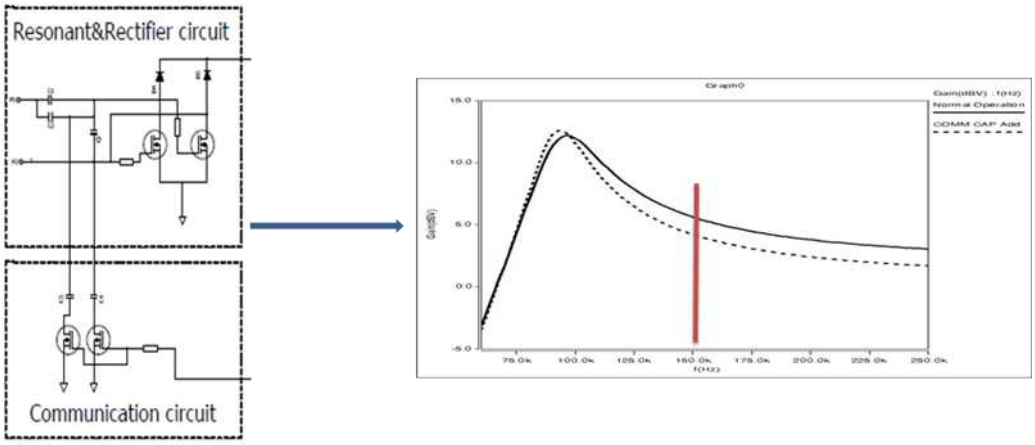


Figure 7. Load Modulation Principle

The Bode diagram in Figure 7 shows that the voltage amplitude on the Tx coil will decrease when the modulation capacitor is connected on the Rx side, the Rx couples the communication signal onto the power signal through modulating power signal directly. WPC defines the modulation baud rate to 2 kbps.

5.3.2 Demodulator

As the Rx modulates the communication signal on the power signal, the Tx has to demodulate communication signal from power signal to get the correct information sent by Rx, and further control the whole system operation. Figure 8 shows the power signal (voltage) waveform coupled with communication signal on Tx coil.

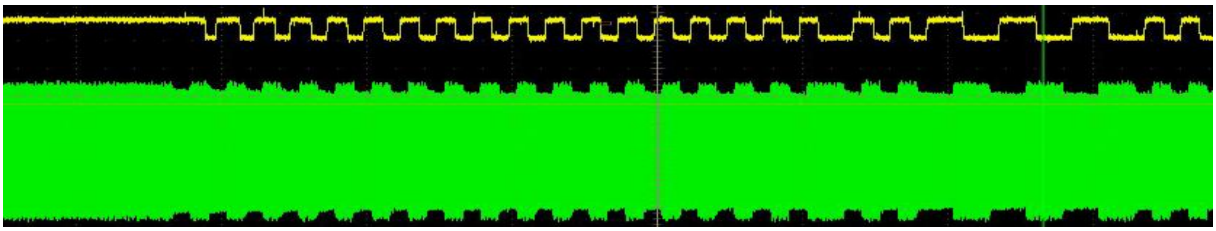


Figure 8. Tx Coil Voltage Profile with Rx Modulation

WCT1000 employs software solution to implement demodulator, also called digital demodulation technology. WCT1000 directly senses the voltage on resonant capacitor through the very simple, low cost RC circuit (Figure 9), and the high speed 12-bit cyclic ADC is capable of handling the maximum 205 kHz signal in time to assure accurate signal sampling. After the resonant capacitors voltage value is obtained, the equivalent resonant current in the coil can be calculated, and this coil current is used for the digital demodulation algorithm. After that, WCT1000 decodes the demodulated information to get the accurate communication message. Besides, the calculated coil current is also used for the FOD algorithm.

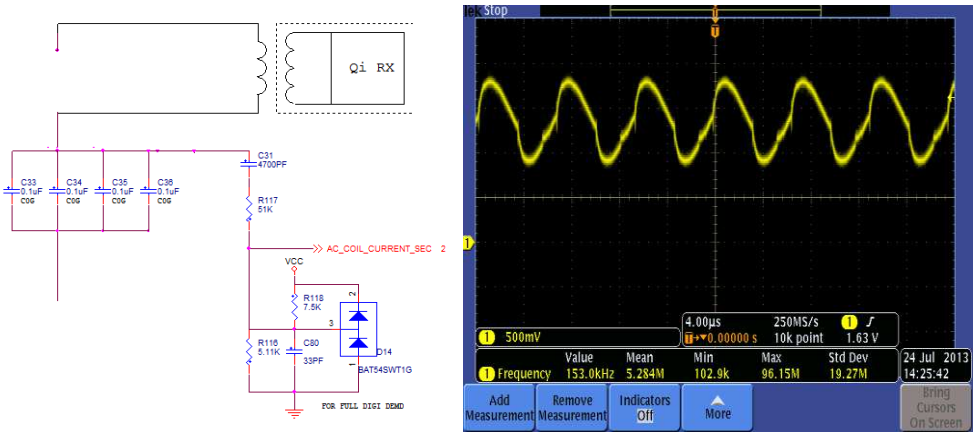


Figure 9. Sensing Circuit and Waveform of Tx Resonant Capacitor Voltage

With Freescale digital demodulation algorithm, WCT1000 can support all available modulation methods on the Rx, such AC resistor, DC resistor, or AC capacitor, and pass all compliance tests defined in the WPC specifications.

5.3.3 Message Encoding Scheme

The WCT1000 demodulates and decodes the message sent from Rx that is encoded by the differential bi-phase scheme. A logic ONE bit is encoded using two transitions in the 2 kHz clock period (500 us), and a logic ZERO bit using one transition. One 8-bit data, one Start bit, one Parity bit and one Stop bit compose one message byte. A typical packet consists of four parts, namely a preamble ($\geq$ 11 bits), a header (1 byte), a message (1 to 27 bytes), and a checksum (1 byte). Figure 10 shows the detailed message encoding scheme that WPC defines. Digital demodulation module in WCT1000 extracts the digital encoded communication signal from the analog power signal. The decoding module packs up the demodulated bits into message byte, and then message packet, which is processed by the system State Machine.

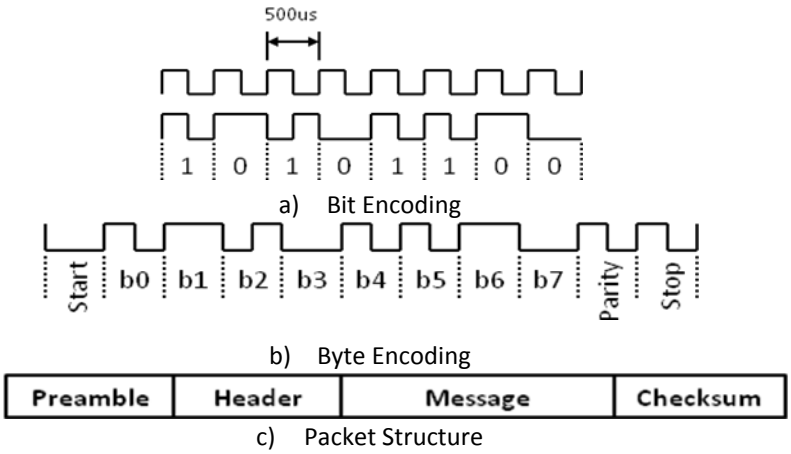


Figure 10. WPC Communication Message Encoding Scheme

5.4 System Control State Machine

WCT1000 embeds a WPC "Qi" State Machine to process received communication message from Rx and control power transfer to Rx. The overall system behavior between transmitter and receiver is controlled by the state machine shown here:

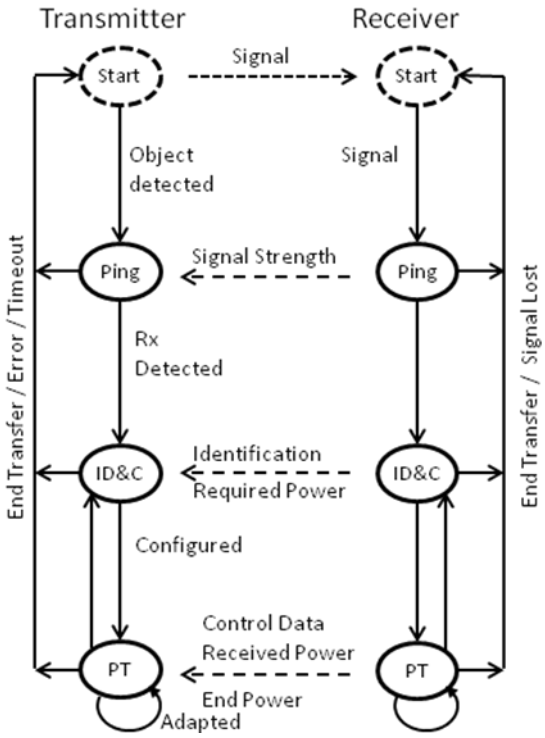


Figure 11. WPC Wireless Charging System State Machine

5.4.1 Selection Phase

In the Selection phase, the Tx system runs in low power mode to judge whether an object is placed on the Tx coil surface. The PING operation runs every 400 ms, and during the PING interval, the system is in Selection phase. If the touch sensor module is enabled, WCT1000 enters deep low power mode as described in the Standby Power section.

5.4.2 Ping Phase

In the Ping phase, the Tx system works on both analog PING and digital PING to detect a receiver placed on the Tx charging area. The analog PING time is far shorter than the digital PING for power-saving purposes. The analog PING enables a very short AC pulse on the Tx coil, WCT1000 reads back the coil current and compares it with the predefined current change threshold to judge whether an object is put on. The default coil current change threshold is 5%, which the user can set in FreeMASTER GUI to get good sensitivity.

For digital PING, the Tx system applies a power signal at 175 kHz with 50% duty cycle to attempt to set up communication with Rx. In response, Rx must send out the Signal Strength packet. Signal Strength message indicates the degree of coupling between Tx coil and Rx coil, and is the percentage of rectifier output signal against the possible maximum PING signal.

$$\text{Signal Strength Value} = \frac{U}{U_{max}} \times 256$$

In this formula, U is the monitored variable, and U_{max} is the maximum value, which the Rx expects for during digital PING.

When the Signal Strength packet is received in the Ping phase, the system enters the Identification & Configuration phase.

5.4.3 Identification & Configuration Phase

In the Identification & Configuration phase, the Tx system continues to identify the receiver device and collects the configuration information for a power transfer setup.

Required packets in the Identification & Configuration phase:

- Identification packet (0x71)
- Extended Identification packet (0x81)*
- Configuration packet (0x51)

* If Ext bit of Identification packet is set to 1.

The system must receive these packets in order:

- Identification packet (0x71)
- Extended Identification packet (0x81)
- Up to 7 optional configuration packets (0x51)