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MWCT101XSF

MWCT101XS Data Sheet

Key Features

- Operating characteristics
  - Voltage range: 2.7 V to 5.5 V
  - Ambient temperature range: -40 °C to 105 °C for HSRUN, -40 °C to 125 °C for RUN
- Arm™ Cortex-M4F core, 32-bit CPU
  - Supports up to 112 MHz frequency (HSRUN) with 1.25 Dhrystone MIPS per MHz
  - Arm Core based on the Armv7 Architecture and Thumb®-2 ISA
  - Integrated Digital Signal Processor (DSP)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single Precision Floating Point Unit (FPU)
- Clock interfaces
  - 4 - 40 MHz fast external oscillator (SOSC)
  - 48 MHz Fast Internal RC oscillator (FIRC)
  - 8 MHz Slow Internal RC oscillator (SIRC)
  - 128 kHz Low Power Oscillator (LPO)
  - Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)
  - Up to 50 MHz DC external square wave input clock
  - Real Time Counter (RTC)
- Power management
  - Low-power Arm Cortex-M4F core with excellent energy efficiency
  - Power Management Controller (PMC) with multiple power modes: HSRUN, Run, Stop, VLPR, and VLPS
  - Supports peripheral specific clock gating. Only specific peripherals remain working in low power modes.
- Memory and memory interfaces
  - Up to 2 MB program flash memory with ECC
  - 64 KB FlexNVM for data flash memory with ECC and EEPROM emulation
  - Up to 256 KB SRAM with ECC
  - Up to 4 KB of FlexRAM for use as SRAM or EEPROM emulation
  - Up to 4 KB Code cache to minimize performance impact of memory access latencies
  - QuadSPI with HyperBus™ support
- Mixed-signal analog
  - Up to two 12-bit Analog-to-Digital Converter (ADC) with up to 32 channel analog inputs per module
  - One Analog Comparator (CMP) with internal 8-bit Digital to Analog Converter (DAC)
- Debug functionality
  - Serial Wire JTAG Debug Port (SWJ-DP) combines
  - Debug Watchpoint and Trace (DWT)
  - Instrumentation Trace Macrocell (ITM)
  - Test Port Interface Unit (TPIU)
  - Flash Patch and Breakpoint (FPB) Unit
- Human-machine interface (HMI)
  - Up to 156 GPIO pins with interrupt functionality
  - Non-Maskable Interrupt (NMI)
- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for flexible and high performance serial interfaces
- Reliability, safety and security
  - HW Security Engine (CSEc)
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - Cyclic Redundancy Check (CRC) module
  - 128-bit Unique Identification (ID) number
  - System Memory Protection Unit (System MPU)

- Timing and control
  - Up eight independent 16-bit FlexTimers (FTM) module, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- I/O and package
  - 64-pin LQFP, 100-pin LQFP, 144-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

Table of Contents

1 Block diagram

The figure below shows a superset high level architecture block diagram of the device. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.

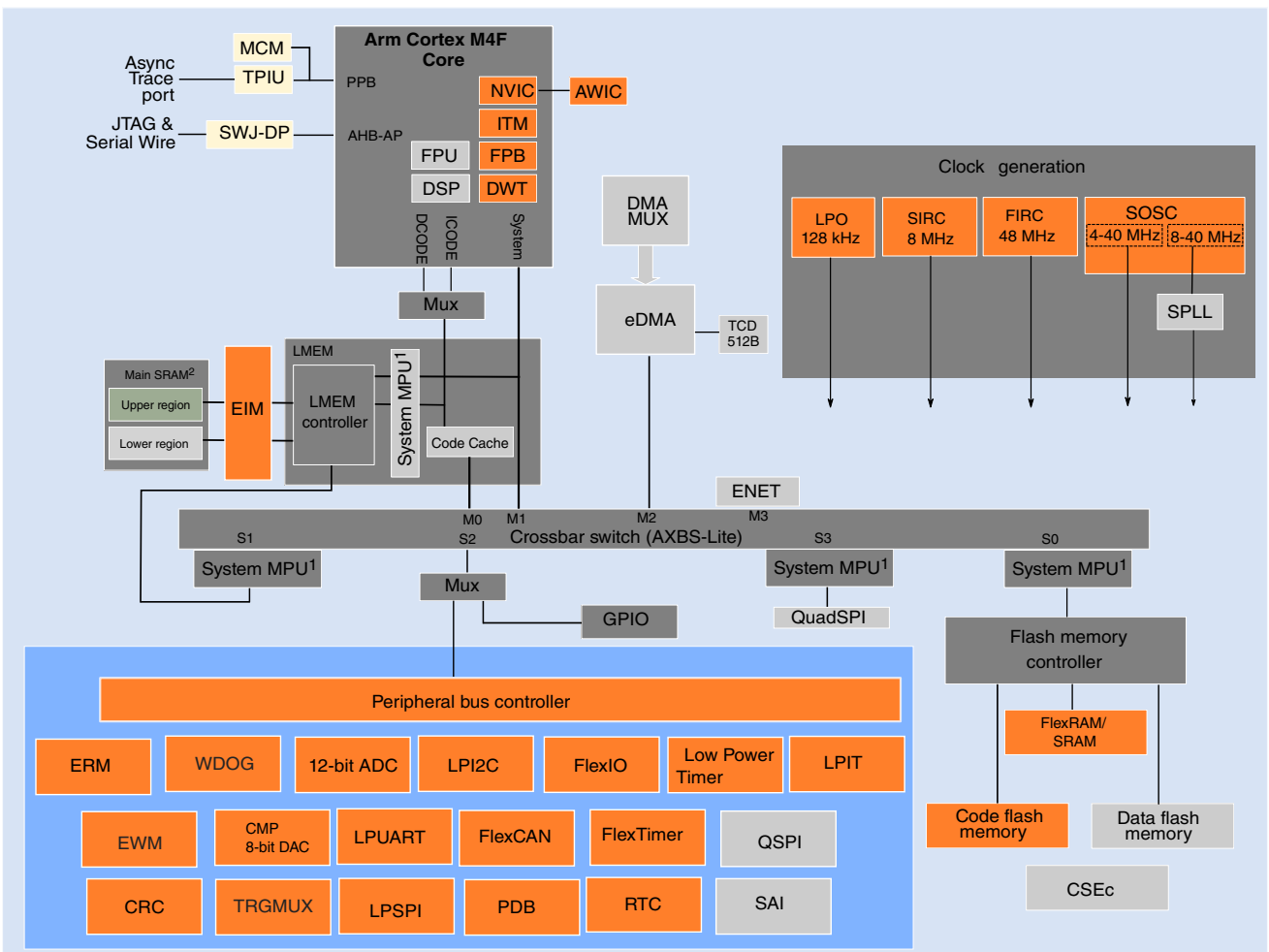


Figure 1. High-level architecture diagram for the MWCT101xS family

2 Feature comparison

The following figure summarizes the memory and package options for the MWCT101xS series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

Feature comparison

	Parameter	MWCT101xS		
		MWCT1014S	MWCT1015S	MWCT1016S
	Core	Arm® Cortex™-M4F		
	Frequency	up to 112 MHz (HSRUN)		
System	IEEE-754 FPU	●		
System	HW security module (CSEc)[1]	●		
System	CRC module	1x		
System	ISO 26262	capable up to ASIL-B		
System	Peripheral speed	up to 112 MHz (HSRUN)		
System	Crossbar	●		
System	DMA	●		
System	EWM	●		
System	Memory protection unit	●		
System	FIRC CMU	○		
System	Watchdog	1x		
System	Low power modes	●		
System	HSRUN mode	●		
System	Number of I/Os	up to 89	up to 128	up to 156
System	Single supply voltage	2.7 - 5.5 V		
System	Operating temperature (T_a) Temperature ambient	-40 to +105°C		
Memory	Flash	512 KB	1 MB	2 MB[2]
Memory	Error correction code (ECC)	●		
Memory	System RAM (including FlexRAM)	64 KB	128 KB	256 KB
Memory	FlexRAM (also available as system RAM)	4 KB		
Memory	Cache	4 KB		
Memory	EEPROM emulated by FlexRAM	4 KB (up to 64 KB D-Flash)		See footnote 3
Memory	External memory interface	○		QuadSPI incl. HyperBus™
Timer	Low power interrupt timer	1x		
Timer	FlexTimer (16-bit counter) 8 channels	4x (32)	6x (48)	8x (64)
Timer	Low power timer (LPTMR)	1x		
Timer	Real time counter (RTC)	1x		
Timer	Programmable delay block (PDB)	2x		
Analog	Trigger mux (TRGMUX)	1x (64)	1x (73)	1x (81)
Analog	12-bit SAR ADC (1 MSPS each)	2x (16)	2x (24)	2x (32)
Analog	Comparator with 8-bit DAC	1x		
Communication	100 Mbit IEEE-1588 ethernet MAC	○		1x
Communication	Serial audio interface (AC97, TDM, I2S)	○		2x
Communication	Low power UART/LIN (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A and SAE J2602)	3x		
Communication	Low power SPI	3x		
Communication	Low power I2C	1x		2x
Communication	FlexCAN (CAN-FD ISO/CD 11898-1)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
Communication	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		
IDEs	Debug & trace	SWD, JTAG (ITM, SWV, SWO)		SWD, JTAG (ITM, SWV, SWO), ETM
IDEs	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach, iSystems		
Other	Packages	LQFP-64 LQFP-100	LQFP-100	LQFP-144

LEGEND:
- ○ Not implemented
- ● Available on the device

1 No FTFC commands, including CSE commands (CSEc parts) are available when chip is in VLPR or HSRUN mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2M Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.

Figure 2. MWCT101xS product series comparison

3 Ordering parts

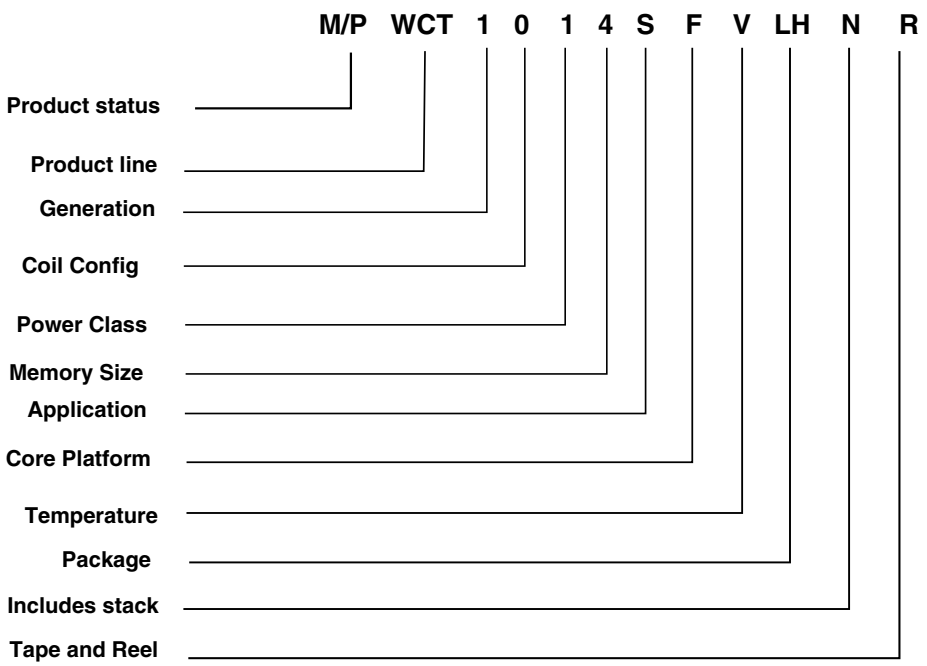
3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search.

NOTE

Not all part number combinations exist

3.2 Ordering information



Product status
P: Pre Qualification
M: Fully Qualified

Product line
WCT: Wireless Charging Technology

Generation
1: 1st product Gen
2: 2nd product Gen

Coil config
0 = Standard
1 = Premium

Power Class
0 = 5 W
1 = 15 W
2 = 60 W
3 =200 W

Memory size (Flash)

	4	5	6
M0+		128 K	256 K
M4F	512 K	1 M	2 M

Application
Blank =Customer
A = Auto/Industr
S = A + AUTOSAR

Core platform
Z: Arm Cortex M0+
F: Arm Cortex M4F

Temperature
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

Package

Pins	LQFP	LQFP -EP	QFN	BGA
32	LC	-	FM	-
48	LF	KF	FT	-
64	LH	KH	-	-
100	LL	-	-	MH
144	LQ	-	-	-
176	LU	-	-	-

Includes stack
Blank = No stack
N = NFC

Tape and Reel
T: Trays and Tubes
R: Tape and Reel

Figure 3. Ordering information

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not gaurantee desired operation.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{DD}[2]	2.7 V - 5. 5V input supply voltage	—	-0.3	5.8 [3]	V
V_{REFH}	3.3 V / 5.0 V ADC high reference voltage	—	-0.3	5.8 [3]	V
$I_{INJPAD\_DC\_ABS}$[4]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	—	-3	+3	mA
V_{IN_DC}	Continuous DC Voltage on any I/O pin with respect to V_{SS}	—	-0.8	5.8[5]	V
$I_{INJSUM\_DC\_ABS}$	Sum of absolute value of injected currents on all the pins (Continuous DC limit)	—	—	30	mA
T_{ramp}[6]	Supply ramp rate	—	0.5 V/min	500 V/ms	—
T_A[7]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	-55	165	°C
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pin beyond $V_{IN\_DC\ limit}$	—	—	6.8 [8]	V

1. All voltages are referred to V_{SS} unless otherwise specified.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. 60 s lifetime – No restrictions i.e. The part can switch.

   10 hours lifetime – Device in reset i.e. The part cannot switch.
4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

- Assumes maximum θJA for 2s2p board. See Thermal characteristics

8. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Full functionality/specifications cannot be guaranteed when voltage drops below 2.7 V.

Table 2. Voltage and current operating requirements [1]

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. MWCT1016S will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MWCT1016S is guaranteed to operate from 2.97 V. All other MWCT101xS family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decap to be used to filter noise on V_{DDA}. See application note AN5032 for reference supply design for SAR ADC.
5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP and 100 LQFP packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	85[1]	°C
$T_{J\ C\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	105[1]	°C
$T_{A\ V\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	105[1]	°C
$T_{J\ V\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	125[1]	°C
$T_{A\ M\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	125[2]	°C
$T_{J\ M\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	135[2]	°C

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

4.4 Power and ground pins

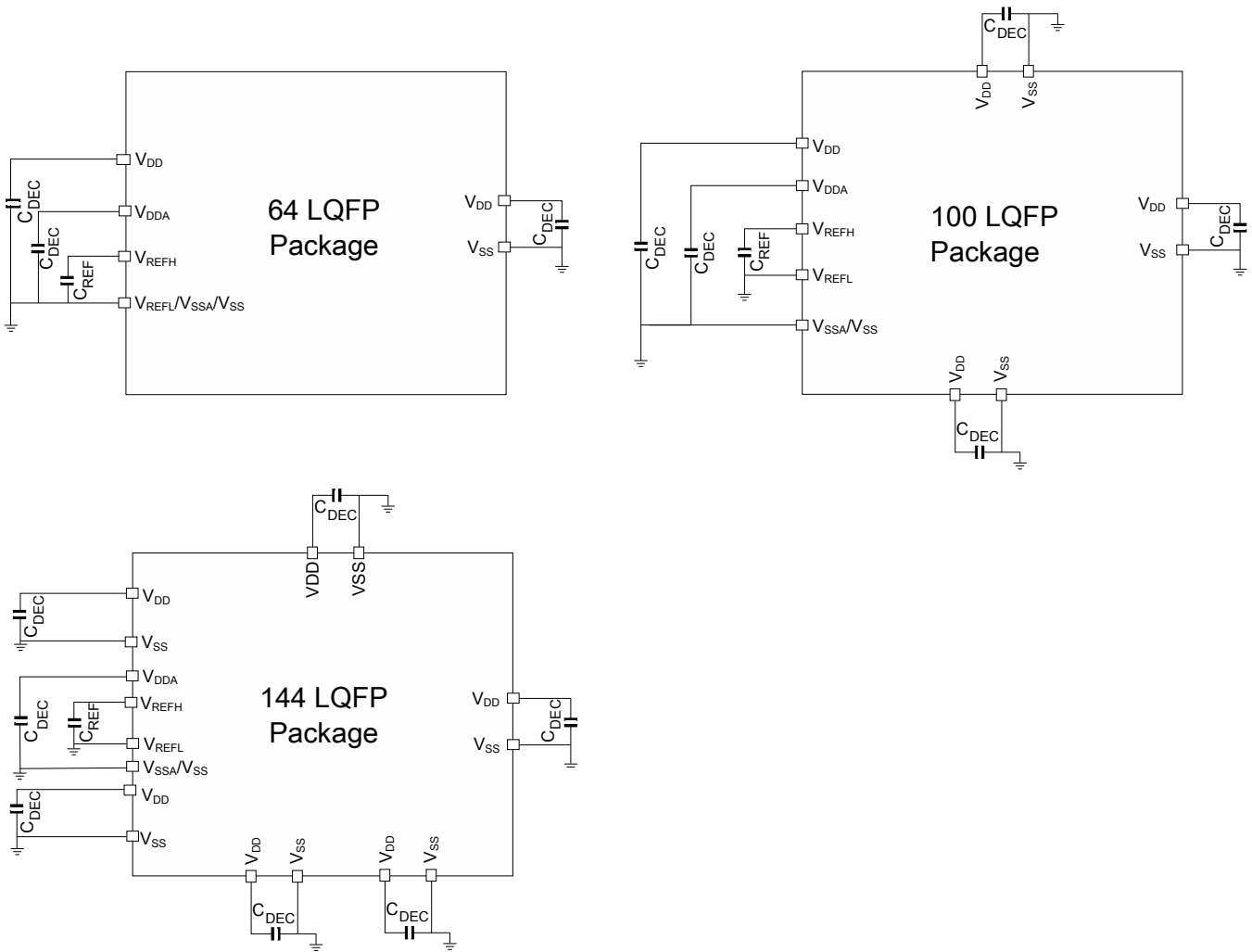


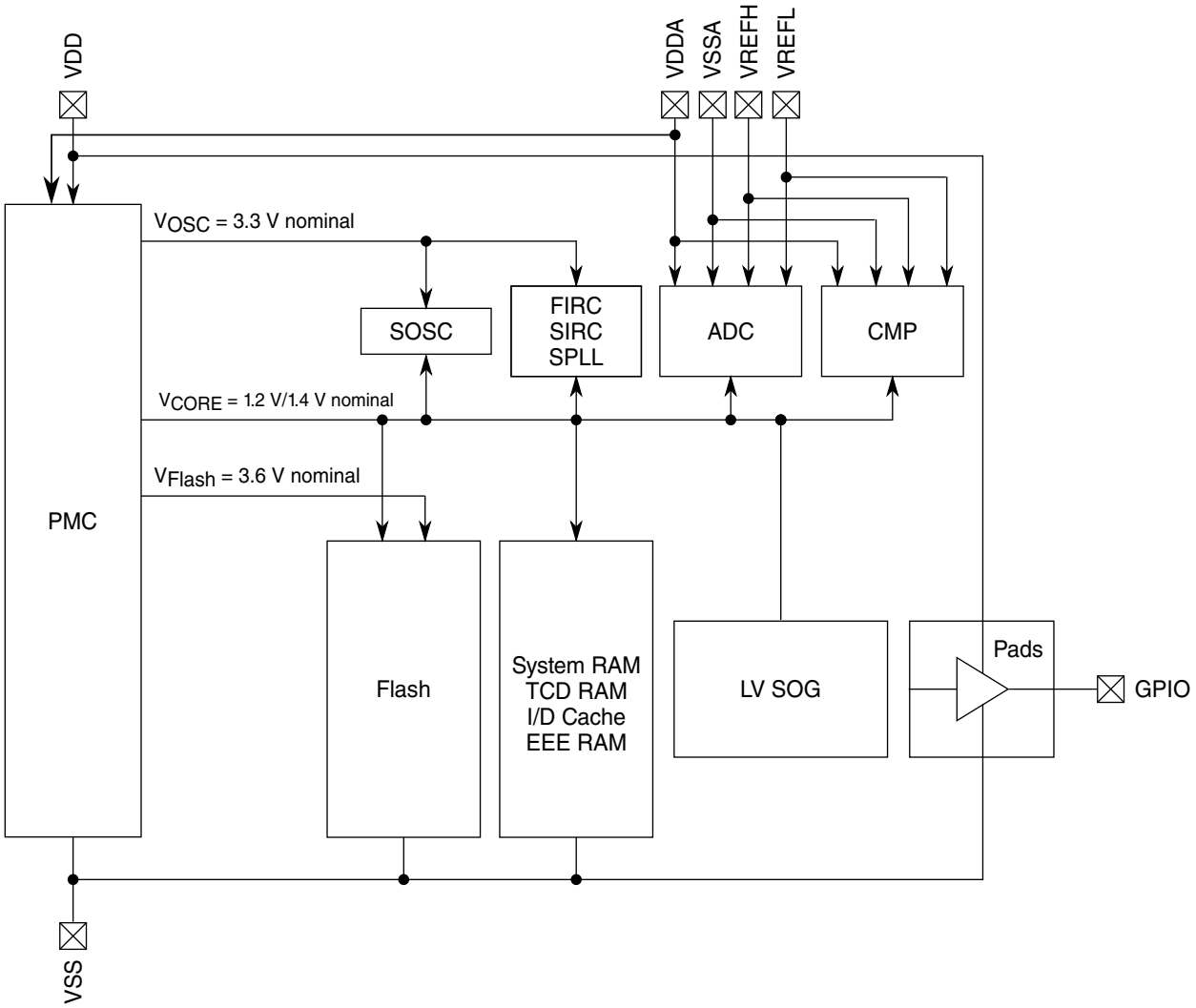
Figure 4. Pinout decoupling

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. [3]	Typ.	Max.	Unit
C_{REF} [4, 5]	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} [5, 6, 7]	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.

- No trace exceeding 1 mm from the protection to the trace or to the ground.
- The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
- The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.



*Note: VSSA and VSS are shorted at package level

Figure 5. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	

Table continues on the next page...

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- HSRUN Mode:
  - Clock source: SPLL
  - SYS_CLK/CORE_CLK = 112 MHz
  - BUS_CLK = 56 MHz
  - FLASH_CLK = 28 MHz
- VLPR Mode:
  - Clock source: SIRC
  - SYS_CLK/CORE_CLK = 4 MHz
  - BUS_CLK = 4 MHz
  - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled.

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	µs

Table continues on the next page...

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.75	6.25	6.5	µs
	VLPS → VLPR	26.5	27.25	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	HSRUN → Compute operation	0.3	0.31	0.35	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.35	0.38	0.4	µs
	RUN → VLPR	4.4	4.7	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations.

Table 7. Power consumption (Typicals unless stated otherwise) 1

	Ambient Temperature (°C)		VLPS (µA)[2, 3]		VLPR (mA)		STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [4]		Idd/MHz (µA/MHz)[5]
			Peripherals disabled [6]	Peripherals enabled	Peripherals disabled	Peripherals enabled			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
MWCT1014S	25	Typ	29.8	39.1	1.48	1.50	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378
	85	Typ	150	159	1.72	1.85	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	8.3	9.2	21.9	28.5	27.8	34.4	32.9	41.5	45.5	57.5	411
	105	Typ	256	273	1.80	2.10	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	10.3	10.6	22.7	30	28.3	36.5	33.4	43.3	47.9	61.3	418
	125	Max	1960	1998	3.18	3.25	12.2	13	25.3	32.7	35	39.8	37.1	46.5	NA	NA	464
MWCT1015S	25	Typ	40	55	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	95	110	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	70	80	NA	NA	TBD
MWCT1016S[7, 8]	25	Typ	40	60	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	120	125	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	100	110	NA	NA	TBD

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration.
2. This is an average based on the use case described in the Comparator section, whereby the analog sampling is taking place periodically, with a mechanism to only enable the DAC as required. The numbers quoted assumes that only a single ANLCMP is active and the others are disabled
3. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
4. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
5. Values mentioned are measured at 25 ℃ at RUN@80 MHz with peripherals disabled.
6. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
7. Above MWCT1016S data is preliminary targets only
8. The MWCT1016S data points assume that ENET/QuadSPI/SAI etc. are active. If the same configuration is selected as per the MWCT1014S, then the two devices will have very similar IDD.

4.7.1 Modes configuration

Attached *MWCT101xS_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the above table Table 7. For full functionality refer to table: Module operation in available low power modes of the *Reference Manual*.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

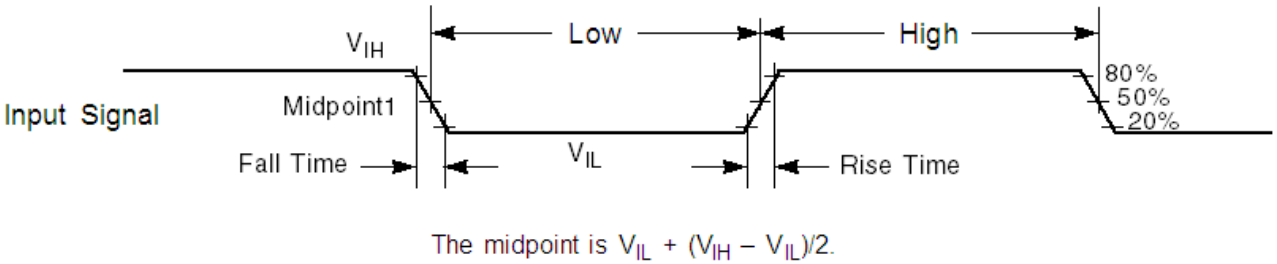


Figure 6. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 8. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	100	ns	4
WFRST	$\overline{\text{RESET}}$ input not filtered pulse	100	—	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter.

5.3 DC electrical specifications at 3.3 V Range

Table 9. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_Standard	I/O current source capability measured when pad = (V_{DDE} – 0.8 V)	3.5	—	—	mA	

Table continues on the next page...

Table 9. DC electrical specifications at 3.3 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Iol_Standard	I/O current sink capability measured when pad = 0.8 V	3	—	—	mA	
Ioh_Strong	I/O current source capability measured when pad = (V_{DDE} – 0.8 V)	14	—	—	mA	4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	12	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins [7]		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	8
R_{PD}	Internal pulldown resistors	20		60	kΩ	9

1. MWCT1016S will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MWCT1016S is guaranteed to operate from 2.97 V. All other MWCT101xS family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *MWCT101xS_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. When using ENET and SAI on MWCT1016S, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = V_{SS}
9. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 10. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_Standard	I/O current source capability measured when pad = (V_{DDE} - 0.8 V)	5	—	—	mA	
Iol_Standard	I/O current sink capability measured when pad = 0.8 V	5	—	—	mA	

Table continues on the next page...

Table 10. DC electrical specifications at 5.0 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Ioh_Strong	I/O current source capability measured when pad = V_{DDE} - 0.8 V	20	—	—	mA	3, 4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	20	—	—	mA	4, 5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	7
R_{PD}	Internal pulldown resistors	20		50	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. The strong pad I/O pin is capable of switching a 50 pF load at up to 40 MHz.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *MWCT101xS_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. Measured at input V = V_{SS}
8. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 11. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
Standard	NA	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
Strong	0	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
	1	2.0	5.8	1.8	6.1	25
		2.8	8.0	2.6	8.3	50
		7.0	20.7	6.0	22.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 12. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
Standard	NA	3.2	9.4	3.6	10.7	25
		5.4	15.7	5.1	17.4	50
		18.5	52.6	17.6	59.7	200
Strong	0	4.0	9.4	3.6	10.7	25
		5.8	15.7	5.1	17.4	50
		18.1	52.6	17.6	59.7	200
	1	1.6	4.6	1.5	5.0	25
		2.2	5.7	2.2	5.8	50
		5.6	14.6	5.0	15.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 13. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 14. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (MWCT101xS series) [3]				

Table continues on the next page...

Table 14. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[4]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

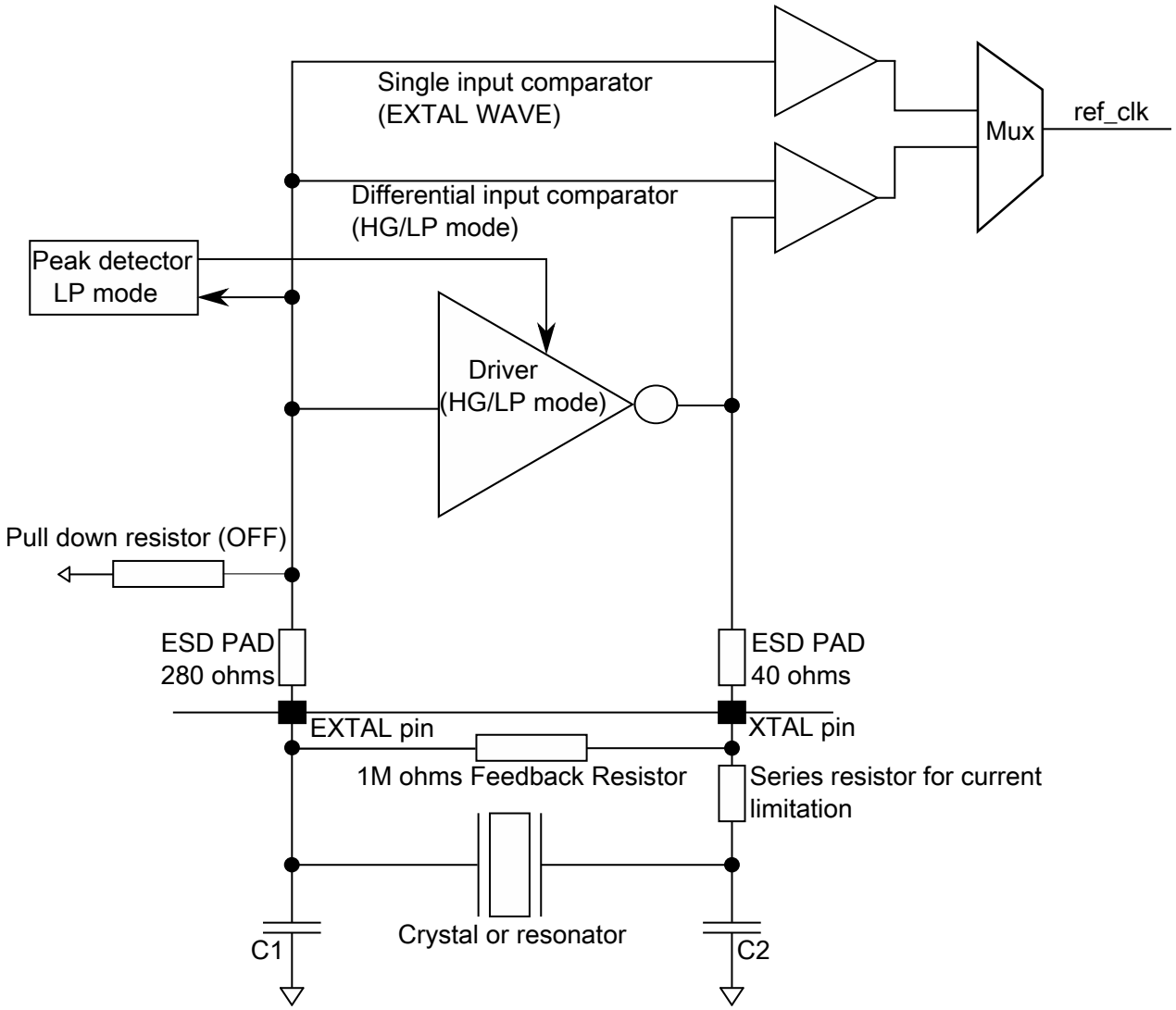


Figure 7. Oscillator connections scheme

Table 15. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	4-8 MHz	2.2	—	13.7	mA/V	
	8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 * V_{DD}	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 15. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 16. External System Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_hi}	Oscillator crystal or resonator frequency	4	—	40	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal Start-up Time					
	8 MHz low-gain mode (HGO=0)	—	1.5	—	ms	1
	8 MHz high-gain mode (HGO=1)	—	2.5	—		
	40 MHz low-gain mode (HGO=0)	—	2	—		
	40 MHz high-gain mode (HGO=1)	—	2	—		

1. Proper PC board layout procedures must be followed to achieve specifications.