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Freescale Semiconductor
Technical Data

Document Number: MWIC930
Rev. 5, 5/2006

Replaced by MWIC930NR1(GNR1). There are no form, fit or function changes with this part replacement. N suffix added to part number to indicate transition to lead-free terminations.

RF LDMOS Wideband Integrated Power Amplifiers

MWIC930R1
MWIC930GR1

The MWIC930 wideband integrated circuit is designed for CDMA and GSM/GSM EDGE applications. It uses Freescale's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On-Chip integral matching circuitry makes it usable from 790 to 1000 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, N-CDMA and W-CDMA.

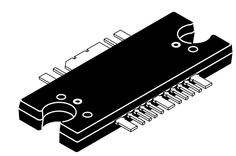
746-960 MHz, 30 W, 26-28 V SINGLE N-CDMA, GSM/GSM EDGE RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

Final Application

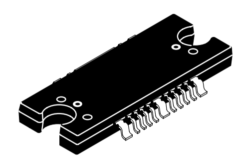
- Typical Performance @ P1dB: V_{DD} = 26 Volts, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, P_{out} = 30 Watts P1dB, Full Frequency Band (921-960 MHz)
  Power Gain — 30 dB
  Power Added Efficiency — 45%

Driver Application

- Typical Single-Carrier N-CDMA Performance: V_{DD} = 27 Volts, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, P_{out} = 5 Watts Avg., Full Frequency Band (865-894 MHz), IS-95 (Pilot, Sync, Paging, Traffic Codes 8 Through 13), Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
  Power Gain — 31 dB
  Power Added Efficiency — 21%
  ACPR @ 750 kHz Offset — -52 dBc in 30 kHz Bandwidth
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 921 MHz, 30 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >4 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application [1]
- Integrated ESD Protection
- 200°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1329-09
TO-272 WB-16
PLASTIC
MWIC930R1



CASE 1329A-03
TO-272 WB-16 GULL
PLASTIC
MWIC930GR1

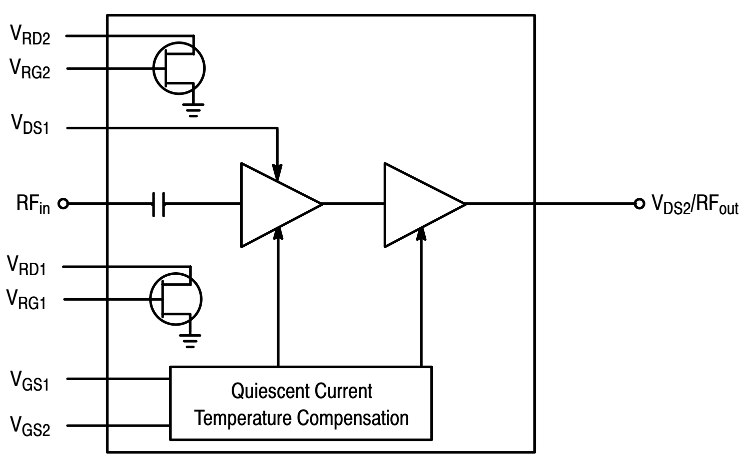
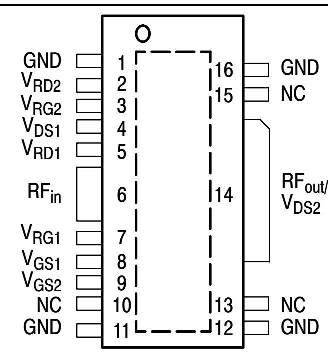


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

1. Refer to AN1987/D, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
GSM Application (P_{out} = 30 W CW)	Stage 1, 26 Vdc, I_{DQ} = 90 mA		5.9	
	Stage 2, 26 Vdc, I_{DQ} = 240 mA		1.4	
GSM EDGE Application (P_{out} = 15 W CW)	Stage 1, 27 Vdc, I_{DQ} = 90 mA		6.5	
	Stage 2, 27 Vdc, I_{DQ} = 240 mA		1.7	
CDMA Application (P_{out} = 5 W CW)	Stage 1, 27 Vdc, I_{DQ} = 90 mA		6.5	
	Stage 2, 27 Vdc, I_{DQ} = 240 mA		1.8	

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C2 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, P_{out} = 5 W Avg. N-CDMA, f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Bandwidth @ ±750 MHz Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF					
Power Gain	G_{ps}	28	31	—	dB
Power Added Efficiency	PAE	18	21	—	%
Input Return Loss (f = 880 MHz)	IRL	—	-12	-9	dB
Adjacent Channel Power Ratio	ACPR	—	-52	-48	dBc
Typical Performances (In Freescale Test Fixture) V_{DD} = 26 Vdc, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, 840 MHz<Frequency<920 MHz					
Quiescent Current Accuracy over Temperature (2)		—		—	%
Stage 1 with 33.2 kΩ Gate Feed Resistors (-30 to 115°C)	ΔI_{1QT}		±2.5		
Stage 2 with 47.5 kΩ Gate Feed Resistors (-30 to 115°C)	ΔI_{2QT}		±2.5		
Gain Flatness in 80 MHz Bandwidth @ P_{out} = 5 W CW	G_F	—	0.3	—	dB
Deviation from Linear Phase in 80 MHz Bandwidth @ P_{out} = 5 W CW	Φ	—	0.6	—	°
Delay @ P_{out} = 5 W CW Including Output Matching	Delay	—	3	—	ns
Part-to-Part Phase Variation @ P_{out} = 5 W CW	$\Delta\Phi$	—	±15	—	°

1. Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
2. Refer to AN1977/D, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977.

(continued)

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Table 5. Electrical Characteristics (T_C = 25°C, unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical GSM/GSM EDGE Performances (In Freescale GSM/GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, 921 MHz<Frequency<960 MHz					
Output Power, 1dB Compression Point	P1dB	—	30	—	W
Power Gain @ P_{out} = 30 W CW	G_{ps}	—	30	—	dB
Power Added Efficiency @ P_{out} = 30 W CW	PAE	—	45	—	%
Input Return Loss @ P_{out} = 30 W CW	IRL	—	-12	—	dB
Intermodulation Distortion (15 W, 2-Tone, 100 kHz Tone Spacing)	IMD	—	-30	—	dBc
Intermodulation Distortion (1 W, 2-Tone, 100 kHz Tone Spacing)	IMD backoff	—	-45	—	dBc
Gain Flatness in a 40 MHz Bandwidth @ P_{out} = 30 W CW	G_F	—	0.3	—	dB
Deviation from Linear Phase in a 40 MHz Bandwidth @ P_{out} = 30 W CW	Φ	—	0.6	—	°

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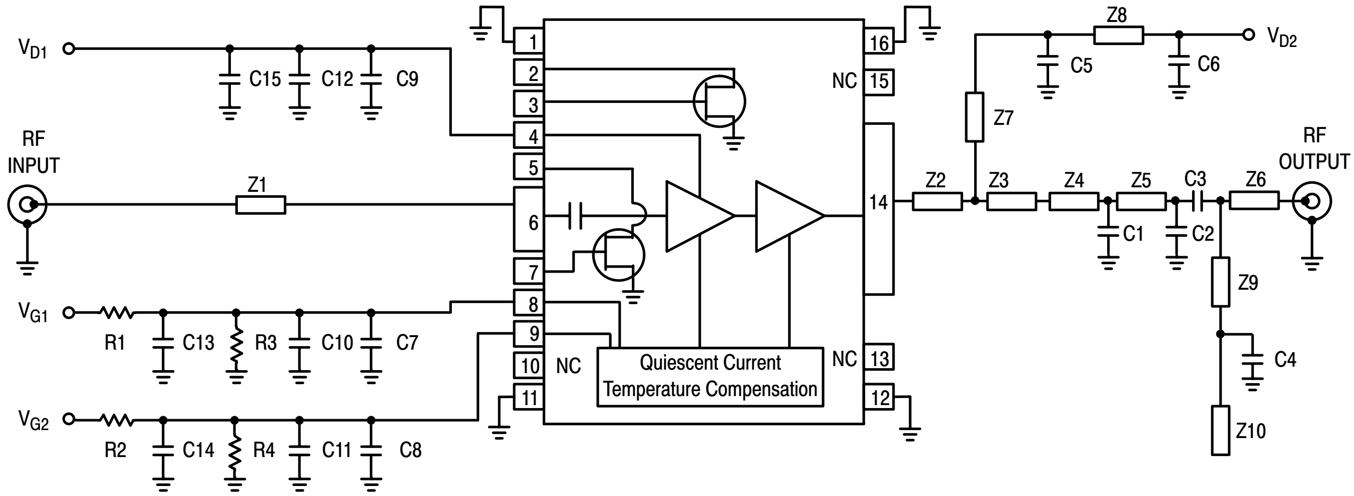

Z1	0.0438″ x 0.970″ 50 Ω Microstrip (not including lead pad)	Z6	0.0438″ x 0.2009″ Microstrip
Z2	0.234″ x 0.1183″ Microstrip (including lead pad)	Z7	0.5274″ x 0.0504″ Microstrip
Z3	0.1575″ x 0.9379″ Microstrip	Z8	0.0504″ x 0.250″ Microstrip
Z4	0.08425″ x 0.0729″ Microstrip	Z9	0.880″ x 0.0254″ Microstrip
Z5	0.08425″ x 0.5111″ Microstrip	Z10	0.0254″ x 0.250″ Microstrip
		PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 3. MWIC930R1(GR1) Test Fixture Schematic

Table 6. MWIC930R1(GR1) Test Fixture Component Designations and Values

Part	Description	Part Number	Manufacturer
*C1	15 pF High Q Capacitor	ATC600S150JW	ATC
*C2	6.8 pF High Q Capacitor - GSM Fixture 8.2 pF High Q Capacitor - CDMA Fixture	ATC600S6R8CW ATC600S8R2CW	ATC
*C3	5.6 pF High Q Capacitor	ATC600S5R6CW	ATC
*C4, C5, C7, C8, C9	47 pF High Q Capacitors	ATC600S470JW	ATC
C6, C13, C14, C15	1 μF Chip Capacitors	GRM42-2X7R105K050AL	Murata
C10, C11, C12	10 nF Chip Capacitors	C0603C103J5R	Kemet
R1, R2	1 kΩ, 1/8 W Chip Resistors	RM73B2AT102J	KOA Speer
R3, R4	1 MΩ, 1/4 W Chip Resistors	RM73B2BT105J	KOA Speer

* For output matching and bypass purposes, it is strongly recommended to use these exact capacitors.

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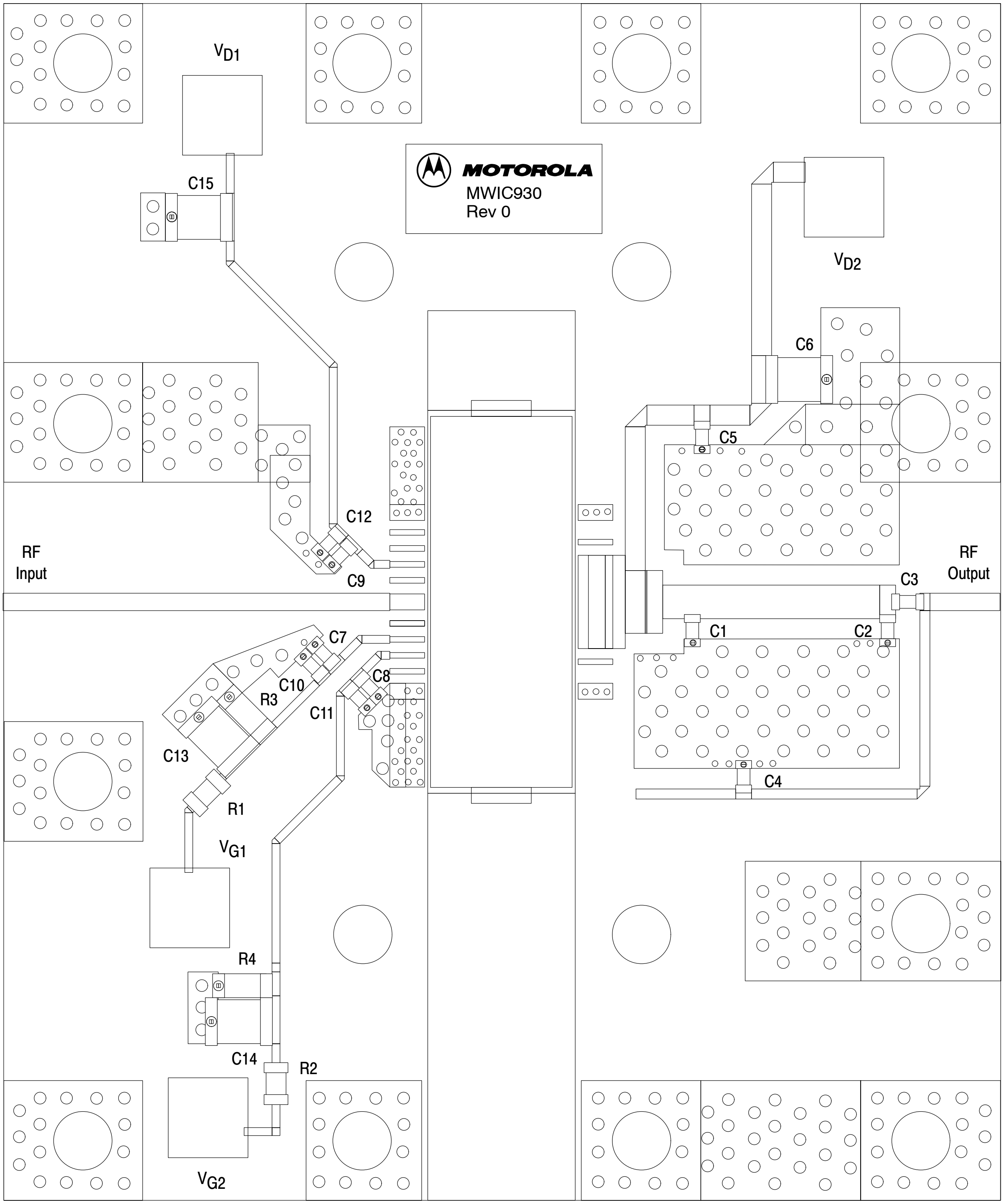


Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. MWIC930R1(GR1) Test Circuit Component Layout

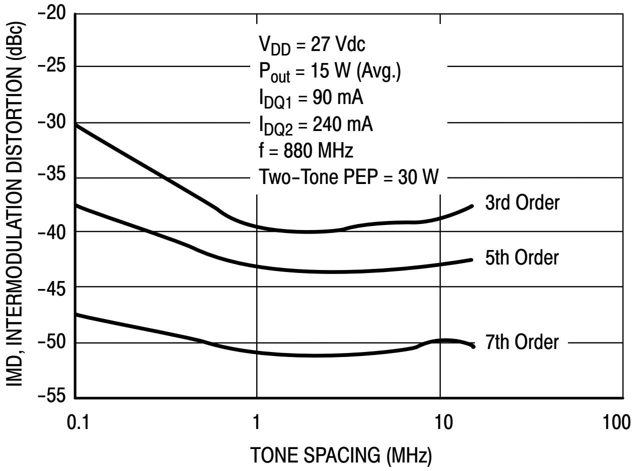


Figure 5. Intermodulation Distortion Products versus Output Power

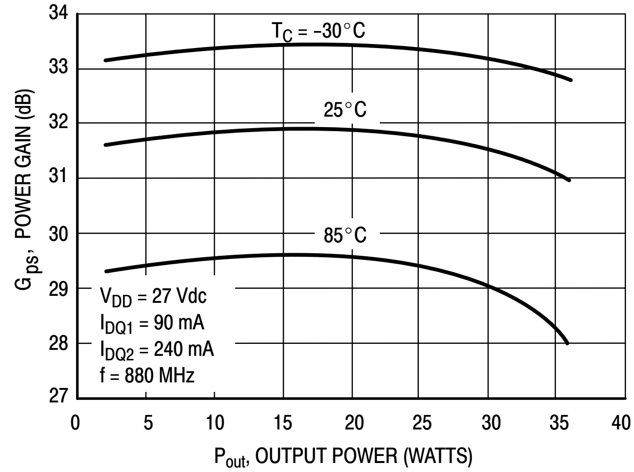


Figure 6. Power Gain versus Output Power

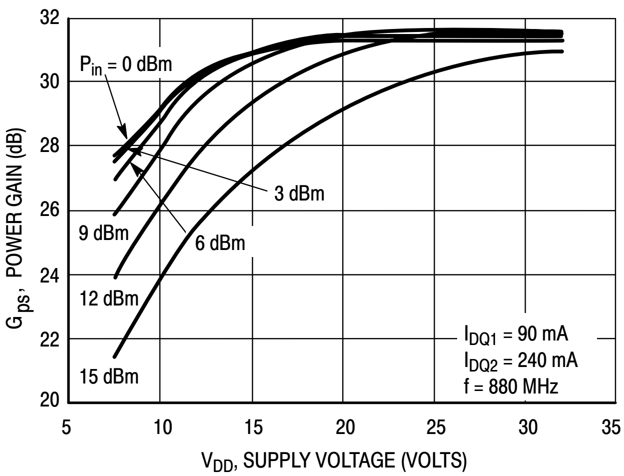


Figure 7. Power Gain versus Supply Voltage

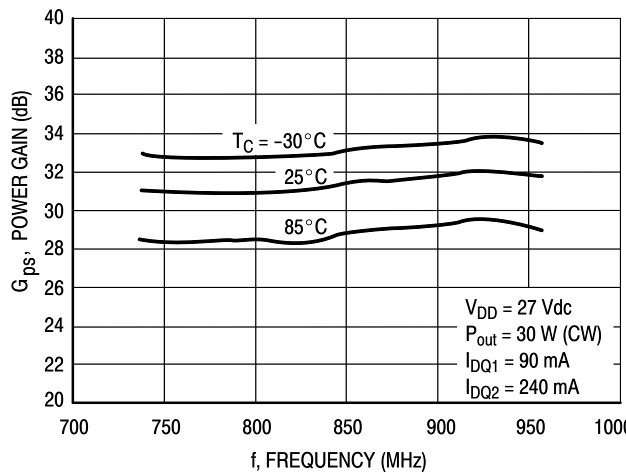


Figure 8. Power Gain versus Frequency

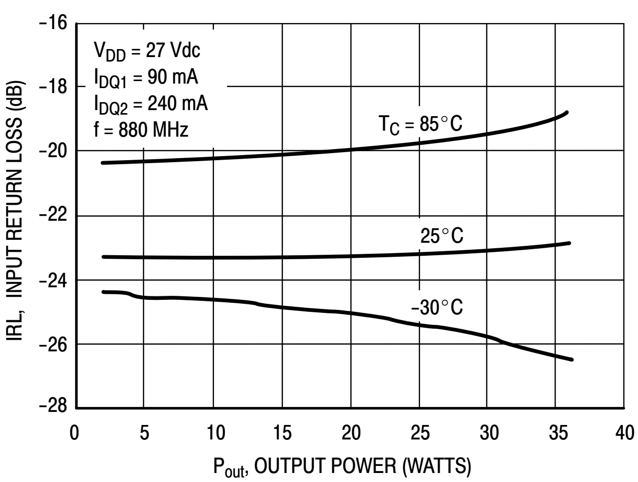


Figure 9. Input Return Loss versus Output Power

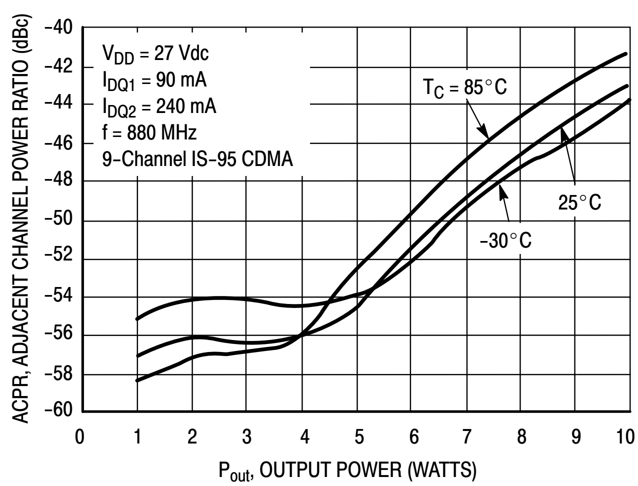


Figure 10. Adjacent Channel Power Ratio versus Output Power

TYPICAL CHARACTERISTICS

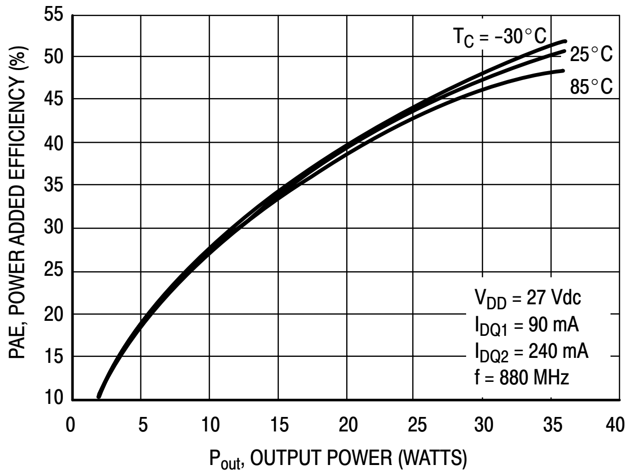


Figure 11. Power Added Efficiency versus Output Power

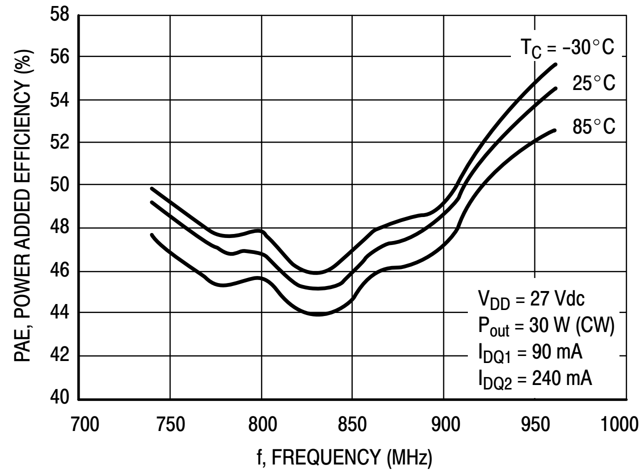
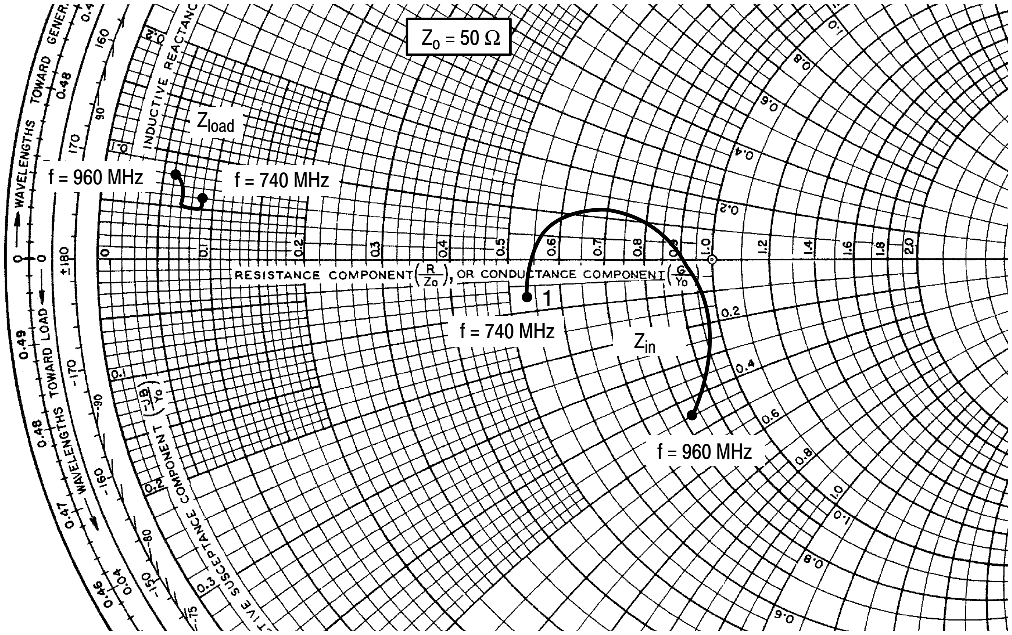


Figure 12. Power Added Efficiency versus Frequency

ARCHIVE INFORMATION



V_{DD} = 27 Vdc, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, P_{out} = 5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
740	26.61 - j3.68	4.28 + j2.99
760	26.88 - j0.53	4.37 + j2.91
780	28.22 + j2.21	4.39 + j2.79
800	30.57 + j4.31	4.34 + j2.64
820	33.79 + j5.53	4.21 + j2.54
840	37.83 + j5.30	4.06 + j2.52
860	41.92 + j3.42	3.90 + j2.58
880	45.58 - j0.40	3.73 + j2.70
900	47.77 - j5.84	3.59 + j2.93
920	47.83 - j12.15	3.43 + j3.17
940	45.55 - j18.05	3.28 + j3.44
960	41.58 - j22.64	3.13 + j3.75

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

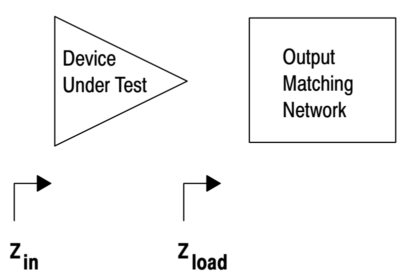
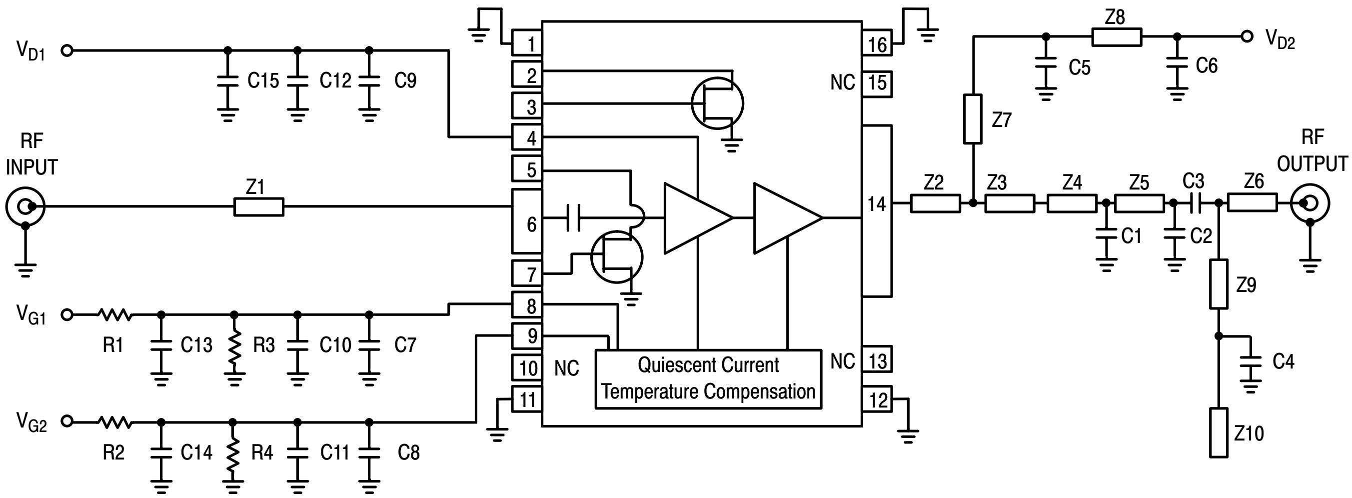


Figure 13. Series Equivalent Input and Load Impedance



Z1	0.0438″ x 0.970″ 50 Ω Microstrip (not including lead pad)	Z6	0.0438″ x 0.2009″ Microstrip
Z2	0.234″ x 0.1183″ Microstrip (including lead pad)	Z7	0.5274″ x 0.0504″ Microstrip
Z3	0.1575″ x 0.9379″ Microstrip	Z8	0.0504″ x 0.250″ Microstrip
Z4	0.08425″ x 0.0729″ Microstrip	Z9	0.880″ x 0.0254″ Microstrip
Z5	0.08425″ x 0.5111″ Microstrip	Z10	0.0254″ x 0.250″ Microstrip
		PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 14. MWIC930R1(GR1) Test Fixture Schematic — Alternate Characterization for Driver/Pre-Driver Performance

Table 7. MWIC930R1(GR1) Test Fixture Component Designations and Values — Alternate Characterization for Driver/Pre-Driver Performance

Part	Description	Part Number	Manufacturer
*C1	12 pF High Q Capacitor	ATC600S120JW	ATC
*C2	8.2 pF High Q Capacitor - CDMA Fixture	ATC600S8R2CW	ATC
*C3	5.6 pF High Q Capacitor	ATC600S5R6CW	ATC
*C4, C5, C7, C8, C9	47 pF High Q Capacitors	ATC600S470JW	ATC
C6, C13, C14, C15	1 μF Chip Capacitors	GRM42-2X7R105K050AL	Murata
C10, C11, C12	10 nF Chip Capacitors	C0603C103J5R	Kemet
R1, R2	1 kΩ, 1/8 W Chip Resistors	RM73B2AT102J	KOA Speer
R3, R4	1 MΩ, 1/4 W Chip Resistors	RM73B2BT105J	KOA Speer

* For output matching and bypass purposes, it is strongly recommended to use these exact capacitors.

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TYPICAL CHARACTERISTICS
DRIVER/PRE-DRIVER PERFORMANCE

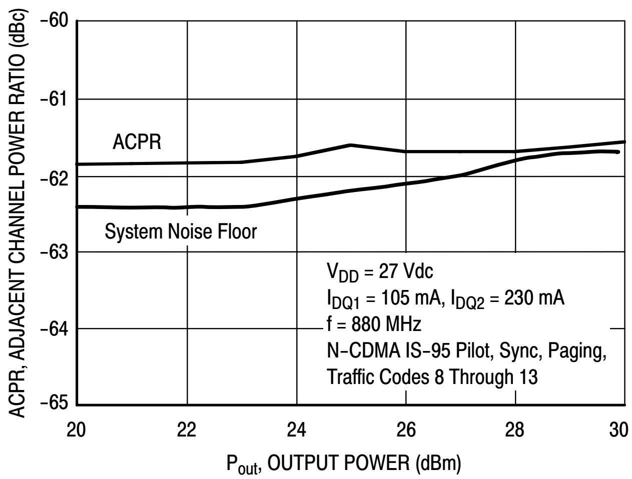

Figure 15. Single-Carrier N-CDMA ACPR versus Output Power

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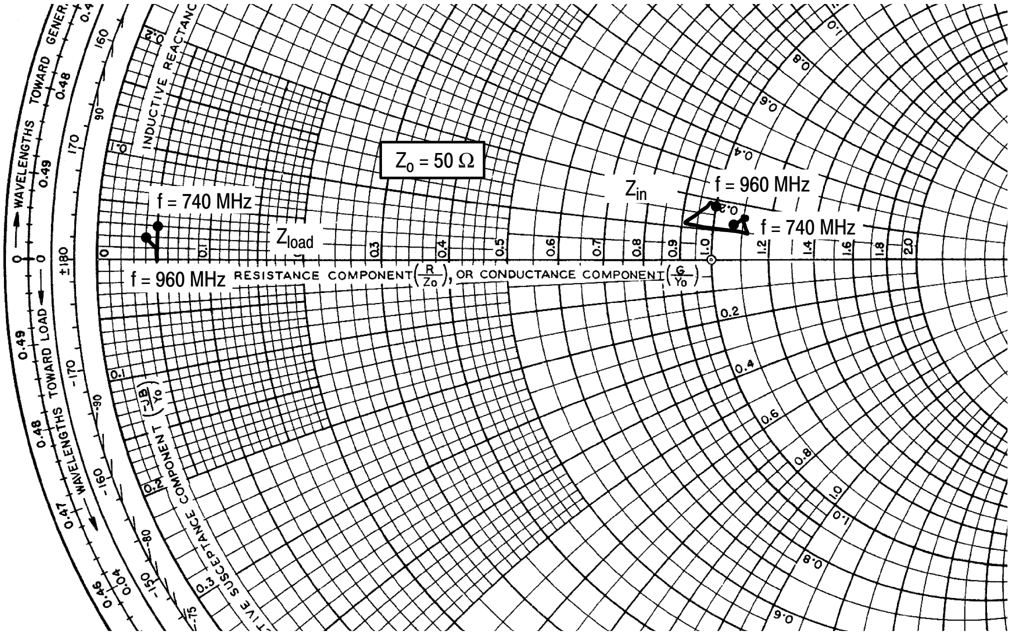


V_{DD} = 27 Vdc, I_{DQ1} = 105 mA, I_{DQ2} = 230 mA, P_{out} = 5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
740	53.944 + j6.745	2.535 + j1.662
760	54.452 + j7.112	2.602 + j1.080
780	55.006 + j7.440	2.688 + j0.548
800	55.549 + j7.656	2.659 + j0.064
820	55.604 + j7.855	2.615 + j0.329
840	55.190 + j7.835	2.568 + j0.450
860	55.110 + j7.410	2.494 + j0.620
880	55.752 + j4.763	2.444 + j0.650
900	45.606 + j5.832	2.440 + j0.689
920	49.206 + j9.284	2.134 + j0.930
940	49.939 + j9.030	2.155 + j0.835
960	50.088 + j8.752	2.095 + j1.235

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

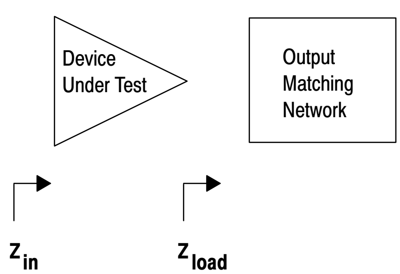
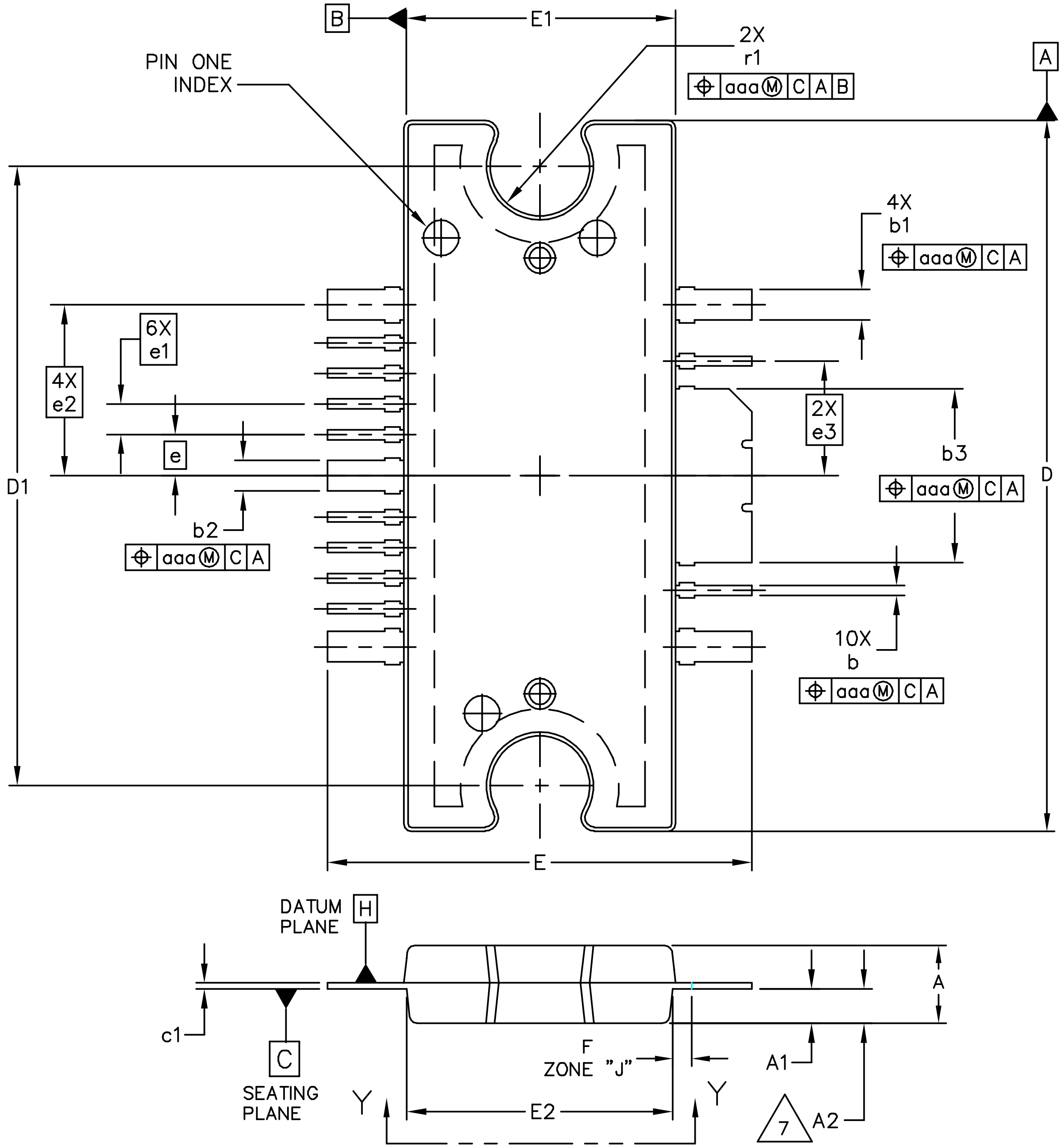


Figure 16. Series Equivalent Input and Load Impedance — Alternate Characterization for Driver/Pre-Driver Performance

NOTES

NOTES

PACKAGE DIMENSIONS



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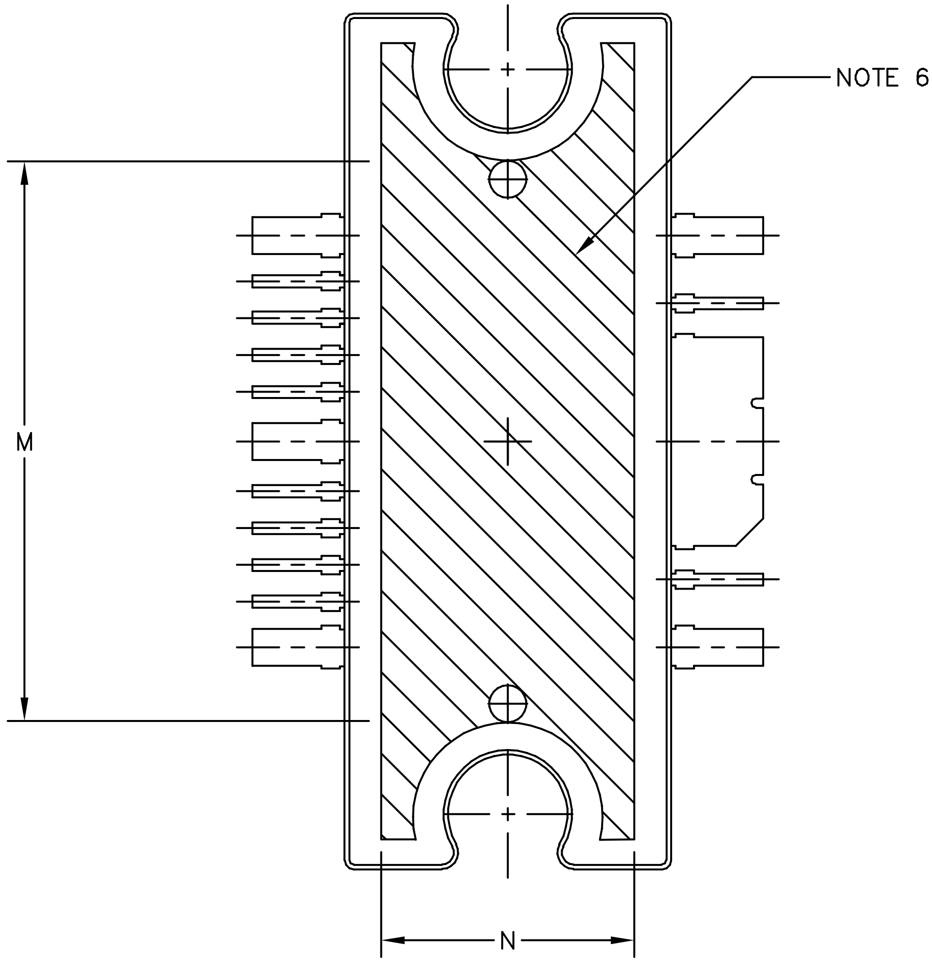
TITLE: TO−272 WIDE BODY MULTI−LEAD	DOCUMENT NO: 98ARH99164A	REV: L
	CASE NUMBER: 1329−09	13 MAR 2006
	STANDARD: NON−JEDEC	



VIEW Y–Y

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–272 WIDE BODY MULTI–LEAD	DOCUMENT NO: 98ARH99164A	REV: L
	CASE NUMBER: 1329–09	13 MAR 2006
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

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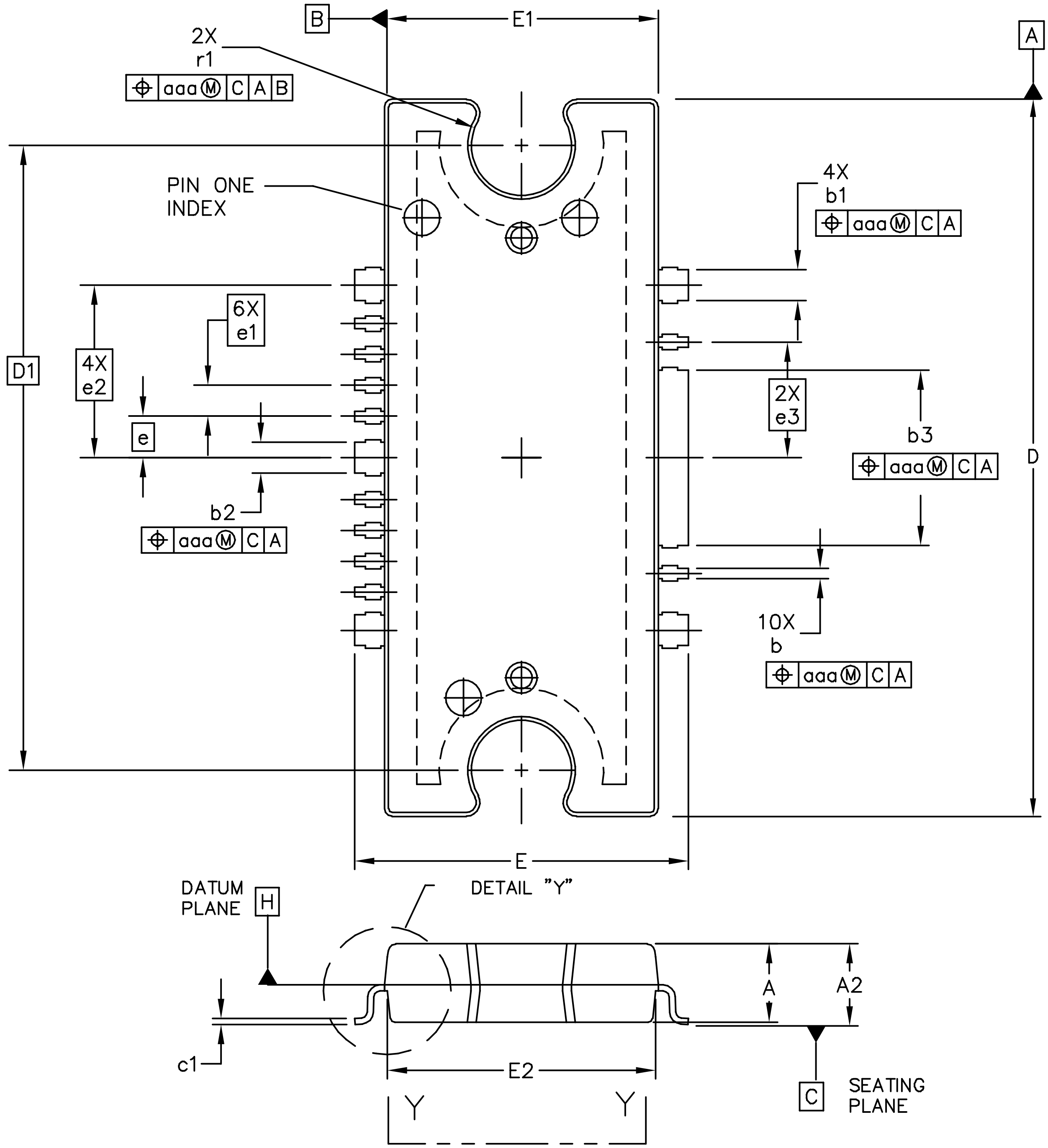
	STANDARD: NON–JEDEC	



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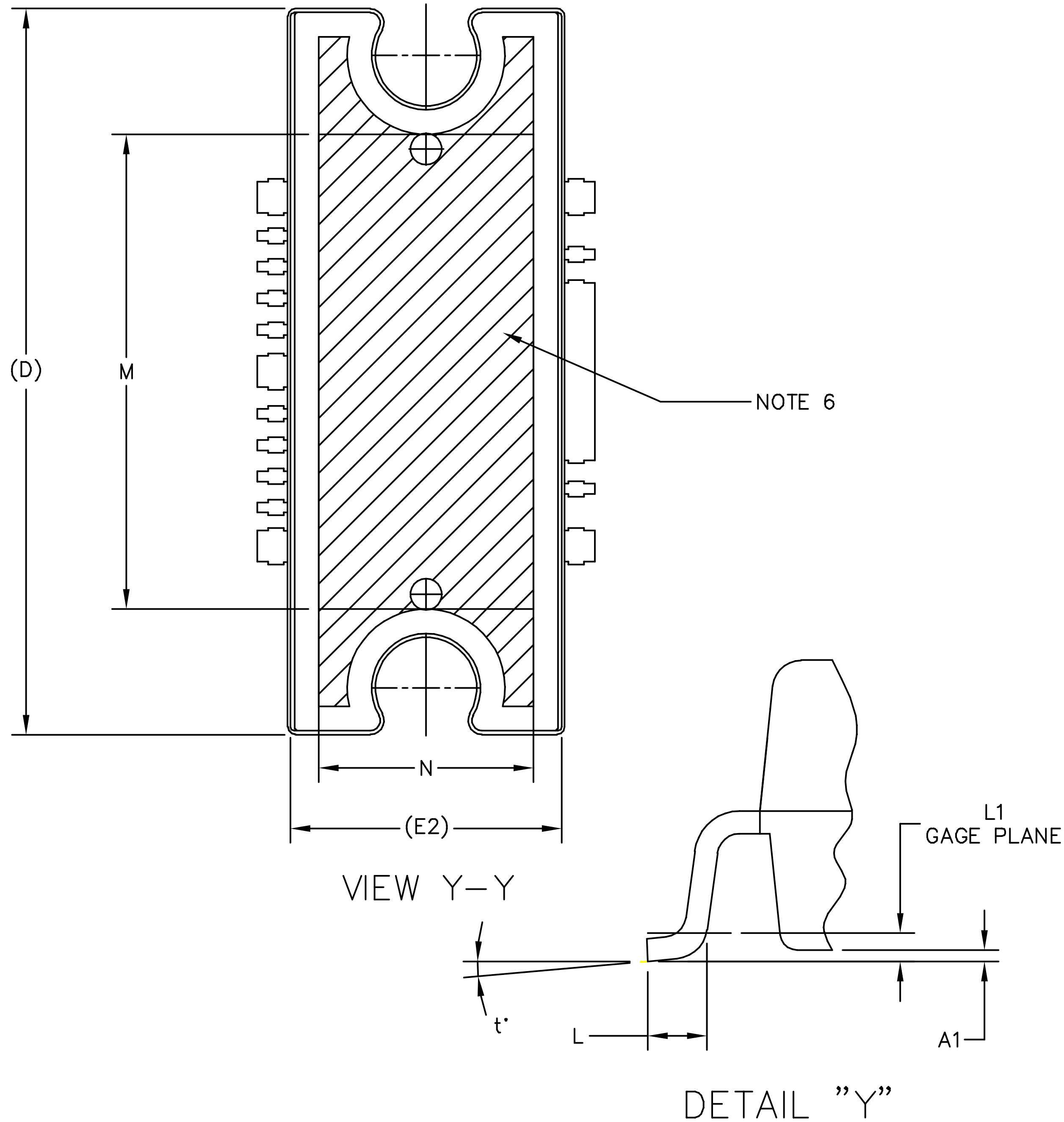
	CASE NUMBER: 1329A–03	3 APR 2006
	STANDARD: NON–JEDEC	



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TITLE: TO–272WB, 16 LEAD GULL WING PLASTIC		DOCUMENT NO: 98ASA10532D	REV: E
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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	4.90	5.06	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		.025 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2°	8°	2°	8°
N	.270	----	6.86						
				----	aaa	.004		.10	

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