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MX25L12845G

3V, 128M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Protocol Support - Single I/O, Dual I/O and Quad I/O*
- *Support DTR (Double Transfer Rate) Mode*
- *Support clock frequency up to 133MHz*

Contents

3V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 134,217,728 x 1 bit structure
  or 67,108,864 x 2 bits (two I/O mode) structure
  or 33,554,432 x 4 bits (four I/O mode) structure
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V
- Fast read for SPI mode
  - Support clock frequency up to 133MHz for all protocols
  - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Support DTR (Double Transfer Rate) Mode
  - Configurable dummy cycle number for fast read operation
- Quad Peripheral Interface (QPI) available
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Programming:
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Individual sector protection function (Solid Protect)
- Additional 4K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware Write Protection or Serial Data Input/Output for 4 x I/O read mode
- RESET#/SIO3
  - Hardware Reset pin or Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-pins SOP (200mil)
  - 8-land WSON (8x6mm, 6x5mm)
  - 24-ball BGA (4x6 ball array)
  - 24-Ball BGA (5x5 ball array)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L12845G is 128Mb bits Serial NOR Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108,864 bits x 2 or 33,554,432 bits x 4. MX25L12845G features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# and RESET# pin (of the 8-pin packages) become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25L12845G MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25L12845G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

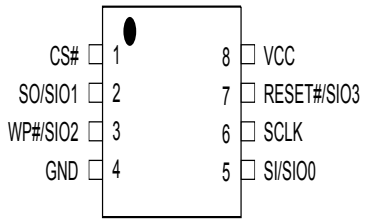
Table 1. Read performance Comparison

Numbers of Dummy Cycles	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual IO Fast Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	80*	54	-
6	-	-	-	-	80*	54*
8	120*/133R	120*/133R	120*/133R	120/133R	84/104R	70/80R
10	-	-	-	-	120/133R	84/100R

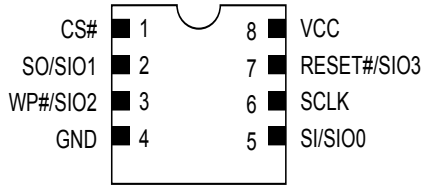
Notes:
1. * mean default status.
2. R mean VCC range = 3.0V-3.6V.

3. PIN CONFIGURATIONS

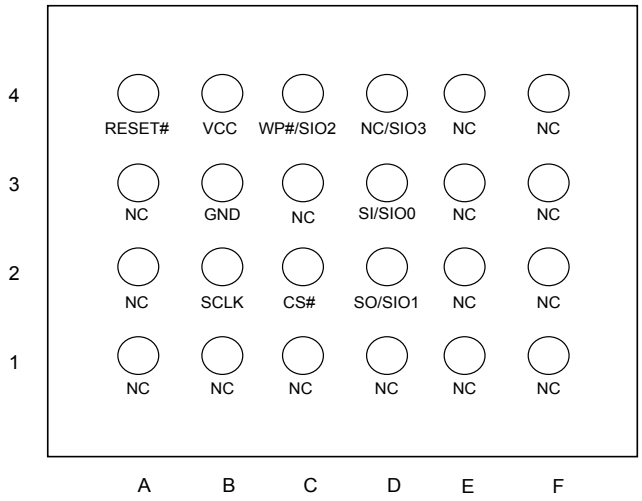
8-PIN SOP (200mil)



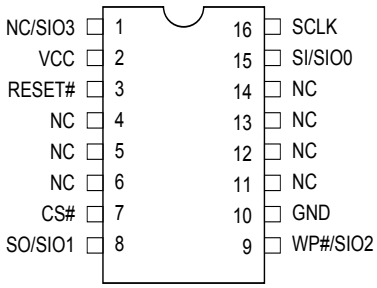
8-WSON (8x6mm, 6x5mm)



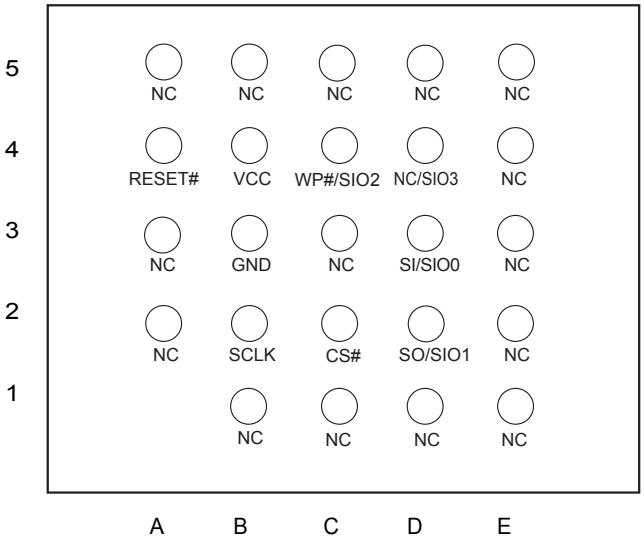
24-Ball BGA (4x6 ball array)



16-PIN SOP (300mil)



24-Ball BGA (5x5 ball array)

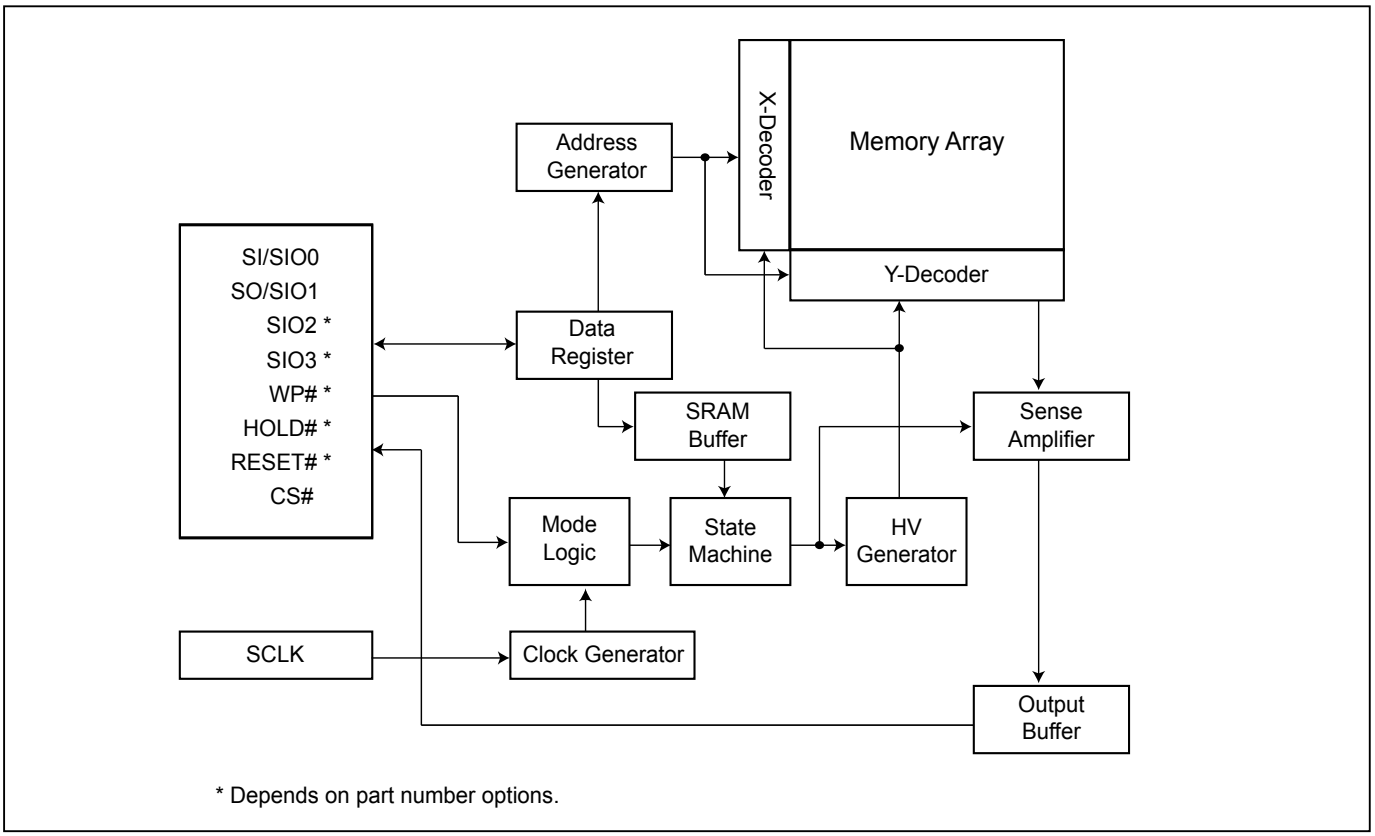


4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#*/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
RESET#*/SIO3	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC or Serial Data Input & Output (for 4xI/O read mode)
RESET#*	Hardware Reset Pin Active low
VCC	+ 3V Power Supply
GND	Ground
NC	No Connection

***Note:** The pin of RESET#, RESET#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration.
However, the internal pull up function will be disabled if the system has physical connection to RESET#, RESET#/SIO3 or WP#/SIO2 pin.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 255th)
0	0	1	0	2 (2 blocks, block 254th-255th)
0	0	1	1	3 (4 blocks, block 252nd-255th)
0	1	0	0	4 (8 blocks, block 248th-255th)
0	1	0	1	5 (16 blocks, block 240th-255th)
0	1	1	0	6 (32 blocks, block 224th-255th)
0	1	1	1	7 (64 blocks, block 192nd-255th)
1	0	0	0	8 (128 blocks, block 128th-255th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th-1st)
0	0	1	1	3 (4 blocks, protected block 0th-3rd)
0	1	0	0	4 (8 blocks, protected block 0th-7th)
0	1	0	1	5 (16 blocks, protected block 0th-15th)
0	1	1	0	6 (32 blocks, protected block 0th-31st)
0	1	1	1	7 (64 blocks, protected block 0th-63rd)
1	0	0	0	8 (128 blocks, protected block 0th-127th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 12. Security Register Definition"* for security register bit definition and *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010-xxx1FF	3968-bit	N/A	

7. Memory Organization

Table 4. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
255	511	4095	FFF000h	FFFFFFh
		⋮		
		4088	FF8000h	FF8FFFh
	510	4087	FF7000h	FF7FFFh
		⋮		
		4080	FF0000h	FF0FFFh
254	509	4079	FEF000h	FEFFFFh
		⋮		
		4072	FE8000h	FE8FFFh
	508	4071	FE7000h	FE7FFFh
		⋮		
		4064	FE0000h	FE0FFFh
253	507	4063	FDF000h	FDFFFFh
		⋮		
		4056	FD8000h	FD8FFFh
	506	4055	FD7000h	FD7FFFh
		⋮		
		4048	FD0000h	FD0FFFh
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

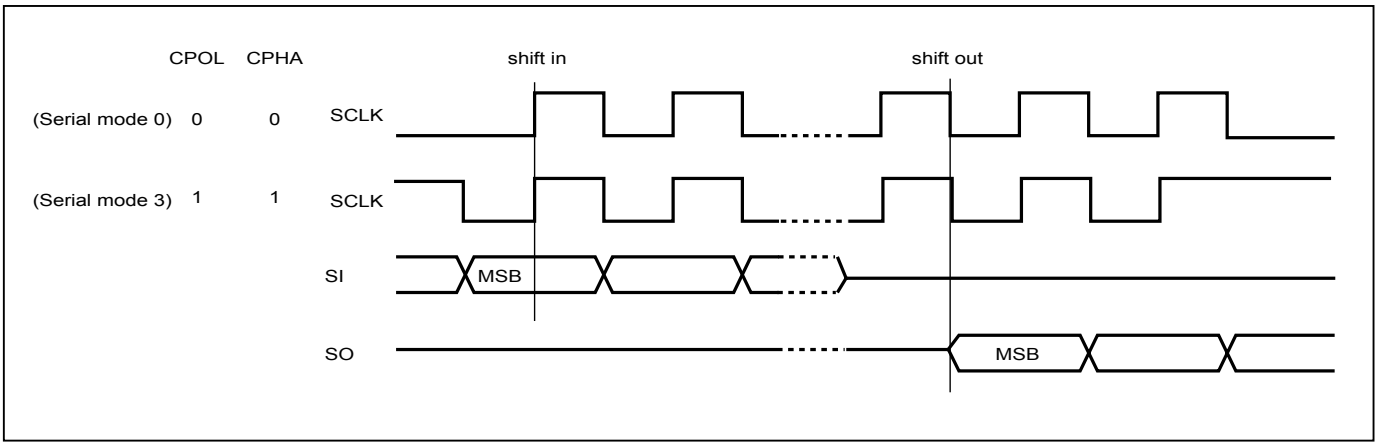
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, DREAD, 4READ, QREAD, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDCR, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

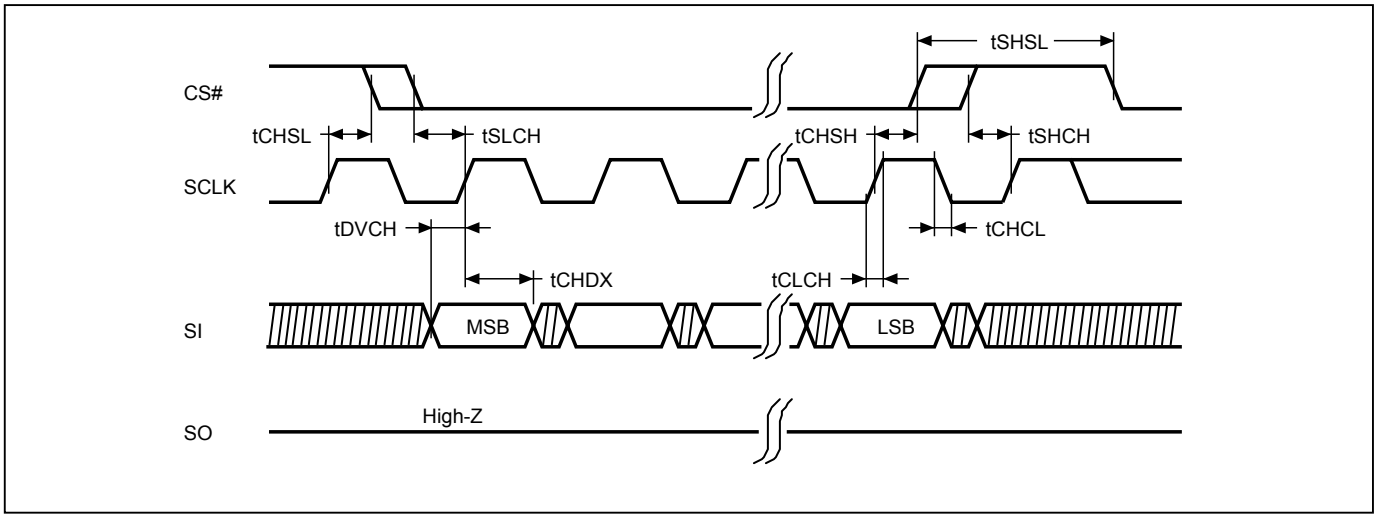


Figure 3. Output Timing (STR mode)

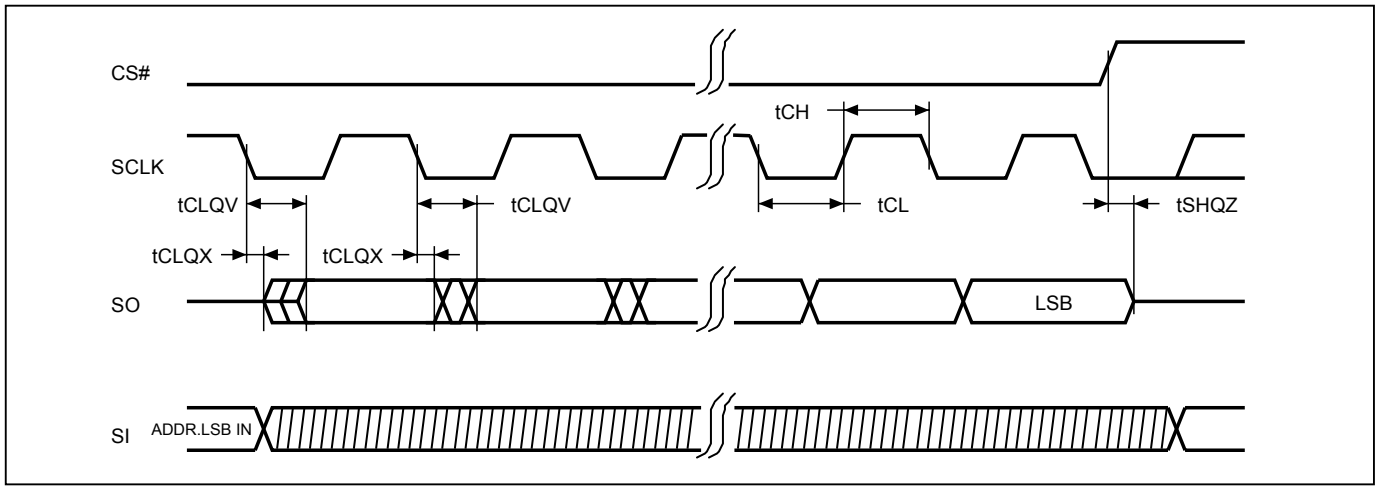
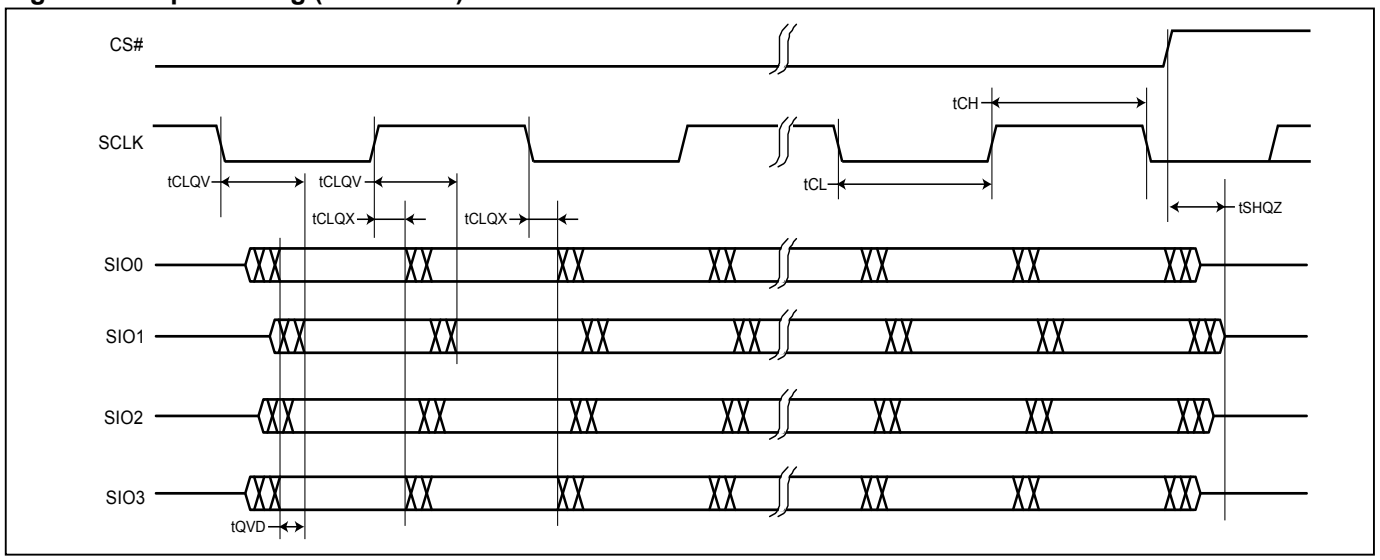


Figure 4. Output Timing (DTR mode)



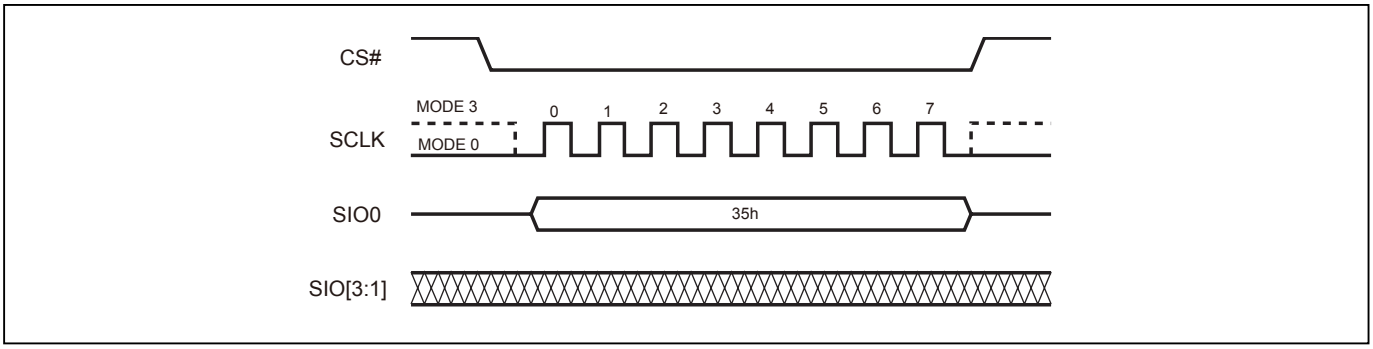
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing EQIO(35h) command, the QPI mode is enabled. After QPI mode is enabled, the device enters quad mode (4-4-4) without QE bit status changed.

Figure 5. Enable QPI Sequence

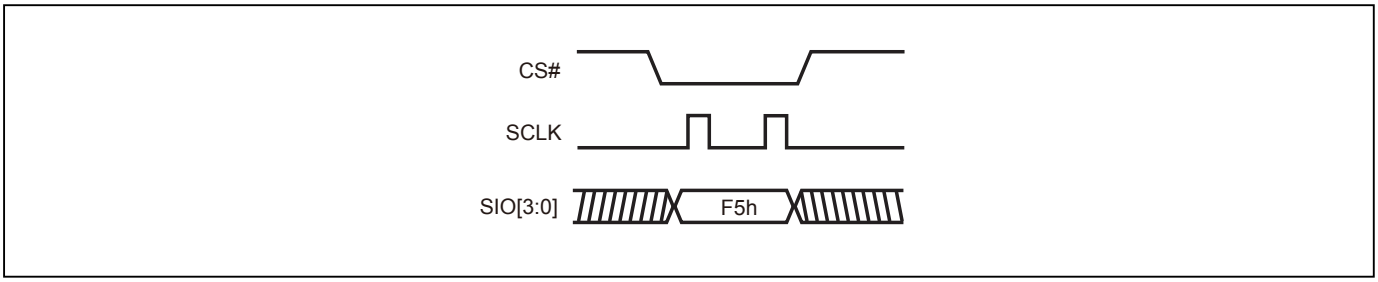


Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:
For EQIO and RSTQIO commands, CS# high width has to follow "From Write/Erase/Program to Read Status Register" specification of tSHSL (as defined by *"Table 22. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)"*) for next instruction.

Figure 6. Reset QPI Mode



9. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)(Note 1)	DREAD (1I 2O read)	4READ	QREAD (1I 4O read)	4DTRD (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	3	3	3	3	3	3	3
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)	ED (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	Quad I/O read for bottom 128Mb with 6 dummy cycles	n bytes read out by Quad output until CS# goes high	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3	3	3	3	3	0
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte		ADD1	ADD1	ADD1	ADD1	
3rd byte		ADD2	ADD2	ADD2	ADD2	
4th byte		ADD3	ADD3	ADD3	ADD3	
5th byte						
Data Cycles	1-256	1-256				
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	FMEN (factory mode enable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	WPSEL (Write Protect Selection)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI
1st byte	06 (hex)	04 (hex)	41 (hex)	05 (hex)	15 (hex)	01 (hex)	68 (hex)
2nd byte						Values	
3rd byte						Values	
4th byte							
5th byte							
Data Cycles						1-2	
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	enable factory mode	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register	to enter and enable individal block protect mode

Command (byte)	EQIO (Enable QPI)	RSTQIO (Reset QPI)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)
Mode	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	35 (hex)	F5 (hex)	B0 (hex)	30 (hex)	B9 (hex)	AB (hex)	C0 (hex)
2nd byte							
3rd byte							
4th byte							
5th byte							
Data Cycles							
Action	Entering the QPI mode	Exiting the QPI mode			enters deep power down mode	release from deep power down mode	to set Burst length

ID/Security Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	0	0	3	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1		
3rd byte		x	x		ADD2		
4th byte			ADD1		ADD3		
5th byte					Dummy(8)(Note 5)		
Data Cycles							
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID(Note 2)	ID in QPI interface	Read SFDP mode	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	WRSPB (SPB bit program)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	WRDPB (write DPB register)	RDDPB (read DPB register)
Mode	SPI/QPI	SPI/QPI	SPI	SPI	SPI	SPI	SPI
Address Bytes	0	0	4	0	4	4	4
1st byte	2B (hex)	2F (hex)	E3 (hex)	E4 (hex)	E2 (hex)	E1 (hex)	E0 (hex)
2nd byte			ADD1		ADD1	ADD1	ADD1
3rd byte			ADD2		ADD2	ADD2	ADD2
4th byte			ADD3		ADD3	ADD3	ADD3
5th byte			ADD4		ADD4	ADD4	ADD4
Data Cycles					1	1	1
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)					

Command (byte)	GBLK (gang block lock)	GBULK (gang block unlock)	WRLR (write lock register)	RDLR (read lock register)
Mode	SPI	SPI	SPI	SPI
Address Bytes	0	0	0	0
1st byte	7E (hex)	98 (hex)	2C (hex)	2D (hex)
2nd byte				
3rd byte				
4th byte				
5th byte				
Data Cycles			2	2
Action	whole chip write protect	whole chip unprotect		

Reset Commands

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)(Note 4)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1 which is different from 1 x I/O condition.
Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 4: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.
Note 5: The number in parentheses after "Dummy" stands for how many clock cycles it has.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 7. Write Enable (WREN) Sequence (SPI Mode)

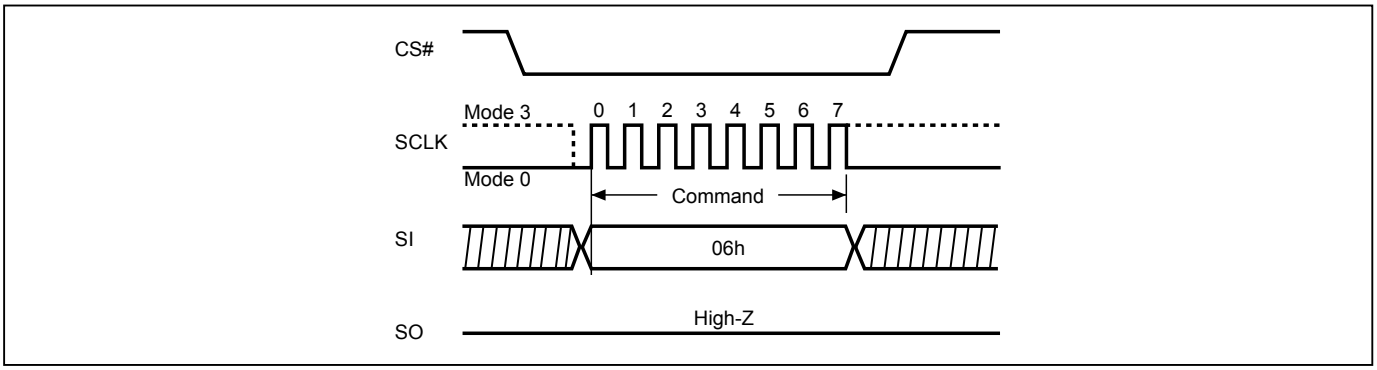
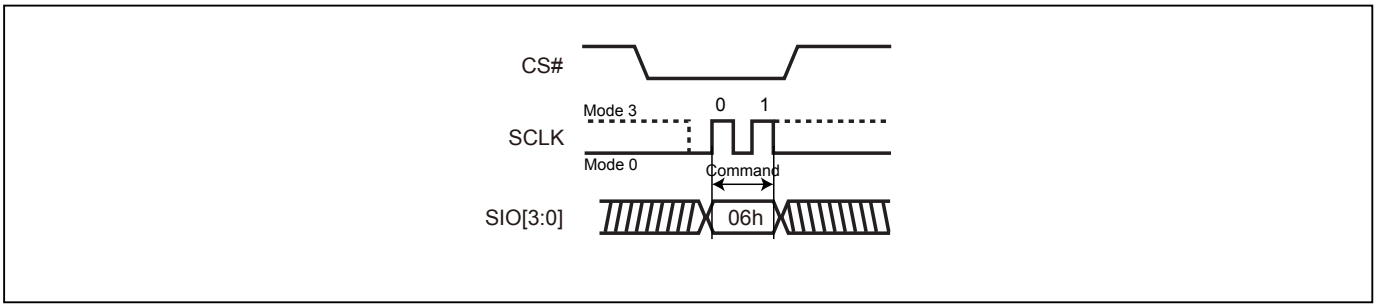


Figure 8. Write Enable (WREN) Sequence (QPI Mode)



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WRLR command completion
- WRSPB command completion
- WRDPB command completion
- ESSPB command completion

Figure 9. Write Disable (WRDI) Sequence (SPI Mode)

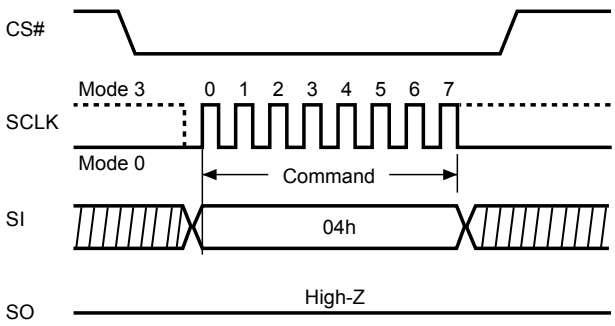
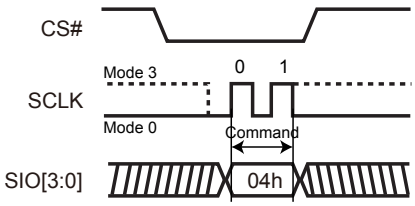


Figure 10. Write Disable (WRDI) Sequence (QPI Mode)



9-3. Factory Mode Enable (FMEN)

The Factory Mode Enable (FMEN) instruction is for enhance Program and Erase performance for increase factory production throughput. The FMEN instruction need to combine with the instructions which are intended to change the device content, like PP, 4PP, SE, BE32K, BE, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→sending FMEN instruction code→ CS# goes high. A valid factory mode operation need to included three sequences: WREN instruction → FMEN instruction→ Program or Erase instruction.

Suspend command is not acceptable under factory mode.

The FMEN is reset by following situations

- Power-up
- Reset# pin driven low
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- Softreset command completion

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 11. Factory Mode Enable (FMEN) Sequence (SPI Mode)

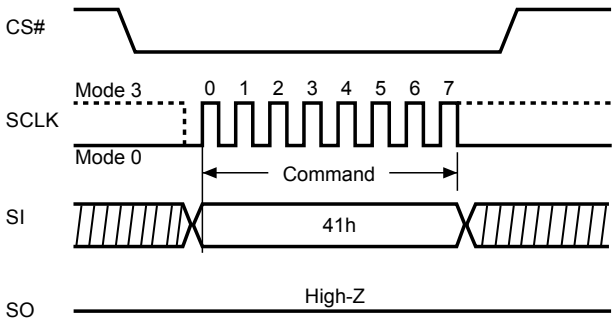
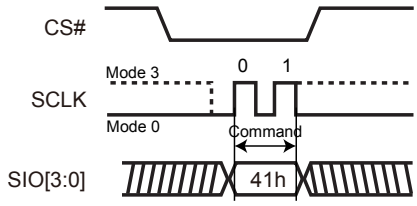


Figure 12. Factory Mode Enable (FMEN) Sequence (QPI Mode)



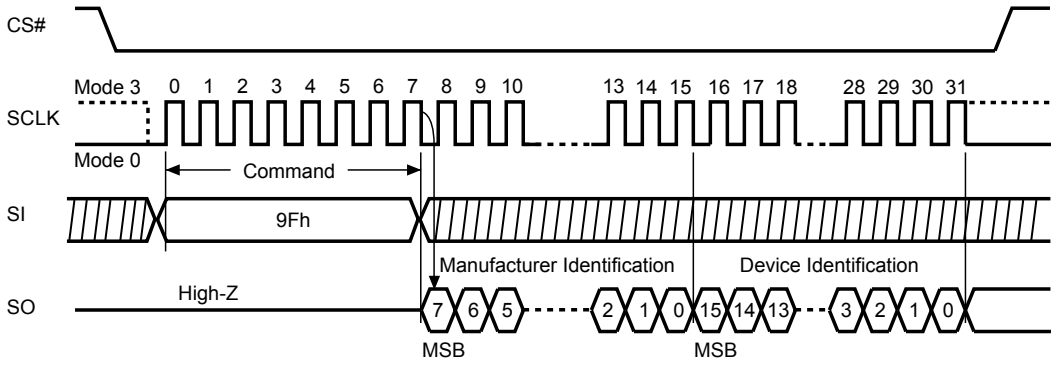
9-4. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 6. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 13. Read Identification (RDID) Sequence (SPI mode only)



9-5. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 22. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 14. Read Electronic Signature (RES) Sequence (SPI Mode)

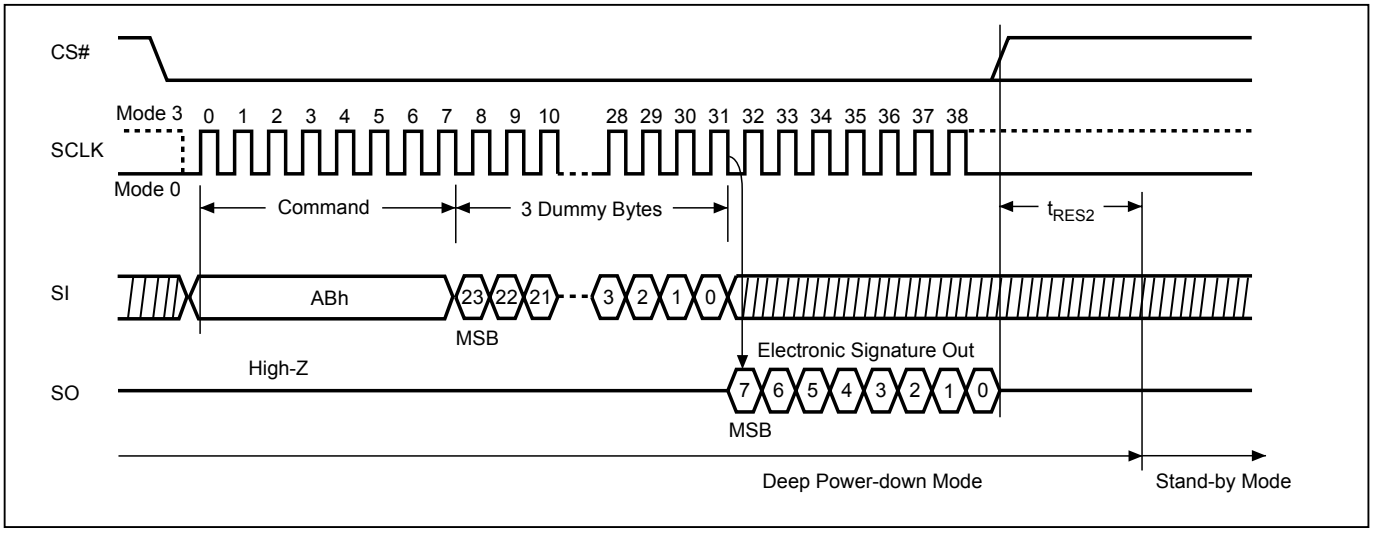


Figure 15. Read Electronic Signature (RES) Sequence (QPI Mode)

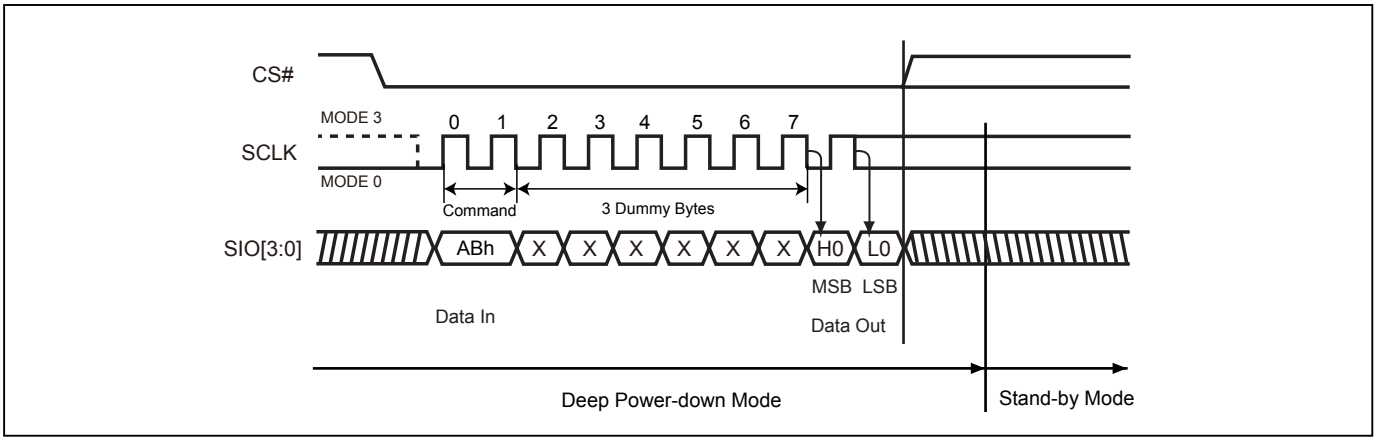


Figure 16. Release from Deep Power-down (RDP) Sequence (SPI Mode)

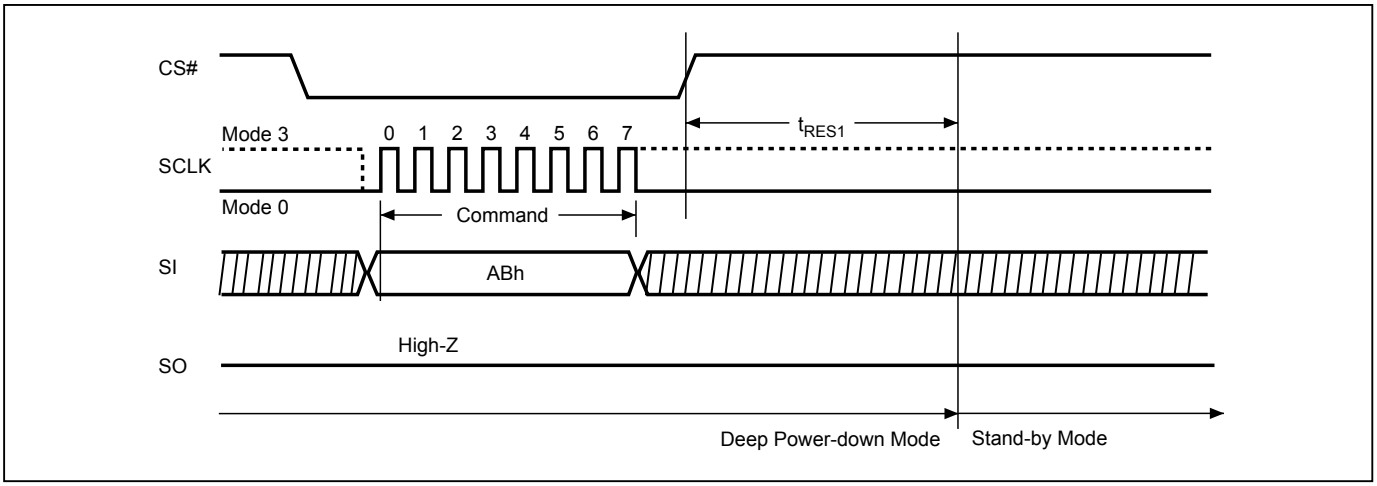


Figure 17. Release from Deep Power-down (RDP) Sequence (QPI Mode)