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MX25L1633E

DATASHEET

Contents

16M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

FEATURES

General

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (two I/O read mode) structure or 4,194,304 x 4 bits (four I/O read mode) structure
- 512 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

Performance

- High Performance
  - Fast read
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 85MHz with 4 dummy cycles
    - 4 I/O: 85MHz with 6 dummy cycles
  - Fast access time: 104MHz serial clock
  - Serial clock of four I/O read mode : 85MHz, which is equivalent to 340MHz
  - Fast program time: 0.6ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Fast erase time: 40ms (typ.)/sector (4K-byte per sector) ; 0.4s(typ.) /block (64K-byte per block); 5s(typ.) /chip
- Low Power Consumption
  - Low active read current: 25mA(max.) at 104MHz and 10mA(max.) at 33MHz
  - Low active programming current: 15mA (typ.)
  - Low active sector erase current: 9mA (typ.)
  - Low standby current: 15uA (typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

Software Features

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 512-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - Both REMS,REMS2 and REMS4 commands for 1-byte manufacturer ID and 1-byte device ID

Hardware Features

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- NC/SIO3
  - NC pin or serial data Input/Output for 4 x I/O read mode
- PACKAGE
  - 8-land WSON (6x5mm)
  - 8-land USON (4x4mm)
  - 8-pin SOP (200mil)
  - **All devices are RoHS Compliant & Halogen-free.**

GENERAL DESCRIPTION

The MX25L1633E are 16,777,216 bit serial Flash memory, which is configured as 2,097,152 x 8 internally. When it is in two or four I/O read mode, the structure becomes 8,388,608 bits x 2 or 4,194,304 bits x 4. The MX25L1633E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and NC pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25L1633E provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, and erase command is executes on sector (4K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

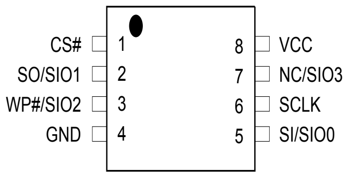
The MX25L1633E utilizes Macronix proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

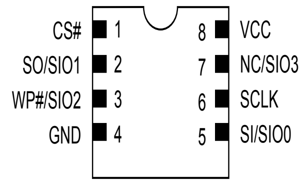
Additional Features / Part Name	Protection and Security		Read Performance		Identifier				
	Flexible Block Protection (BP0-BP3)	512-bit secured OTP	2 I/O Read	4 I/O Read	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	RDID (command: 9F hex)
MX25L1633E	V	V	V	V	24 (hex)	C2 24 (hex) (if ADD=0)	C2 24 (hex) (if ADD=0)	C2 24 (hex) (if ADD=0)	C2 24 15 (hex)
MX25L1635D	V	V	V	V	24 (hex)	C2 24 (hex) (if ADD=0)	C2 24 (hex) (if ADD=0)	C2 24 (hex) (if ADD=0)	C2 24 15 (hex)

PIN CONFIGURATIONS

8-PIN SOP (200mil)



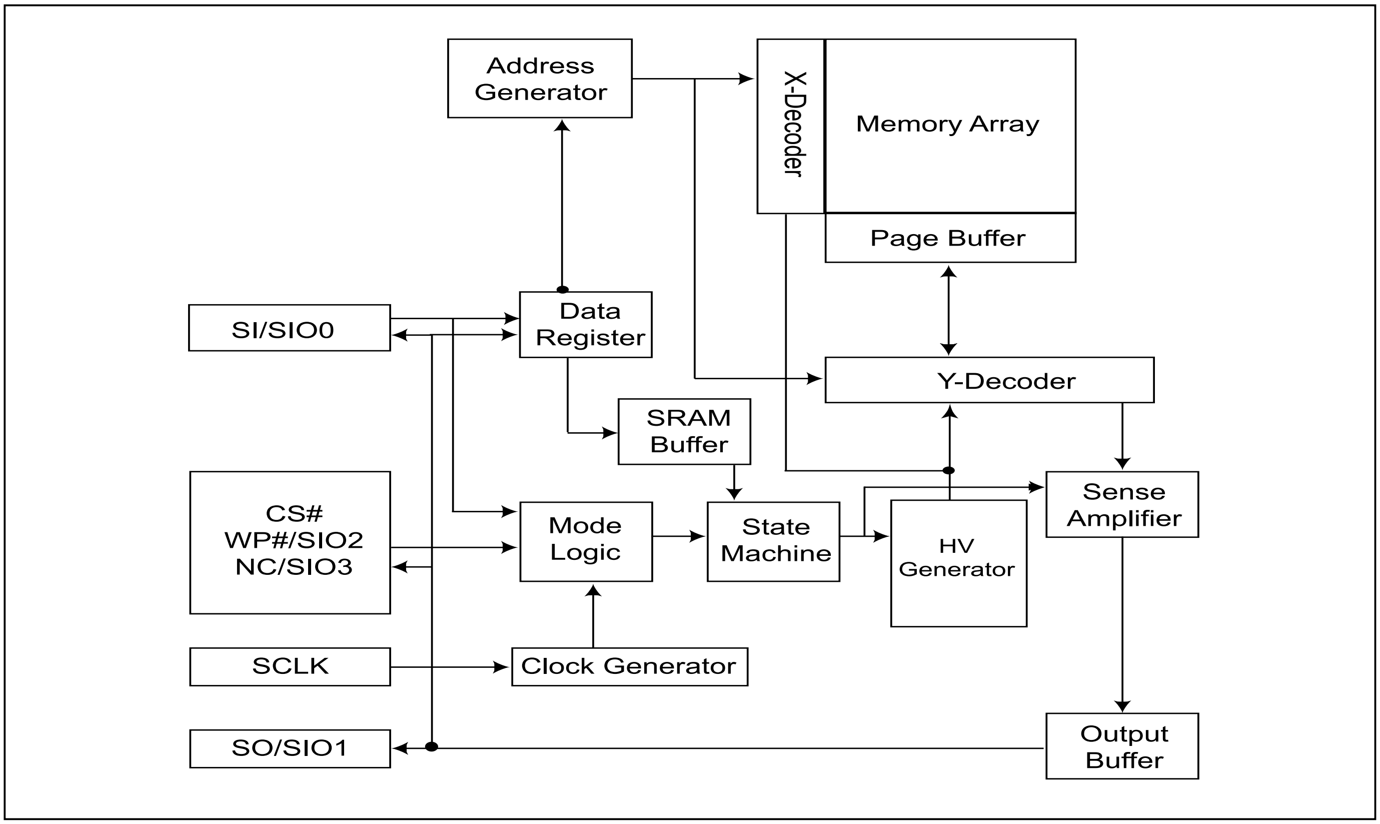
8-LAND WSON (6x5mm), USON (4x4mm)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC pin (Not connect) or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 3.3V Power Supply
GND	Ground

BLOCK DIAGRAM



DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP, 4PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and securuity features which protect content from inadvertent write and hostile access.

  I. Block lock protection
  - The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The proected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
  Please refer to table of "protected area sizes".

  - The Hardware Proteced Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O read mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	16Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, protected block 31th)
0	0	1	0	2 (2blocks, protected block 30th-31th)
0	0	1	1	3 (4blocks, protected block 28th-31th)
0	1	0	0	4 (8blocks, protected block 24th-31th)
0	1	0	1	5 (16blocks, protected block 16th-31th)
0	1	1	0	6 (32blocks, protected all)
0	1	1	1	7 (32blocks, protected all)
1	0	0	0	8 (32blocks, protected all)
1	0	0	1	9 (32blocks, protected all)
1	0	1	0	10 (16blocks, protected block 0th-15th)
1	0	1	1	11 (24blocks, protected block 0th-23th)
1	1	0	0	12 (28blocks, protected block 0th-27th)
1	1	0	1	13 (30blocks, protected block 0th-29th)
1	1	1	0	14 (31blocks, protected block 0th-30th)
1	1	1	1	15 (32blocks, protected all)

II. Additional 512-bit secured OTP for unique identifier: to provide 512-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to *table 3. 512-bit secured OTP definition*.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 512-bit secured OTP by entering 512-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 512-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "security register definition" for security register bit definition and table of "512-bit secured OTP definition" for address range definition.

- ***Note:*** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512-bit secured OTP mode, array access is not allowed.

Table 3. 512-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128-bit	ESN (electrical serial number)	Determined by customer
xxxx10~xxxx3F	384-bit	N/A	

Memory Organization

Table 4. Memory Organization

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	:	:	:
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	:	:	:
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	:	:	:
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	:	:	:
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	:	:	:
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	:	:	:
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	:	:	:
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	:	:	:
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	:	:	:
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	:	:	:
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	:	:	:
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	:	:	:
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	:	:	:
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	:	:	:
	256	100000h	100FFFh

Block	Sector	Address Range	
15	255	0FF000h	0FFFFFh
	:	:	:
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	:	:	:
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	:	:	:
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	:	:	:
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	:	:	:
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	:	:	:
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	:	:	:
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	:	:	:
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	:	:	:
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	:	:	:
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	:	:	:
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	:	:	:
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	:	:	:
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	:	:	:
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, all SO pins of this LSI should be High-Z.

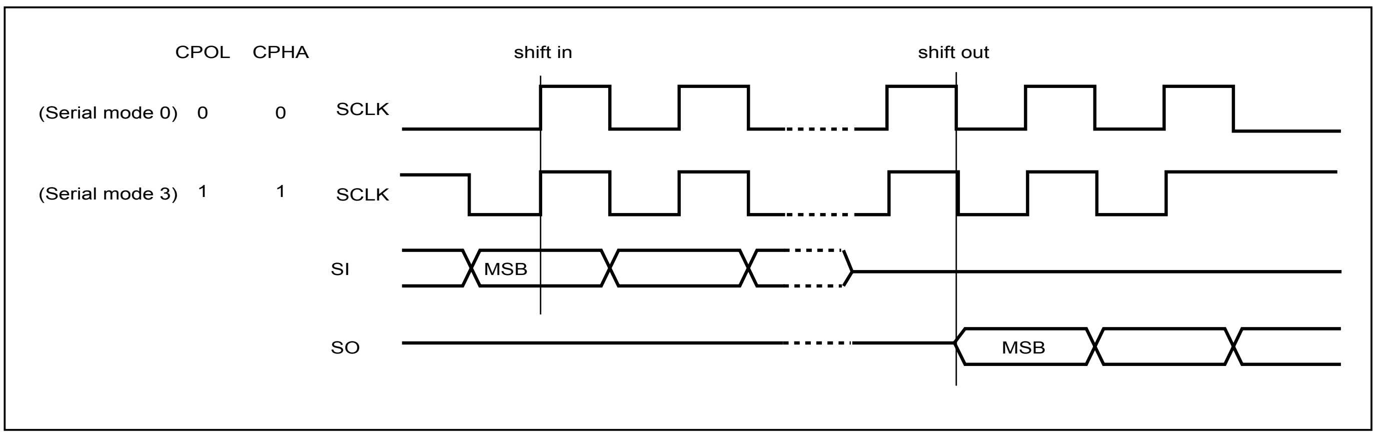
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *Figure 1*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, 4READ, RES, REMS, REMS2, and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, 4PP, RDP, DP, ENSO, EXSO,and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master,

-CPOL=1 for SCLK high while idle,

-CPOL=0 for SCLK low while not transmitting.

CPHA indicates clock phase.

The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

Table 5. Command Set

Command (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identific-ation)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)	2READ (2 x I/O read command) Note1	4READ (4 x I/O read command) Note2
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	03 (hex)	0B (hex)	BB (hex)	EB (hex)
2nd byte					Values	AD1 (A23-A16)	AD1	ADD(2)	ADD(4) & Dummy(4)
3rd byte						AD2 (A15-A8)	AD2	ADD(2) & Dummy(2)	Dummy(4)
4th byte						AD3 (A7-A0)	AD3		
5th byte							Dummy		
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufact-urer ID & 2-byte Device ID	to read out the values of the status register	to write new values of the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by 4 x I/O until CS# goes high

Command (byte)	4PP (quad page program)	SE (sector erase)	BE (block erase)	CE (chip erase)	PP (page program)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)
1st byte	38 (hex)	20 (hex)	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	AB (hex)
2nd byte	AD1	AD1	AD1		AD1			x
3rd byte		AD2	AD2		AD2			x
4th byte		AD3	AD3		AD3			x
Action	quad input to program the selected page	to erase the selected sector	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID

Command (byte)	Release Read Enhanced	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)
1st byte	FFh (hex)	90 (hex)	EF (hex)	DF (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte	x	x	X	x				
3rd byte	x	x	X	x				
4th byte	x	ADD (Note 3)	ADD (Note 3)	ADD (Note 3)				
Action	All these commands FFh, 00h, AAh or 55h will escape the performance enhance mode	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	to enter the 512-bit secured OTP mode	to exit the 512-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O.
Note 2: The count base is 4-bit for ADD(4) and Dummy(4) because of 4 x I/O.
Note 3: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 4: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→CS# goes high. (see *Figure 9*)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high. (see *Figure 10*)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Quad Page Program (4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID is C2(hex), the memory type ID is 24(hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as table of "ID Definitions". (see *table 7*)

The sequence of issuing RDID instruction is: CS# goes low→sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (see *Figure 11*.)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→sending RDSR instruction code→Status Register data out on SO (see *Figure 12*)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in *table 2*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

QE bit. The Quad Enable (QE) bit, non-volatile bit, performs Quad when it is reset to "0" (factory default) to enable WP# or is set to "1" to enable Quad SIO2 and SIO3.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, which is set to "0" (factory default). The SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	*(note 1)*	*(note 1)*	*(note 1)*	*(note 1)*	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the table 2 "*Protected Area Size*".

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *table 2*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the statur register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→sending WRSR instruction code→Status Register data on SI→ CS# goes high. (see *Figure 13*)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 6. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3, QE bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3, QE of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *Table 2*.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0 and QE. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0 and QE. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note:
If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.
If the system goes into four I/O read mode, the feature of HPM will be disabled.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→data out on SO→to end READ operation can use CS# to high at any time during data out. (see *Figure 14*)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (see *Figure 15*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→4 dummy cycles on SIO1 & SIO0→data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (see *Figure 16* for 2 x I/O Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(9) 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out (see *Figure 17* for 4 x I/O Read Mode Timing Waveform).

Another sequence of issuing 4 READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→24-bit address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out interleave on SIO3, SIO2, SIO1 and SIO0 till CS# goes high →CS# goes low (reduce 4 Read instruction) →24-bit random access address (see *Figure 18* for 4x I/O read enhance performance mode timing waveform).

In the performance-enhancing mode (Note of *Figure. 18*), P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h. And afterwards CS# is raised or issuing FF command (CS# goes high → CS# goes low→sending 0xFF→CS# goes high) instead of no toggling, the system then will escape from performance enhance mode and return to normal opertaion. In these cases, tSHSL=15ns(min) will be specified.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *table 3*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the eighth bit of last address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→sending SE instruction code→3-byte address on SI →CS# goes high. (see Figure 21)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

(11) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see *table 3*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the eighth bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low →sending BE instruction code→3-byte address on SI →CS# goes high. (see *Figure 22*)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

(12) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary (the eighth bit of instruction code been latched-in), otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→ sending CE instruction code→ CS# goes high. (see *Figure 23*)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

(13) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence of issuing PP instruction is: CS# goes low→sending PP instruction code→3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (see *Figure 19*)

The CS# must be kept to low during the whole Page Program instruction cycle; The CS# must go high exactly at the byte boundary(the eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in

Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(14) 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 85MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 85MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→sending 4PP instruction code→3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high. (see Figure 20)

(15) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→ CS# goes high. (see *Figure 24*)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

(16) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in *Table 10. AC Characteristics*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *table of ID Definitions* in next page. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The sequence is shown as *Figure 25* and *Figure 26*. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

(17) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2 & REMS4 instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID. The REMS4 instruction is recommended to use for 4 I/O identification and REMS2 instruction is recommended to use for 2 I/O identification.

The REMS, REMS2 & REMS4 instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" or "EFh" or "DFh" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 27*. The Device ID values are listed in *Table 7 of ID Definitions* in next page. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table 7. ID Definitions

RDID Command	manufacturer ID	memory type	memory density
	C2	24	15
RES Command	electronic ID		
	24		
REMS/REMS2/REMS4/ Command	manufacturer ID	device ID	
	C2	24	

(18) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512-bit secured OTP mode. The additional 512-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

(19) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→sending EXSO instruction to exit Secured OTP mode→CS# goes high.

(20) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→ sending RDSCUR instruction → Security Register data out on SO→CS# goes high.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non- factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512-bit Secured OTP area cannot be update any more. While it is in 512-bit secured OTP mode, main array access is not allowed.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	x	x	LDSO (indicate if lock-down	Secured OTP indicator bit
reserved	reserved	reserved	reserved	reserved	reserved	0 = not lock-down 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit

(21) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→sending WRSCUR instruction→CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the figure of "*power-up timing*".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to 4.6V
Applied Output Voltage		-0.5V to 4.6V
VCC to Ground Potential		-0.5V to 4.6V

NOTICE:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see *Figure 2*, and *Figure 3*.

Figure 2. Maximum Negative Overshoot Waveform

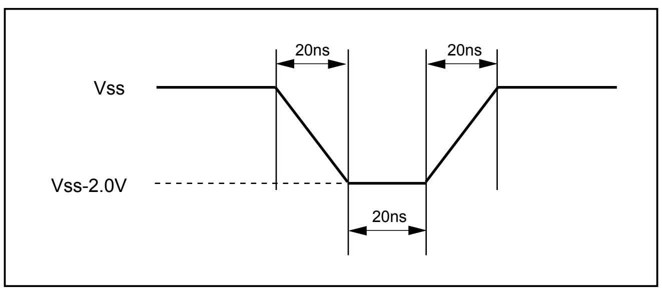
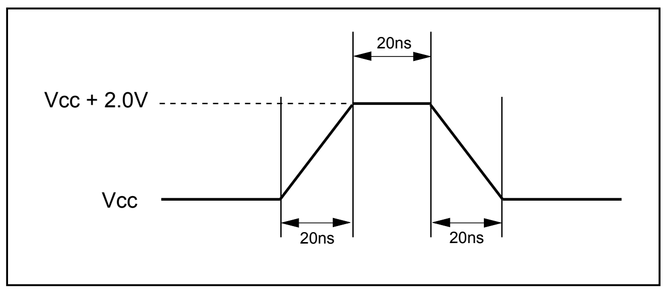


Figure 3. Maximum Positive Overshoot Waveform



Capacitance

TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V