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MX25L1673E

HIGH PERFORMANCE

SERIAL FLASH SPECIFICATION

Contents

16M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (two I/O read mode) structure or 4,194,304 x 4 bits (four I/O read mode) structure
- 512 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Permanent fixed QE bit, QE =1 and 4 I/O mode is enabled

PERFORMANCE

- High Performance
  - Fast read
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 85MHz with 4 dummy cycles
    - 4 I/O: 85MHz with 6 dummy cycles
  - Fast access time: 104MHz serial clock
  - Serial clock of four I/O read mode : 85MHz, which is equivalent to 340MHz
  - Fast program time: 0.6ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Fast erase time: 40ms (typ.)/sector (4K-byte per sector) ; 0.4s(typ.) /block (64K-byte per block); 5s(typ.) /chip
- Low Power Consumption
  - Low active read current: 25mA(max.) at 104MHz and 10mA(max.) at 33MHz
  - Low active programming current: 15mA (typ.)
  - Low active sector erase current: 9mA (typ.)
  - Low standby current: 15uA (typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 512-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - Both REMS,REMS2 and REMS4 commands for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SIO2
  - Serial data Input/Output for 4 x I/O read mode
- SIO3
  - Serial data Input/Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (200mil)
  - 8-WSON (6x5mm)
  - **All devices are RoHS Compliant & Halogen-free.**

2. GENERAL DESCRIPTION

The MX25L1673E are 16,777,216 bit serial Flash memory, which is configured as 2,097,152 x 8 internally. When it is in two or four I/O read mode, the structure becomes 8,388,608 bits x 2 or 4,194,304 bits x 4. The MX25L1673E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin become SIO0 pin and SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

The MX25L1673E provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, and erase command is executes on sector (4K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

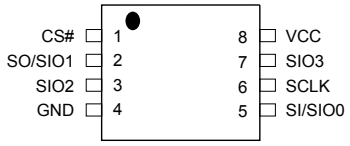
The MX25L1673E utilizes Macronix proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Feature

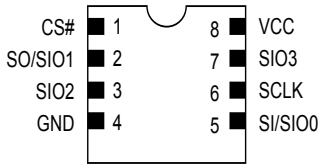
Additional Features / Part Name	Protection and Security		Read Performance		Identifier				
	Flexible Block Protection (BP0-BP3)	512-bit secured OTP	2 I/O Read	4 I/O Read	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	RDID (command: 9F hex)
MX25L1673E	V	V	V	V	24 (hex)	C2 24 (hex) (if ADD=0)	C2 24 (hex) (if ADD=0)	C2 24 (hex) (if ADD=0)	C2 24 15 (hex)

3. PIN CONFIGURATION

8-PIN SOP (200mil)



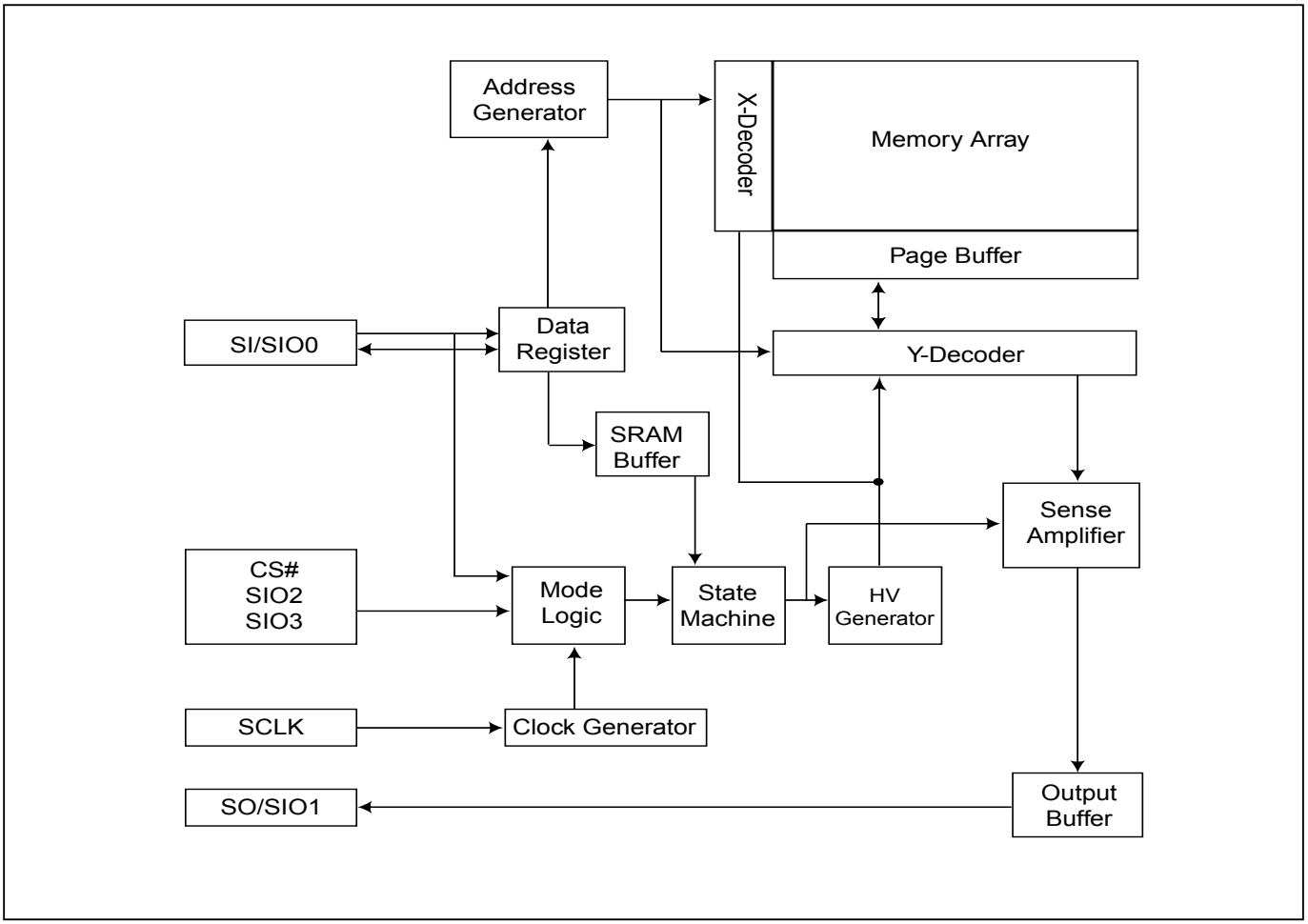
8-WSON (6x5mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
SIO2	Serial Data Input & Output (for 4xI/O read mode)
SIO3	Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 3.3V Power Supply
GND	Ground

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP, 4PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and securuity features which protect content from inadvertent write and hostile access.

  I. Block lock protection

  - The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The proected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
  Please refer to table of "protected area sizes".

Table 2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	16Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, protected block 31th)
0	0	1	0	2 (2blocks, protected block 30th-31th)
0	0	1	1	3 (4blocks, protected block 28th-31th)
0	1	0	0	4 (8blocks, protected block 24th-31th)
0	1	0	1	5 (16blocks, protected block 16th-31th)
0	1	1	0	6 (32blocks, protected all)
0	1	1	1	7 (32blocks, protected all)
1	0	0	0	8 (32blocks, protected all)
1	0	0	1	9 (32blocks, protected all)
1	0	1	0	10 (16blocks, protected block 0th-15th)
1	0	1	1	11 (24blocks, protected block 0th-23th)
1	1	0	0	12 (28blocks, protected block 0th-27th)
1	1	0	1	13 (30blocks, protected block 0th-29th)
1	1	1	0	14 (31blocks, protected block 0th-30th)
1	1	1	1	15 (32blocks, protected all)

II. Additional 512-bit secured OTP for unique identifier: to provide 512-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to *"Table 3. 512-bit Secured OTP Definition"*

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 512-bit secured OTP by entering 512-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 512-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "security register definition" for security register bit definition and table of "512-bit secured OTP definition" for address range definition.

- ***Note:*** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512-bit secured OTP mode, array access is not allowed.

Table 3. 512-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128-bit	ESN (electrical serial number)	Determined by customer
xxxx10~xxxx3F	384-bit	N/A	

7. MEMORY ORGANIZATION

Table 4. Memory Organization

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	:	:	:
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	:	:	:
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	:	:	:
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	:	:	:
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	:	:	:
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	:	:	:
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	:	:	:
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	:	:	:
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	:	:	:
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	:	:	:
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	:	:	:
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	:	:	:
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	:	:	:
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	:	:	:
	256	100000h	100FFFh
15	255	0FF000h	0FFFFFh
	:	:	:
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	:	:	:
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	:	:	:
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	:	:	:
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	:	:	:
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	:	:	:
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	:	:	:
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	:	:	:
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	:	:	:
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	:	:	:
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	:	:	:
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	:	:	:
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	:	:	:
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	:	:	:
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

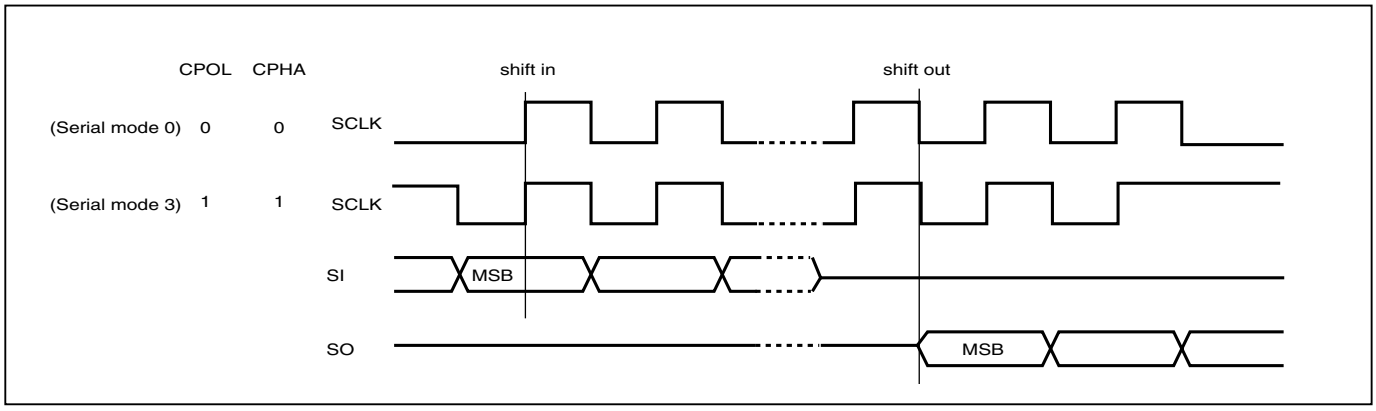
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported (for Normal Serial mode)"* .

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, DREAD, 4READ, QREAD, RES, REMS, REMS2, and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, 4PP, RDP, DP, ENSO, EXSO,and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



Note:
CPOL indicates clock polarity of Serial master,
-CPOL=1 for SCLK high while idle,
-CPOL=0 for SCLK low while not transmitting.
CPHA indicates clock phase.
The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

9. COMMAND DESCRIPTION

Table 5. Command Sets

Read Commands

Command (byte)	READ (read data)	FAST READ (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	4READ (4 x I/O read command)	QREAD (1I / 4O read command)
1st byte	03 (hex)	0B (hex)	5A (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	AD1 (A23-A16)	AD1	AD1	ADD	AD1	ADD & Dummy	AD1
3rd byte	AD2 (A15-A8)	AD2	AD2	ADD & Dummy	AD2	Dummy	AD2
4th byte	AD3 (A7-A0)	AD3	AD3		AD3		AD3
5th byte		Dummy	Dummy		Dummy		Dummy
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high		n bytes read out by 4 x I/O until CS# goes high	

Other Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identific-ation)	RDSR (read status register)	WRSR (write status register)	4PP (quad page program)	SE (sector erase)
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	38 (hex)	20 (hex)
2nd byte					Values	AD1	AD1
3rd byte							AD2
4th byte							AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufact-urer ID & 2-byte Device ID	to read out the values of the status register	to write new values of the status register	quad input to program the selected page	to erase the selected sector

Command (byte)	BE (block erase)	CE (chip erase)	PP (page program)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	Release Read Enhanced
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	AB (hex)	FFh (hex)
2nd byte	AD1		AD1			x	x
3rd byte	AD2		AD2			x	x
4th byte	AD3		AD3			x	x
Action	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	All these commands FFh, 00h, AAh or 55h will escape the performance enhance mode

Command (byte)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)
1st byte	90 (hex)	EF (hex)	DF (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte	x	X	x				
3rd byte	x	X	x				
4th byte	ADD (Note3)	ADD (Note3)	ADD (Note3)				
Action	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	to enter the 512-bit secured OTP mode	to exit the 512-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

Note 3: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 4: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

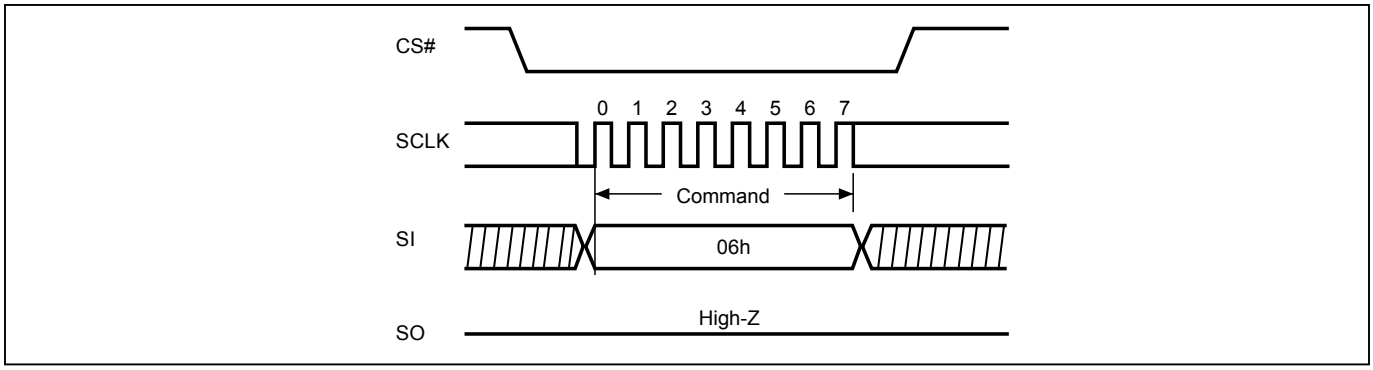
9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

The SIO[3:1] are don't care in this mode.

Figure 2. Write Enable (WREN) Sequence (Command 06)



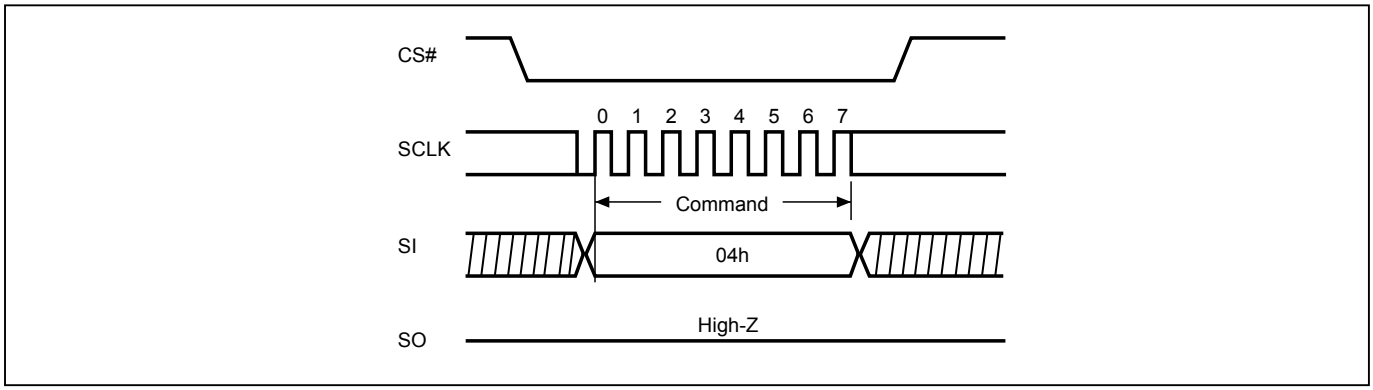
9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP, 4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

Figure 3. Write Disable (WRDI) Sequence (Command 04)



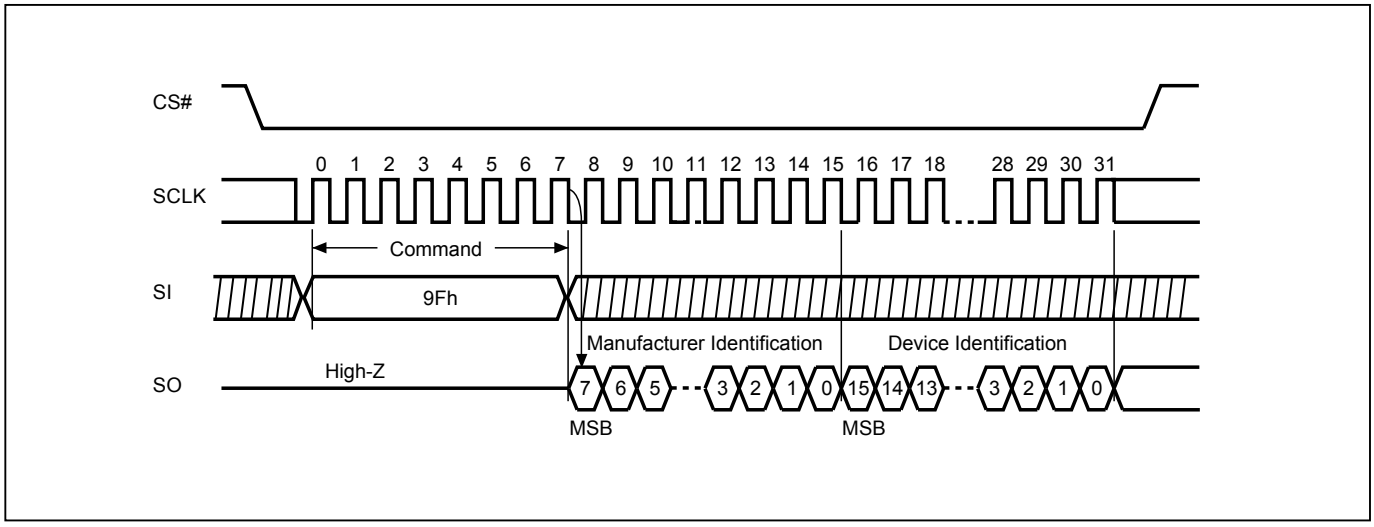
9-3. Read Identification (RDID)

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID is C2(hex), the memory type ID is as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of *"Table 7. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 4. Read Identification (RDID) Sequence (Command 9F)



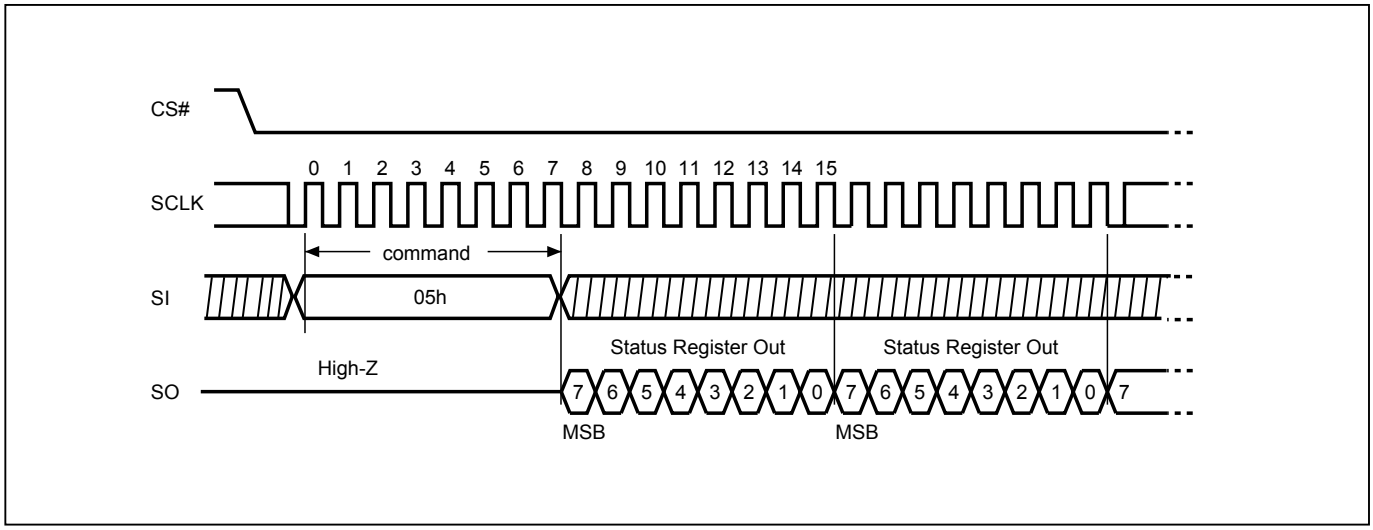
9-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

The SIO[3:1] are don't care when during this mode.

Figure 5. Read Status Register (RDSR) Sequence (Command 05)



The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, a non-volatile bit which is permanently set to "1". The flash always performs Quad I/O mode.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable 0=status register write enable	1=Quad Enable	(Note)	(Note)	(Note)	(Note)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

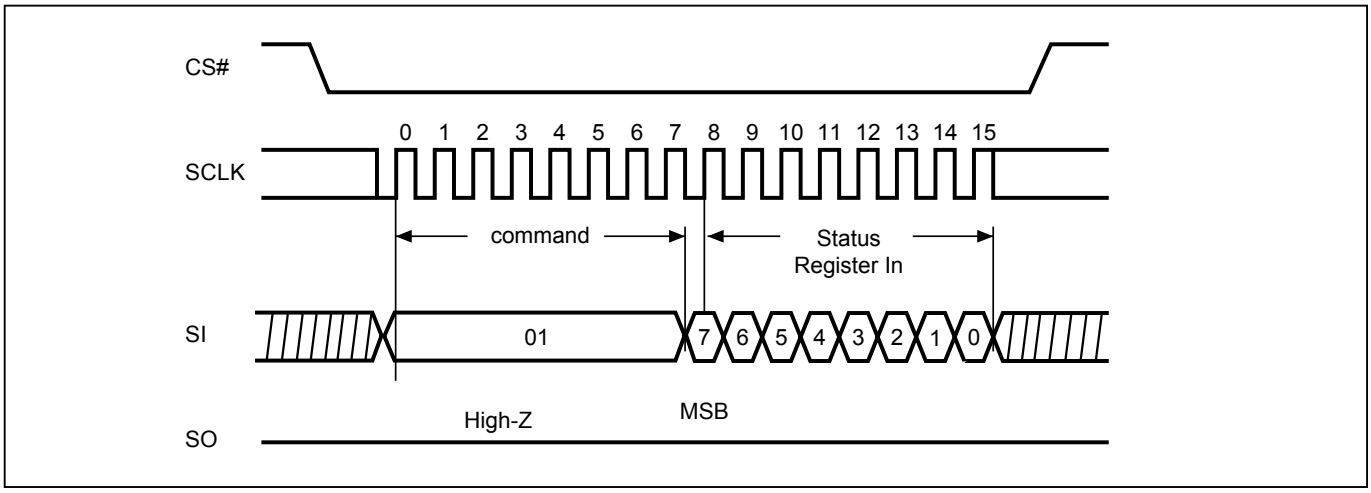
Note: See the *"Table 2. Protected Area Sizes"*.

9-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR can reset the Status Register Write Disable (SRWD) bit, but has no effect on bit1 (WEL) and bit0 (WIP) of the status register.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high.

Figure 6. Write Status Register (WRSR) Sequence (Command 01)



The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 6. Protection Modes

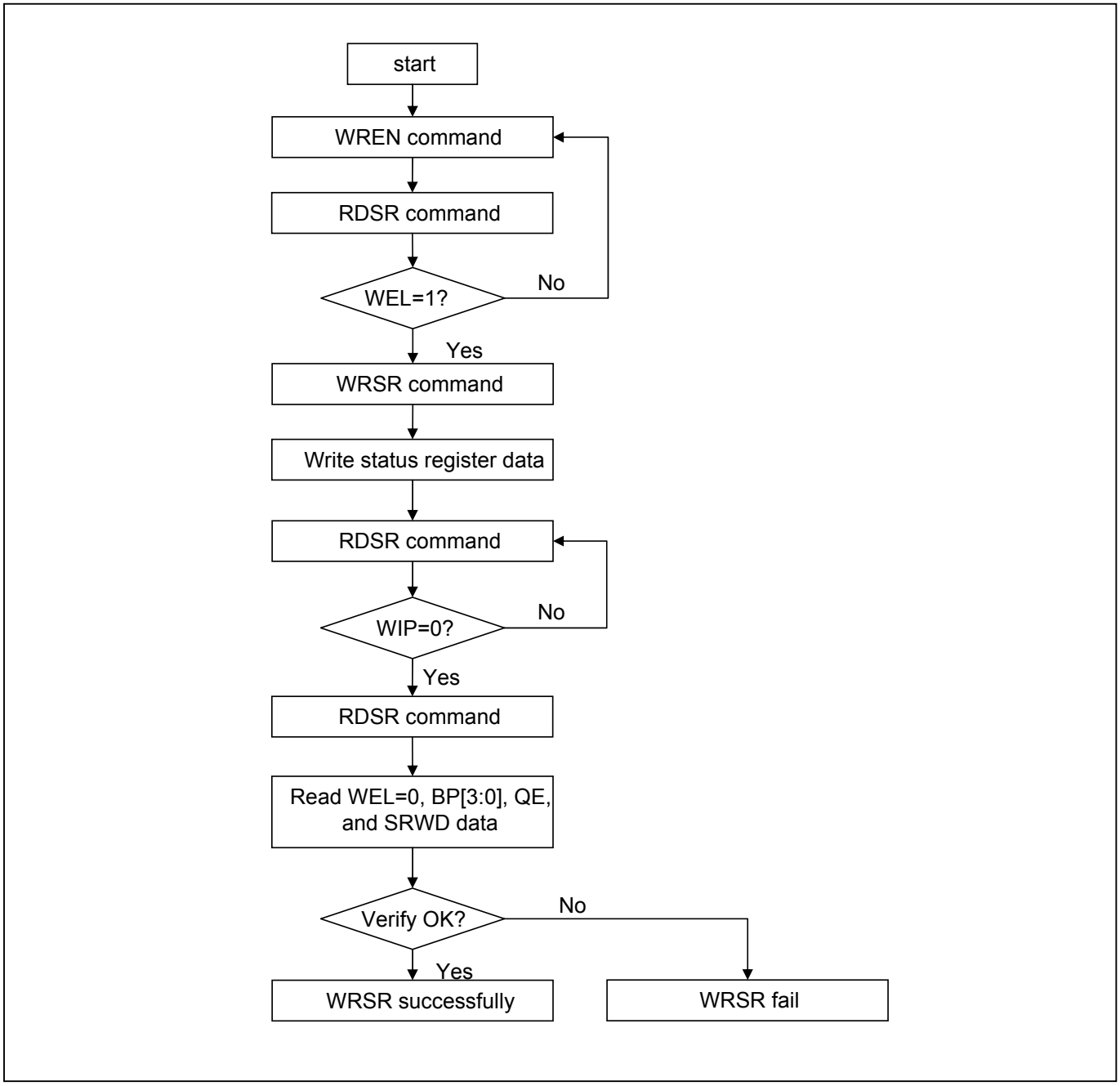
Mode	Status register condition	SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	SRWD bit=0	The protected area cannot be programmed or erased.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

Software Protected Mode (SPM):

- When SRWD bit=0, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).

Figure 7. WRSR flow

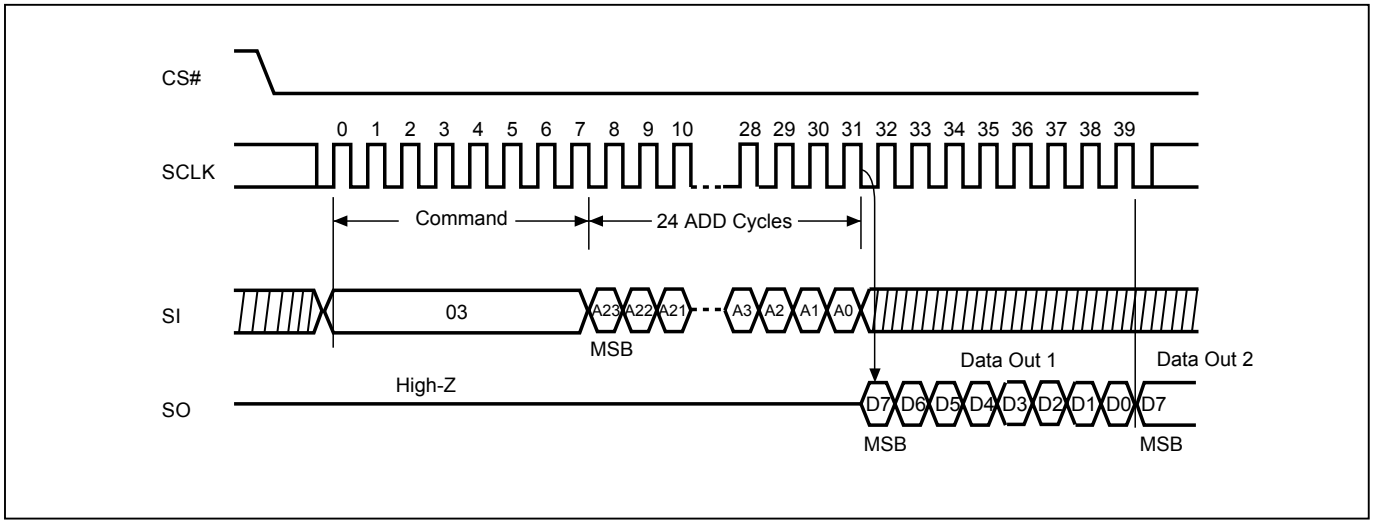


9-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→3-byte address on SI →data out on SO→ to end READ operation can use CS# to high at any time during data out.

Figure 8. Read Data Bytes (READ) Sequence (Command 03)



9-7. Read Data Bytes at Higher Speed (FAST_READ)

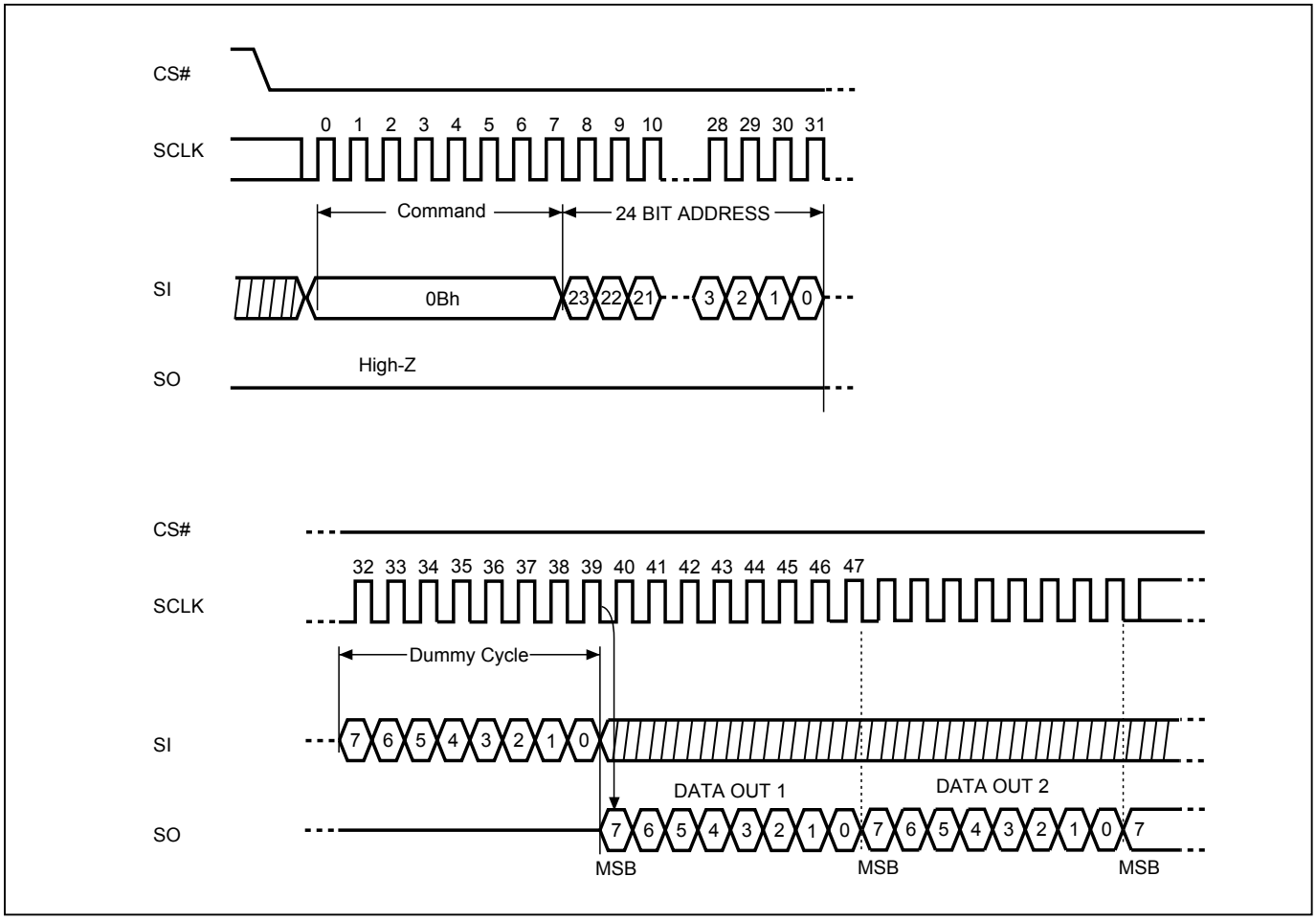
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 9. Read at Higher Speed (FAST_READ) Sequence (Command 0B) (104MHz)



9-8. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10. Dual Read Mode Sequence (Command 3B)