Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MX25L25635E

HIGH PERFORMANCE

SERIAL FLASH SPECIFICATION

Contents

256M-BIT [x 1/x 2/x 4] CMOS MXSMIO™ (SERIAL MULTI I/O) FLASH MEMORY

FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 268,435,456 x 1 bit structure or 134,217,728 x 2 bits (two I/O mode) structure or 67,108,864 x 4 bits (four I/O mode) structure
- 8192 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 1024 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 512 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  VCC = 2.7~3.6V
  - Normal read
    - 50MHz
  - Fast read
    - 1 I/O: 80MHz with 8 dummy cycles
    - 2 I/O: 70MHz with 4 dummy cycles
    - 4 I/O: 70MHz with 6 dummy cycles
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Continuously Program mode (automatically increase address under word program mode)
  - Fast erase time: 60ms (typ.)/sector (4K-byte per sector) ; 0.5s(typ.) /block (32K-byte per block); 0.7s(typ.) /block (64K-byte per block); 160s(typ.) /chip
- Low Power Consumption
  - Low active read current: 45mA(max.) at 80MHz, 40mA(max.) at 70MHz and 30mA(max.) at 50MHz
  - Low active programming current: 25mA (max.)
  - Low active erase current: 25mA (max.)
  - Standby current: 200uA (max.)
  - Deep power down current: 80uA (max.)
- Typical 100,000 erase/program cycles

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - BP0-BP3 block group protect
  - Flexible individual block protect when OTP WPSEL=1

- Additional 4K bits secured OTP for unique identifier

• Auto Erase and Auto Program Algorithms
- Automatically erases and verifies data at selected sector
- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programed should have page in the erased state first.)

• Status Register Feature

• Electronic Identification
- JEDEC 1-byte Manufacturer ID and 2-byte Device ID
- RES command for 1-byte Device ID
- Both REMS,REMS2, REMS4 commands for 1-byte Manufacturer ID and 1-byte Device ID

• Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

• SCLK Input
- Serial clock input

• SI/SIO0
- Serial Data Input or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode

• SO/SIO1
- Serial Data Output or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode

• WP#/SIO2
- Hardware write protection or serial data Input/Output for 4 x I/O mode

• HOLD#/SIO3
- HOLD# pin or serial data Input/Output for 4 x I/O mode, an internal weak pull up on the pin
- The weak pull up on the HOLD# pin will be disabled after QE bit is enabled, until next power-on cycle starts.
- HOLD# function is only available on 16 SOP package

• RESET#
- Hardware reset pin

• PACKAGE
- 16-pin SOP (300mil)
- 8 WSON (8x6mm)
- **All devices are RoHS Compliant**

GENERAL DESCRIPTION

MX25L25635E is 268,435,456 bits serial Flash memory, which is configured as 33,554,432 x 8 internally. When it is in two or four I/O mode, the structure becomes 134,217,728 bits x 2 or 67,108,864 bits x 4. The MX25L25635E features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L25635E, MXSMIO™ (Serial Multi I/O) flash memory, provides sequential read operation on whole chip and multi-I/O features.

When it is in dual I/O mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in quad I/O mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for Continuously Program mode, and erase command is executes on sector (4K-byte), block (32K-byte/64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 200uA DC current.

The MX25L25635E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

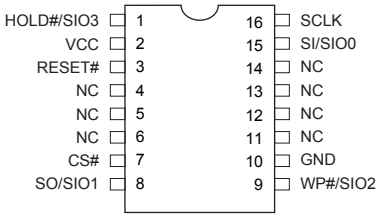
Table 1. Additional Features

Additional Features / Part Name	Protection and Security		Read Performance		
	Flexible or Individual block (or sector) protection	4K-bit secured OTP	1 I/O Read (80 MHz)	2 I/O Read (70 MHz)	4 I/O Read (70 MHz)
MX25L25635E	V	V	V	V	V

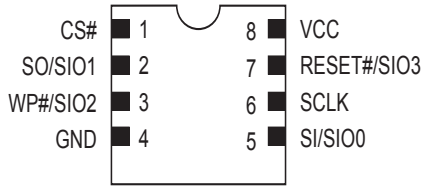
Additional Features / Part Name	Identifier				
	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	RDID (command: 9F hex)
MX25L25635E	18 (hex)	C2 18 (hex)	C2 18 (hex)	C2 18 (hex)	C2 20 19 (hex)

PIN CONFIGURATION

16-PIN SOP (300mil)



8-WSON (8x6mm) *

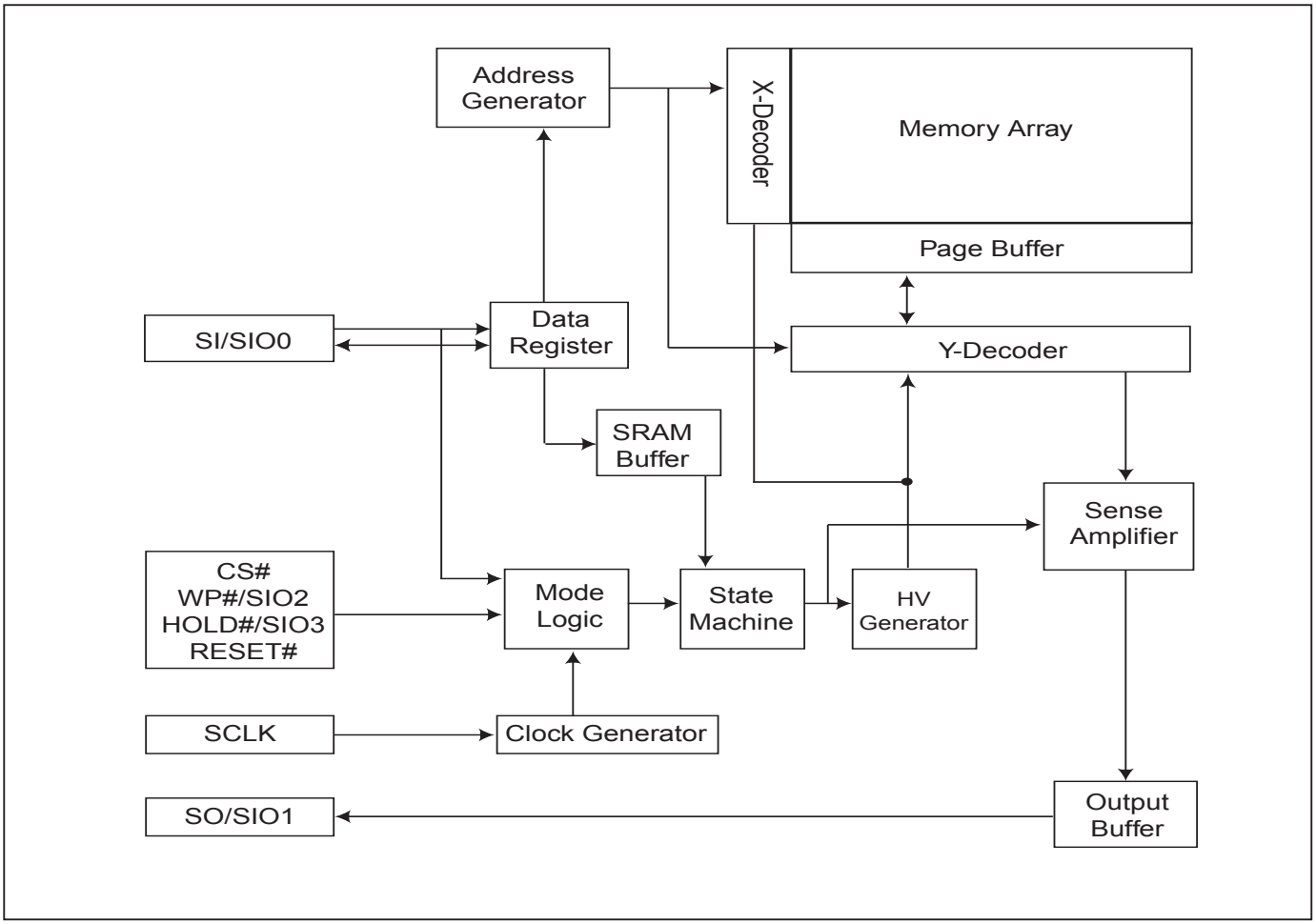


PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O mode)
HOLD#(1,2)/ SIO3	HOLD# pin or Serial Data Input & Output (for 4xI/O mode)
VCC	+ 3.3V Power Supply
GND	Ground
RESET#(3)	Hardware Reset Pin, Active low
NC	No Connection

Note:
(1). HOLD# function is only available on 16-SOP package.
(2). The weak pull up on the HOLD# pin will be disabled after QE bit is enabled, until next power-on cycle starts.
(3). RESET# pin has internal pull up.

BLOCK DIAGRAM



DATA PROTECTION

MX25L25635E is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the standby mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Reset# Pin driven low
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP, 4PP) command completion
  - Continuously Program mode (CP) instruction completion
  - Sector Erase (SE) command completion
  - Block Erase (BE, BE32K) command completion
  - Chip Erase (CE) command completion
  - Single Block Lock/Unlock (SBLK/SBULK) instruction completion
  - Gang Block Lock/Unlock (GBLK/GBULK) instruction completion
  - Write Security Register (WRSCUR) instruction completion
  - Write Protection Selection (WPSEL) instruction completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

I. Block lock protection

- The Software Protected Mode (SPM) uses (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits. Please refer to table of "Protected Area Sizes".

- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O mode, the feature of HPM will be disabled.

- MX25L25635E provide individual block (or sector) write protect & unprotect. User may enter the mode with WPSEL command and conduct individual block (or sector) write protect with SBLK instruction, or SBULK for individual block (or sector) unprotect. Under the mode, user may conduct whole chip (all blocks) protect with GBLK instruction and unlock the whole chip with GBULK instruction.

Table 2. Protected Area Sizes

Status bit				Protection Area
BP3	BP2	BP1	BP0	256Mb
0	0	0	0	0 (none)
0	0	0	1	1 (2 blocks, block 510th-511th)
0	0	1	0	2 (4 blocks, block 508th-511th)
0	0	1	1	3 (8 blocks, block 504th-511th)
0	1	0	0	4 (16 blocks, block 496th-511th)
0	1	0	1	5 (32 blocks, block 480th-511th)
0	1	1	0	6 (64 blocks, block 448nd-511th)
0	1	1	1	7 (128 blocks, block 384th-511th)
1	0	0	0	8 (256 blocks, block 256th-511th)
1	0	0	1	9 (512 blocks, all)
1	0	1	0	10 (512 blocks, all)
1	0	1	1	11 (512 blocks, all)
1	1	0	0	12 (512 blocks, all)
1	1	0	1	13 (512 blocks, all)
1	1	1	0	14 (512 blocks, all)
1	1	1	1	15 (512 blocks, all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. **Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker. Please refer to Table 3. 4K-bit Secured OTP Definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "Security Register Definition" for security register bit definition and table of "4K-bit Secured OTP Definition" for address range definition.
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

Memory Organization

Table 4. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
511	1023	8191	1FFF000h	1FFFFFFh
		⋮	⋮	⋮
		8184	1FF8000h	1FF8FFFh
	1022	8183	1FF7000h	1FF7FFFh
		⋮	⋮	⋮
		8176	1FF0000h	1FF0FFFh
510	1021	8175	1FEF000h	1FEFFFFh
		⋮	⋮	⋮
		8168	1FE8000h	1FE8FFFh
	1020	8167	1FE7000h	1FE7FFFh
		⋮	⋮	⋮
		8160	1FE0000h	1FE0FFFh
509	1019	8159	1FDF000h	1FDFFFFh
		⋮	⋮	⋮
		8152	1FD8000h	1FD8FFFh
	1018	8151	1FD7000h	1FD7FFFh
		⋮	⋮	⋮
		8144	1FD0000h	1FD0FFFh
2	5	47	002F000h	002FFFFh
		⋮	⋮	⋮
		40	0028000h	0028FFFh
	4	39	027000h	0027FFFh
		⋮	⋮	⋮
		32	0020000h	0020FFFh
1	3	31	001F000h	001FFFFh
		⋮	⋮	⋮
		24	0018000h	0018FFFh
	2	23	0017000h	0017FFFh
		⋮	⋮	⋮
		16	0010000h	0010FFFh
0	1	15	000F000h	000FFFFh
		⋮	⋮	⋮
		8	0008000h	0008FFFh
	0	7	0007000h	0007FFFh
		⋮	⋮	⋮
		0	0000000h	0000FFFh

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

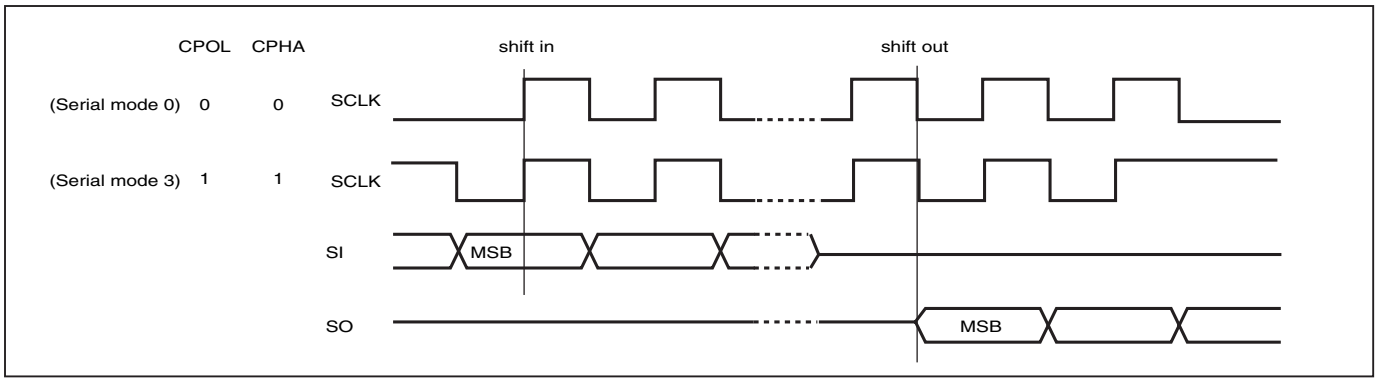
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as Figure 1.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, DREAD, 4READ, QREAD, RDBLOCK, RES, REMS, REMS2, and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, HPM, CE, PP, CP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK, ENSO, EXSO, WRSCUR, EN4B, EX4B, ENPLM, EXPLM, ESRY, DSRY and CLSR the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



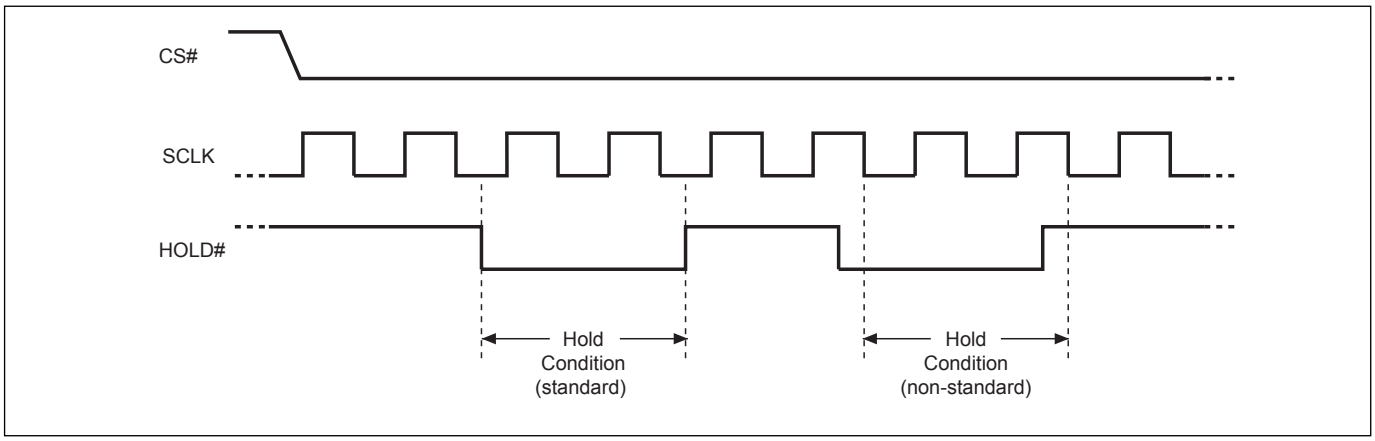
Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

HOLD FEATURES

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 2.

Figure 2. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note 1: The HOLD feature is disabled during Quad I/O mode in 16-SOP package.

COMMAND DESCRIPTION

Table 5. Command Sets

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	EN4B (enter 4-byte mode)	EX4B (exit 4-byte mode)	READ (read data)
Command (hex)	06	04	9F	05	01	B7	E9	03
Input Cycles					Data(8)			ADD(24)
Dummy Cycles								
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new values to the status register	to enter 4-byte mode and set 4BYTE bit as "1"	to exit 4-byte mode and clear 4BYTE bit to be "0"	n bytes read out until CS# goes high

COMMAND (byte)	FAST READ (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command) Note1	DREAD (1I 2O read)	4READ (4 x I/O read command)	QREAD (1I 4O read)	4PP (quad page program)	SE (sector erase)
Command (hex)	0B	5A	BB	3B	EB	6B	38	20
Input Cycles	ADD(24)	ADD(24)	ADD(12)	ADD(24)	ADD(6)+ indicator(2)	ADD(24)	ADD(6)+ Data(512)	ADD(24)
Dummy Cycles	8	8	4	8	4	8		
Action	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	n bytes read out by Quad output until CS# goes high	quad input to program the selected page	to erase the selected sector

COMMAND (byte)	BE (block erase 64KB)	BE 32K (block erase 32KB)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)
Command (hex)	D8	52	60 or C7	02	AD	B9	AB	AB
Input Cycles	ADD(24)	ADD(24)		ADD(24)+ Data(2048)	ADD(24)+ Data(16)			
Dummy Cycles								24
Action	to erase the selected 64KB block	to erase the selected 32KB block	to erase whole chip	to program the selected page	continously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID

COMMAND (byte)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)
Command (hex)	90	EF	DF	B1	C1	2B	2F
Input Cycles	ADD(8)	ADD(8)	ADD(8)				
Dummy Cycles	16	16	16				
Action	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufact-urer ID & device ID	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)

COMMAND (byte)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)	CLSR (Clear SR Fail Flags)	HPM (High Perform-ance Enable Mode)	WPSEL (write protection selection)	SBLK (single block lock) *Note 2	SBULK (single block unlock)
Command (hex)	70	80	30	A3	68	36	39
Input Cycles						ADD(24)	ADD(24)
Dummy Cycles							
Action	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode	clear security register bit 6 and bit 5	Quad I/O high Perform-ance mode	to enter and enable individal block protect mode	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect

COMMAND (byte)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)
Command (hex)	3C	7E	98
Input Cycles	ADD(24)		
Dummy Cycles			
Action	read individual block or sector write protect status	whole chip write protect	whole chip unprotect

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 2: In individual block write protection mode, all blocks/sectors is locked as defualt.
Note 3: The number in parentheses afer "ADD" or "Data" stands for how many clock cycles it has.
For example, "Data(8)" represents there are 8 clock cycles for the data in. Please note the number after "ADD" are based on 3-byte address mode, for 4-byte address mode, which will be increased.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE, BE32K, CE, WRSR, WRSCUR, WPSEL, SBLK, SBULK, GBLK and GBULK, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (Please refer to Figure 10)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (Please refer to Figure 11)

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP, 4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE, BE32K) instruction completion
- Chip Erase (CE) instruction completion
- Continuously Program mode (CP) instruction completion
- Single Block Lock/Unlock (SBLK/SBULK) instruction completion
- Gang Block Lock/Unlock (GBLK/GBULK) instruction completion
- Write Security Register (WRSCUR) instruction completion
- Write Protection Selection (WPSEL) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of "ID Definitions". (Please refer to Table 6)

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (Please refer to Figure 12)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO (Please refer to Figure 13).

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in Table 2) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD#, RESET# are enable. While QE is "1", it performs Quad I/O mode and WP#, HOLD#, RESET# are disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM and HOLD (16SOP package) or RESET (8 WSON package) will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1= Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the Table 2 "Protected Area Size" in page 11.

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in Table 2). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

If Reset# goes low while Write Status Register (WRSR) execution is on going, the operation of WRSR will finish after tw timing before entering Reset mode.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (Please refer to Figure 14)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 2.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.
If the system goes into four I/O mode, the feature of HPM will be disabled.

(6) Enter 4-byte mode (EN4B)

The EN4B instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit2 (4BTYE bit) of security register will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. There are three methods to exit the 4-byte mode: writing exit 4-byte mode (EX4B) instruction, Hardware Reset or power-off.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending EN4B instruction to enter 4-byte mode(automatically set 4BYTE bit as "1") → CS# goes high.

(7) Exit 4-byte mode (EX4B)

The EX4B instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the EX4B instruction, the bit2 (4BTYE bit) of security register will be cleared to be "1" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing EX4B instruction is: CS# goes low → sending EX4B instruction to exit 4-byte mode (automatically clear the 4BYTE bit to be "0") → CS# goes high.

(8) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing READ instruction is: CS# goes low → sending READ instruction code→ 3-byte or 4-byte address (depending on mode state) on SI → data out on SO → to end READ operation can use CS# to high at any time during data out. (Please refer to Figure 15)

(9) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing FAST_READ instruction is: CS# goes low → sending FAST_READ instruction code → 3-byte or 4-byte address (depending on mode state) on SI → 1-dummy byte (default) address on SI → data out on

SO → to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to Figure 16)
While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) 2 x I/O Read Mode (2READ)

The 2READ instruction enables Double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing 2READ instruction is: CS# goes low → sending 2READ instruction → 3-byte or 4-byte address (depending on mode state) interleave on SIO1 & SIO0 → 4-bit dummy cycle on SIO1 & SIO0 → data out interleave on SIO1 & SIO0 → to end 2READ operation can use CS# to high at any time during data out (Please refer to Figure 17 for 2 x I/O Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(11) Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte or 4-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out (Please refer to Figure 18 for Dual Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(12) 4 x I/O Read Mode (4READ)

The 4READ instruction enables quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing 4READ instruction is: CS# goes low → sending 4READ instruction → 3-byte or 4-byte address (depending on mode state) interleave on SIO3, SIO2, SIO1 & SIO0 → 6 dummy cycles → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out (Please refer to Figure 19 for 4 x I/O Read Mode Timing Waveform).

Another sequence of issuing 4 READ instruction especially useful in random access is : CS# goes low→ sending 4 READ instruction → 3-byte or 4-byte address (depending on mode state) interleave on SIO3, SIO2, SIO1 & SIO0 → performance enhance toggling bit P[7:0]→ 4 dummy cycles → data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 3-byte or 4-byte address (depending on mode state) random access address (Please refer to Figure 21 for 4x I/O Read Enhance Performance Mode timing waveform).

In the performance-enhancing mode (the waveform figure), P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h. These commands will reset the performance enhance mode. And afterwards CS# is raised and then lowered, the system then will return to normal operation.
While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(13) Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status register must be set to "1" before sending the QREAD. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte or 4-byte address on SI → 8-bit dummy cycle → data out interleave on SO3, SO2, SO1 & SO0→ to end QREAD operation can use CS# to high at any time during data out (Please refer to Figure 20 for Quad Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(14) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Table of memory organization) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode.

If RESET# goes low while Sector Erase (SE) execution is on going, the operation of SE will finish after tSE timing before entering Reset mode.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte or 4-byte address (depending on mode state) on SI → CS# goes high. (Please refer to Figure 22)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(15) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Table of memory organization) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte or 4-byte address (depending on mode state) on SI → CS# goes high. (Please refer to Figure 23)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(16) Block Erase (BE32K)

The Block Erase (BE32) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32). Any address of the block (Table of memory organization) is a valid address for Block Erase (BE32) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode.

If RESET# goes low while Block Erase (BE32K) execution is on going, the operation of BE32K will finish after tBE (32KB) timing before entering Reset mode.

The sequence of issuing BE32 instruction is: CS# goes low → sending BE32 instruction code → 3-byte or 4-byte address (depending on mode state) on SI → CS# goes high. (Please refer to Figure 23)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(17) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high. (Please refer to Figure 24)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected the Chip Erase (CE) instruction will not be executed, but WEL will be reset.

(18) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte or 4-byte address (depending on mode state) on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to Figure 25)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise, the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

(19) 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3, which can raise programer performance and and the effectiveness of application of lower clock less than 20MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because

the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 20MHz below. The other function descriptions are as same as standard page program.

The default mode is 3-byte address, to access higher address(4-byte address) which requires to enter the 4-byte address read mode.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte or 4-byte address (depending on mode state) on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high. (Please refer to Figure 26)

If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.