



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MACRONIX
INTERNATIONAL Co., LTD.

MX25L25635F

MX25L25635F

DATASHEET

Contents

| | |
|--|-----------|
| 1. FEATURES | 4 |
| 2. GENERAL DESCRIPTION | 6 |
| Table 1. Read performance Comparison | 6 |
| 3. PIN CONFIGURATIONS | 7 |
| 4. PIN DESCRIPTION | 7 |
| 5. BLOCK DIAGRAM | 8 |
| 6. DATA PROTECTION | 9 |
| Table 2. Protected Area Sizes | 10 |
| Table 3. 4K-bit Secured OTP Definition | 11 |
| 7. Memory Organization | 12 |
| Table 4. Memory Organization | 12 |
| 8. DEVICE OPERATION | 13 |
| 8-1. 256Mb Address Protocol..... | 15 |
| 8-2. Quad Peripheral Interface (QPI) Read Mode | 16 |
| 9. COMMAND DESCRIPTION | 17 |
| Table 5. Command Set..... | 17 |
| 9-1. Write Enable (WREN)..... | 22 |
| 9-2. Write Disable (WRDI)..... | 23 |
| 9-3. Read Identification (RDID)..... | 24 |
| 9-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES) | 25 |
| 9-5. Read Electronic Manufacturer ID & Device ID (REMS)..... | 27 |
| 9-6. QPI ID Read (QPIID) | 28 |
| Table 6. ID Definitions | 28 |
| 9-7. Read Status Register (RDSR)..... | 29 |
| 9-8. Read Configuration Register (RDCR)..... | 30 |
| Table 7. Configuration Register | 34 |
| 9-9. Write Status Register (WRSR)..... | 36 |
| Table 8. Protection Modes..... | 37 |
| 9-10. Enter 4-byte mode (EN4B) | 40 |
| 9-11. Exit 4-byte mode (EX4B) | 40 |
| 9-12. Read Data Bytes (READ) | 41 |
| 9-13. Read Data Bytes at Higher Speed (FAST_READ) | 42 |
| 9-14. Dual Output Read Mode (DREAD) | 44 |
| 9-15. 2 x I/O Read Mode (2READ) | 45 |
| 9-16. Quad Read Mode (QREAD) | 46 |
| 9-17. 4 x I/O Read Mode (4READ) | 47 |
| 9-18. 4 Byte Address Command Set..... | 49 |
| 9-19. Burst Read..... | 51 |
| 9-20. Performance Enhance Mode | 52 |
| 9-21. Performance Enhance Mode Reset..... | 55 |
| 9-22. Fast Boot | 57 |
| 9-23. Sector Erase (SE)..... | 60 |
| 9-24. Block Erase (BE32K)..... | 61 |
| 9-25. Block Erase (BE) | 62 |
| 9-26. Chip Erase (CE)..... | 63 |



| | |
|---|------------|
| 9-27. Page Program (PP) | 64 |
| 9-28. 4 x I/O Page Program (4PP)..... | 66 |
| 9-29. Deep Power-down (DP)..... | 67 |
| 9-30. Enter Secured OTP (ENSO)..... | 68 |
| 9-31. Exit Secured OTP (EXSO)..... | 68 |
| 9-32. Read Security Register (RDSCUR)..... | 68 |
| 9-33. Write Security Register (WRSCUR)..... | 68 |
| Table 9. Security Register Definition | 69 |
| 9-34. Write Protection Selection (WPSEL)..... | 70 |
| 9-35. Advanced Sector Protection | 72 |
| 9-35-1. Lock Register | 73 |
| 9-35-2.SPB Lock Bit (SPBLB) | 74 |
| 9-35-3.Solid Protection Bits | 75 |
| 9-35-4.Dynamic Write Protection Bits..... | 77 |
| 9-35-5.Temporary Un-protect Solid write protect bit (USPB) | 78 |
| 9-35-6.Gang Block Lock/Unlock (GBLK/GBULK)..... | 78 |
| 9-35-7.Sector Protection States Summary Table..... | 78 |
| 9-35-8.Password Protection Mode | 79 |
| 9-36. Program/Erase Suspend/Resume | 80 |
| 9-37. Erase Suspend | 80 |
| 9-38. Program Suspend..... | 80 |
| 9-39. Write-Resume | 82 |
| 9-40. No Operation (NOP) | 82 |
| 9-41. Software Reset (Reset-Enable (RSTEN) and Reset (RST)) | 82 |
| 9-42. Read SFDP Mode (RDSFDP)..... | 84 |
| Table 10. Signature and Parameter Identification Data Values | 85 |
| Table 11. Parameter Table (0): JEDEC Flash Parameter Tables | 86 |
| Table 12. Parameter Table (1): Macronix Flash Parameter Tables | 88 |
| 10. RESET..... | 90 |
| Table 13. Reset Timing-(Power On)..... | 90 |
| Table 14. Reset Timing-(Other Operation) | 90 |
| 11. POWER-ON STATE | 91 |
| 12. ELECTRICAL SPECIFICATIONS | 92 |
| Table 16. ABSOLUTE MAXIMUM RATINGS | 92 |
| Table 17. CAPACITANCE TA = 25°C, f = 1.0 MHz..... | 92 |
| Table 18. DC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V) | 94 |
| Table 19. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V) | 95 |
| 13. OPERATING CONDITIONS..... | 96 |
| Table 20. Power-Up/Down Voltage and Timing | 98 |
| 13-1. INITIAL DELIVERY STATE | 98 |
| 14. ERASE AND PROGRAMMING PERFORMANCE | 99 |
| 15. DATA RETENTION | 99 |
| 16. LATCH-UP CHARACTERISTICS | 99 |
| 17. ORDERING INFORMATION | 100 |
| 18. PART NAME DESCRIPTION..... | 101 |
| 19. PACKAGE INFORMATION..... | 102 |
| 20. REVISION HISTORY | 104 |



3V 256M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- 256Mb: 268,435,456 x 1 bit structure or 134,217,728 x 2 bits (two I/O mode) structure or 67,108,864 x 4 bits (four I/O mode) structure
- Protocol Support
 - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 2.3V to 2.5V
- Fast read for SPI mode
 - Support clock frequency up to 133MHz for all protocols
 - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions.
 - Configurable dummy cycle number for fast read operation
- Quad Peripheral Interface (QPI) available
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
 - Any Block can be erased individually
- Programming :
 - 256byte page buffer
 - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
 - Advanced sector protection function (Solid and Password Protect)
- Additional 4K bit security OTP
 - Features unique identifier
 - factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID
 - RES command for 1-byte Device ID
 - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode



HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SIO0
 - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
 - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
 - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- RESET#/SIO3
 - Hardware Reset pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
 - 16-pin SOP (300mil)
 - 8-land WSON (8x6mm)
 - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L25635F is 256Mb bits serial Flash memory, which is configured as 33,554,432 x 8 internally. When it is in two or four I/O mode, the structure becomes 134,217,728 bits x 2 or 67,108,864 bits x 4. MX25L25635F feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# and RESET# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25L25635F MXSMIO[®] (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25L25635F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

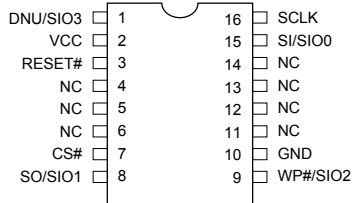
Table 1. Read performance Comparison

| Numbers of Dummy Cycles | Fast Read (MHz) | Dual Output Fast Read (MHz) | Quad Output Fast Read (MHz) | Dual IO Fast Read (MHz) | Quad IO Fast Read (MHz) |
|-------------------------|-----------------|-----------------------------|-----------------------------|-------------------------|-------------------------|
| 4 | - | - | - | 84* | 70 |
| 6 | 104 | 104 | 84 | 104 | 84* |
| 8 | 104* | 104* | 104* | 104 | 104 |
| 10 | 133 | 133 | 133 | 133 | 133 |

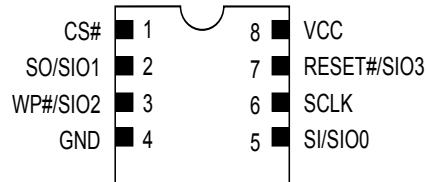
Note: * mean default status

3. PIN CONFIGURATIONS

16-PIN SOP (300mil)



8-WSON (8x6mm)

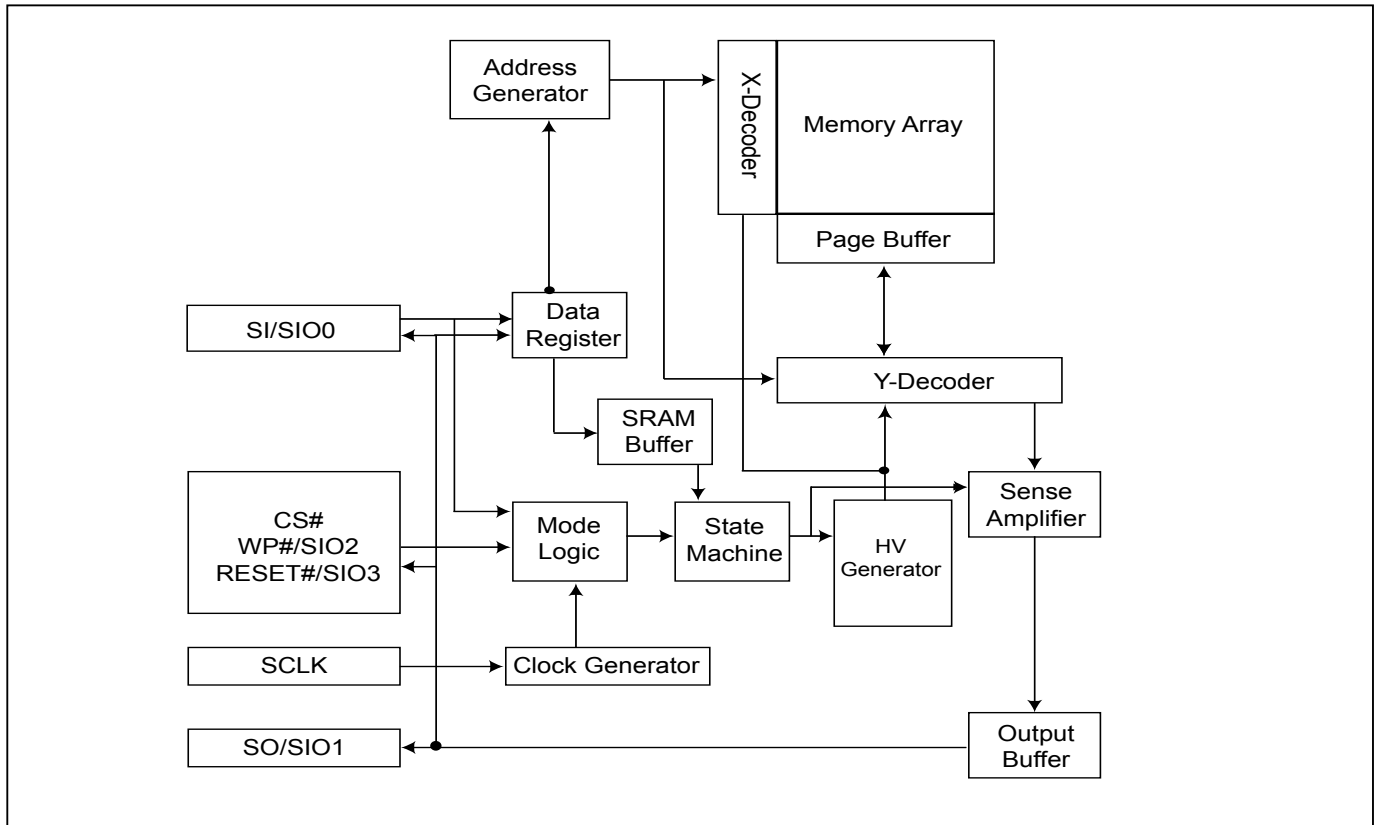


4. PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-------------|---|
| CS# | Chip Select |
| SI/SIO0 | Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SO/SIO1 | Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SCLK | Clock Input |
| WP#/SIO2 | Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode) |
| RESET#/SIO3 | Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode) |
| DNU/SIO3 | Do not use or Serial Data Input & Output (for 4xI/O read mode) |
| RESET#* | Hardware Reset Pin Active low |
| VCC | + 3V Power Supply |
| GND | Ground |
| NC | No Connection |

Notes:

1. RESET# pin has internal pull up.
2. When using 1I/O or 2I/O (QE bit not enable), the DNU/SIO3 pin of 16SOP can not connect to GND. Recommend to connect this pin to VCC or floating.

5. BLOCK DIAGRAM

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as [Table 2](#) Protected Area Sizes, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.



Table 2. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

| Status bit | | | | Protect Level |
|------------|-----|-----|-----|---|
| BP3 | BP2 | BP1 | BP0 | 256Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1 block, protected block 511st) |
| 0 | 0 | 1 | 0 | 2 (2 blocks, protected block 510th~511st) |
| 0 | 0 | 1 | 1 | 3 (4 blocks, protected block 508th~511st) |
| 0 | 1 | 0 | 0 | 4 (8 blocks, protected block 504th~511st) |
| 0 | 1 | 0 | 1 | 5 (16 blocks, protected block 496th~511st) |
| 0 | 1 | 1 | 0 | 6 (32 blocks, protected block 480th~511st) |
| 0 | 1 | 1 | 1 | 7 (64 blocks, protected block 448th~511st) |
| 1 | 0 | 0 | 0 | 8 (128 blocks, protected block 384th~511st) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, protected block 256th~511st) |
| 1 | 0 | 1 | 0 | 10 (512 blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (512 blocks, protected all) |
| 1 | 1 | 0 | 0 | 12 (512 blocks, protected all) |
| 1 | 1 | 0 | 1 | 13 (512 blocks, protected all) |
| 1 | 1 | 1 | 0 | 14 (512 blocks, protected all) |
| 1 | 1 | 1 | 1 | 15 (512 blocks, protected all) |

Protected Area Sizes (T/B bit = 1)

| Status bit | | | | Protect Level |
|------------|-----|-----|-----|---|
| BP3 | BP2 | BP1 | BP0 | 256Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1 block, protected block 0th) |
| 0 | 0 | 1 | 0 | 2 (2 blocks, protected block 0th~1th) |
| 0 | 0 | 1 | 1 | 3 (4 blocks, protected block 0th~3rd) |
| 0 | 1 | 0 | 0 | 4 (8 blocks, protected block 0th~7th) |
| 0 | 1 | 0 | 1 | 5 (16 blocks, protected block 0th~15th) |
| 0 | 1 | 1 | 0 | 6 (32 blocks, protected block 0th~31st) |
| 0 | 1 | 1 | 1 | 7 (64 blocks, protected block 0th~63rd) |
| 1 | 0 | 0 | 0 | 8 (128 blocks, protected block 0th~127th) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, protected block 0th~255th) |
| 1 | 0 | 1 | 0 | 10 (512 blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (512 blocks, protected all) |
| 1 | 1 | 0 | 0 | 12 (512 blocks, protected all) |
| 1 | 1 | 0 | 1 | 13 (512 blocks, protected all) |
| 1 | 1 | 1 | 0 | 14 (512 blocks, protected all) |
| 1 | 1 | 1 | 1 | 15 (512 blocks, protected all) |

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to "[Table 9. Security Register Definition](#)" for security register bit definition and "[Table 3. 4K-bit Secured OTP Definition](#)" for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

| Address range | Size | Standard Factory Lock | Customer Lock |
|---------------|----------|--------------------------------|------------------------|
| xxx000~xxx00F | 128-bit | ESN (electrical serial number) | Determined by customer |
| xxx010~xxx1FF | 3968-bit | N/A | |

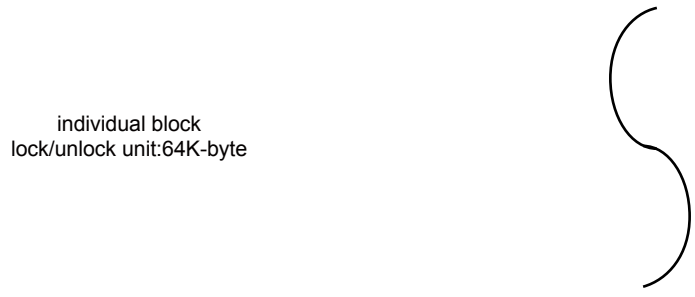
7. Memory Organization

Table 4. Memory Organization

| Block(64K-byte) | Block(32K-byte) | Sector | Address Range | |
|-----------------|-----------------|--------|---------------|----------|
| 511 | 1023 | 8191 | 1FFF000h | 1FFFFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8184 | 1FF8000h | 1FF8FFFh |
| | 1022 | 8183 | 1FF7000h | 1FF7FFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8176 | 1FF0000h | 1FF0FFFh |
| 510 | 1021 | 8175 | 1FEF000h | 1FEFFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8168 | 1FE8000h | 1FE8FFFh |
| | 1020 | 8167 | 1FE7000h | 1FE7FFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8160 | 1FE0000h | 1FE0FFFh |
| 509 | 1019 | 8159 | 1FDF000h | 1FDFFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8152 | 1FD8000h | 1FD8FFFh |
| | 1018 | 8151 | 1FD7000h | 1FD7FFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8144 | 1FD0000h | 1FD0FFFh |

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte



| | | | | |
|---|---|----|----------|----------|
| 2 | 5 | 47 | 002F000h | 002FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 40 | 0028000h | 0028FFFh |
| | 4 | 39 | 027000h | 0027FFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 32 | 0020000h | 0020FFFh |
| 1 | 3 | 31 | 001F000h | 001FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 24 | 0018000h | 0018FFFh |
| | 2 | 23 | 0017000h | 0017FFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 16 | 0010000h | 0010FFFh |
| 0 | 1 | 15 | 000F000h | 000FFFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 8 | 0008000h | 0008FFFh |
| | 0 | 7 | 0007000h | 0007FFFh |
| | | ⋮ | ⋮ | ⋮ |
| | | 0 | 0000000h | 0000FFFh |

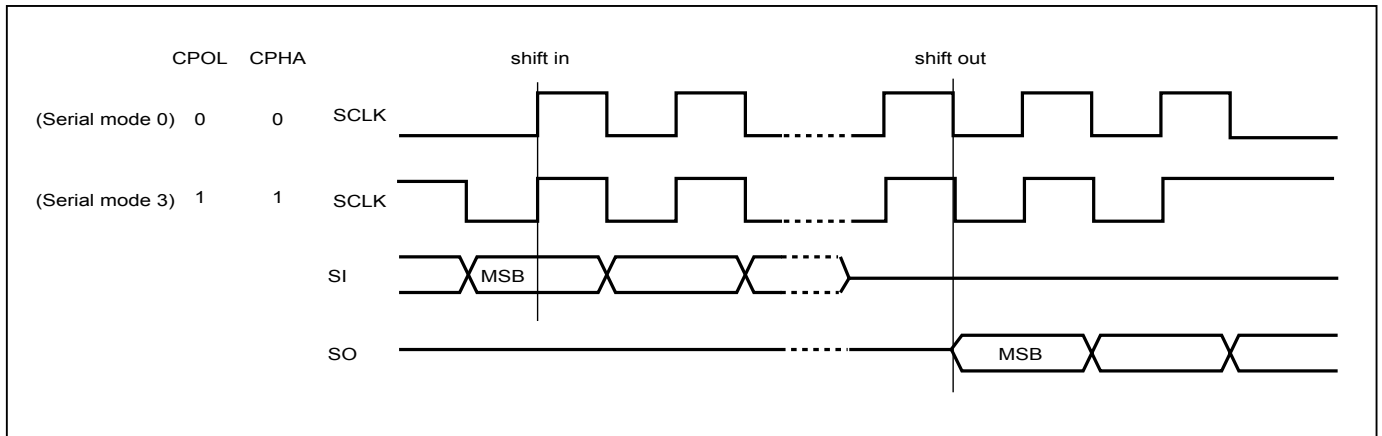
individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Serial Modes Supported".
5. For the following instructions: RDID, RDSR, RDSCUR, READ/READ4B, FAST_READ/FAST_READ4B, 2READ/2READ4B, DREAD/DREAD4B, 4READ/4READ4B, QREAD/QREAD4B, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDPASS, RDLR, RDEAR, RDFBR, RDSPBLK, RDCR, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, PP/PP4B, 4PP/4PP4B, DP, ENSO, EXSO, WRSCUR, EN4B, EX4B, WPSEL, GBLK, GBULK, SPBLK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

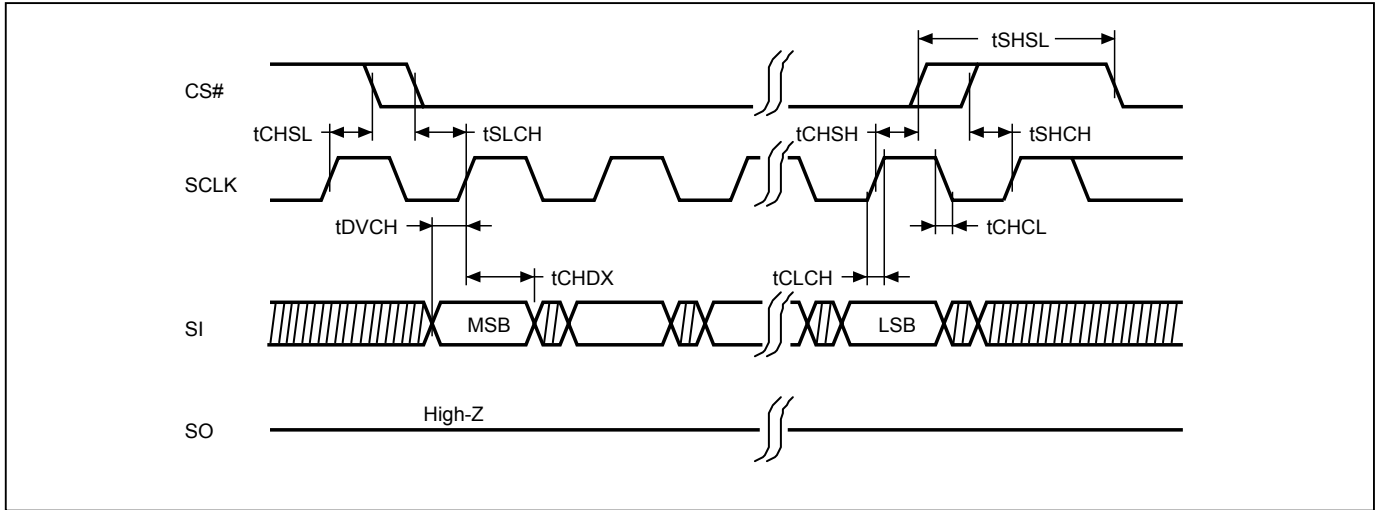
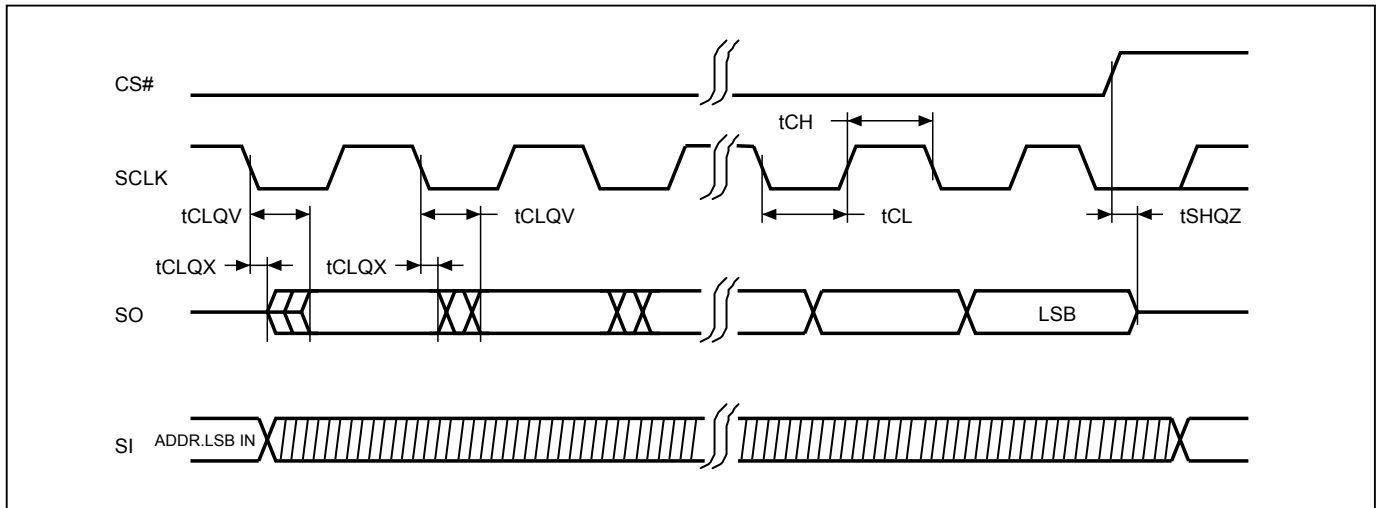


Figure 3. Output Timing



8-1. 256Mb Address Protocol

The original 24 bit address protocol of serial Flash can only access density size below 128Mb. For the memory device of 256Mb and above, the 32bit address is requested for access higher memory size. The MX25L25635F provides three different methods to access the whole 256Mb density:

(1)Command entry 4-byte address mode: Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register bit. After 4BYTE bit has been set, the number of address cycle become 32-bit.

(2)Extended Address Register (EAR): configure the memory device into two 128Mb segments to select which one is active through the EAR bit "0".

(3)4-byte Address Command Set: When issuing 4-byte address command set, 4-byte address (A31-A0) is requested after the instruction code. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Enter 4-Byte Address Mode

In 4-byte Address mode, all instructions are 32-bits address clock cycles. By using EN4B and EX4B to enable and disable the 4-byte address mode.

When 4-byte address mode is enabled, the EAR<0> becomes "don't care" for all instructions requiring 4-byte address. The EAR function will be disabled when 4-byte mode is enabled.

Extended Address Register (Configurable)

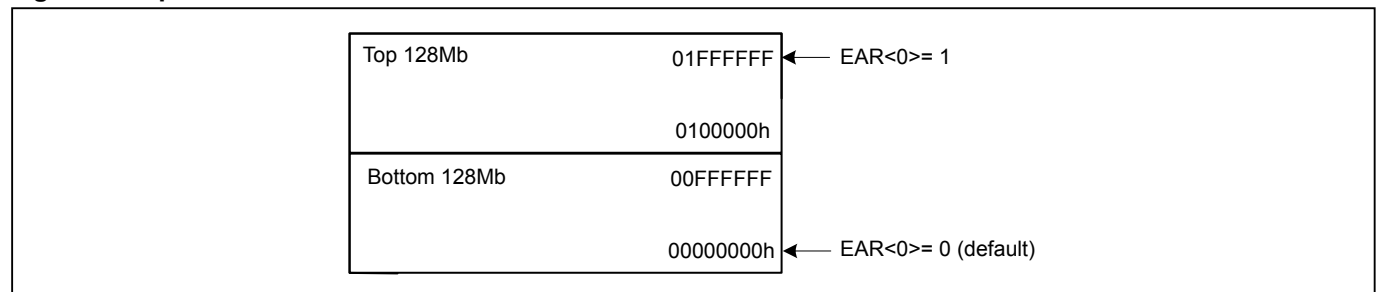
The device provides an 8-bit volatile register for extended Address Register: it identifies the extended address (A31~A24) above 128Mb density by using original 3-byte address.

Extended Address Register (EAR)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| A31 | A30 | A29 | A28 | A27 | A26 | A25 | A24 |

For the MX25L25635F the A31 to A25 are Don't Care. During EAR, reading these bits will read as 0. The bit 0 is default as "0".

Figure 4. Top and Bottom 128M bits



When under EAR mode, Read, Program, Erase operates in the selected segment by using 3-byte address mode.

For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected top or bottom 128Mb, but it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment.

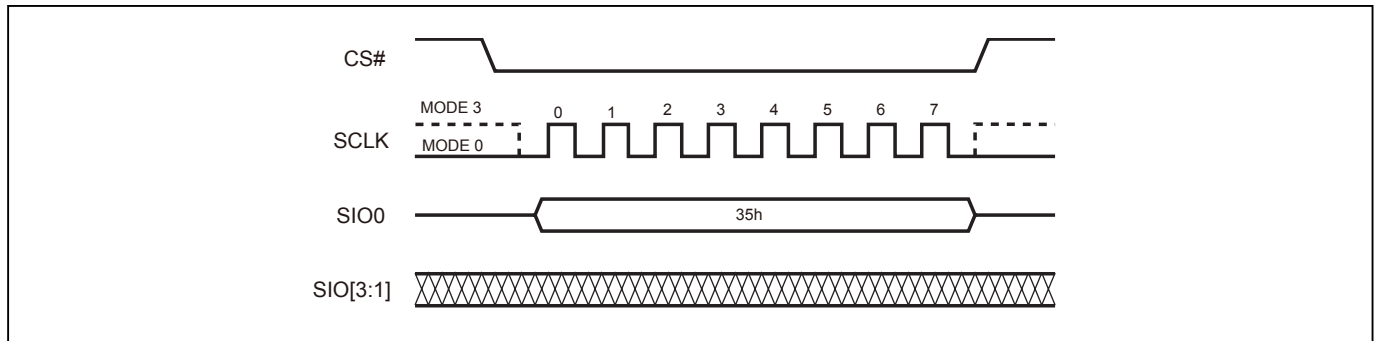
8-2. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enabled. After QPI mode is enabled, the device enters quad mode (4-4-4) without QE bit status changed.

Figure 5. Enable QPI Sequence



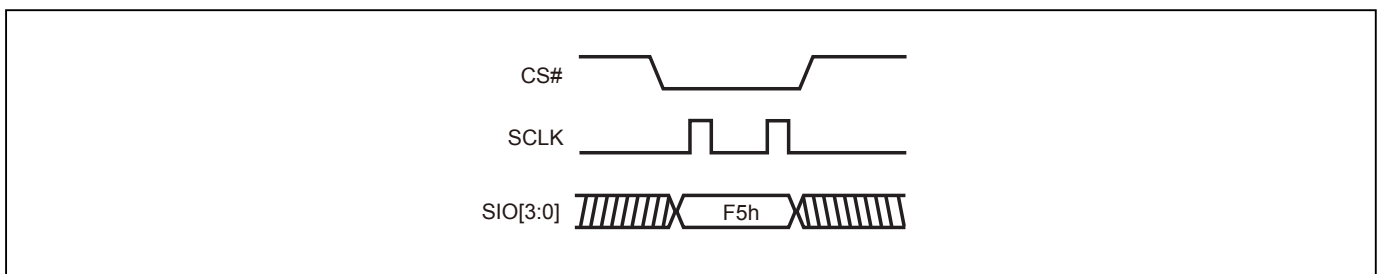
Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5H) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:

For EQIO and RSTQIO commands, CS# high width has to follow "write spec" tSHSL for next instruction.

Figure 6. Reset QPI Mode



9. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

| Command (byte) | READ (normal read) | FAST READ (fast read data) | 2READ (2 x I/O read command) | DREAD (1I 2O read) | 4READ (4 I/O read start from bottom 128Mb) | 4READ (4 I/O read start from Top 128Mb) | QREAD (1I 4O read) |
|----------------|--------------------------------------|--------------------------------------|---|---|--|---|---|
| Mode | SPI | SPI | SPI | SPI | SPI/QPI | SPI/QPI | SPI |
| Address Bytes | 3/4 | 3/4 | 3/4 | 3/4 | 3/4 | 3/4 | 3/4 |
| 1st byte | 03 (hex) | 0B (hex) | BB (hex) | 3B (hex) | EB (hex) | EA (hex) | 6B (hex) |
| 2nd byte | ADD1 | ADD1 | ADD1 | ADD1 | ADD1 | ADD1 | ADD1 |
| 3rd byte | ADD2 | ADD2 | ADD2 | ADD2 | ADD2 | ADD2 | ADD2 |
| 4th byte | ADD3 | ADD3 | ADD3 | ADD3 | ADD3 | ADD3 | ADD3 |
| 5th byte | | Dummy* | Dummy* | Dummy* | Dummy* | Dummy* | Dummy* |
| Data Cycles | | | | | | | |
| Action | n bytes read out until CS# goes high | n bytes read out until CS# goes high | n bytes read out by 2 x I/O until CS# goes high | n bytes read out by Dual output until CS# goes high | Quad I/O read for bottom 128Mb with 6 dummy cycles | Quad I/O read for Top 128Mb with 6 dummy cycles | n bytes read out by Quad output until CS# goes high |

| Command (byte) | PP (page program) | 4PP (quad page program) | SE (sector erase) | BE 32K (block erase 32KB) | BE (block erase 64KB) | CE (chip erase) |
|----------------|------------------------------|---|------------------------------|---------------------------------|-----------------------------|---------------------|
| Mode | SPI/QPI | SPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| Address Bytes | 3/4 | 3/4 | 3/4 | 3/4 | 3/4 | 0 |
| 1st byte | 02 (hex) | 38 (hex) | 20 (hex) | 52 (hex) | D8 (hex) | 60 or C7 (hex) |
| 2nd byte | | ADD1 | ADD1 | ADD1 | ADD1 | |
| 3rd byte | | ADD2 | ADD2 | ADD2 | ADD2 | |
| 4th byte | | ADD3 | ADD3 | ADD3 | ADD3 | |
| 5th byte | | | | | | |
| Data Cycles | 1-256 | 1-256 | | | | |
| Action | to program the selected page | quad input to program the selected page | to erase the selected sector | to erase the selected 32K block | to erase the selected block | to erase whole chip |

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Read/Write Array Commands (4 Byte Address Command Set)

| Command (byte) | READ4B | FAST READ4B | 2READ4B | DREAD4B | 4READ4B | QREAD4B |
|----------------|----------------------------------|----------------------------------|---|---|---|---|
| Mode | SPI | SPI | SPI | SPI | SPI/QPI | SPI |
| Address Bytes | 4 | 4 | 4 | 4 | 4 | 4 |
| 1st byte | 13 (hex) | 0C (hex) | BC (hex) | 3C (hex) | EC (hex) | 6C (hex) |
| 2nd byte | ADD1 | ADD1 | ADD1 | ADD1 | ADD1 | ADD1 |
| 3rd byte | ADD2 | ADD2 | ADD2 | ADD2 | ADD2 | ADD2 |
| 4th byte | ADD3 | ADD3 | ADD3 | ADD3 | ADD3 | ADD3 |
| 5th byte | ADD4 | ADD4 | ADD4 | ADD4 | ADD4 | ADD4 |
| 6th byte | | Dummy | Dummy | Dummy | Dummy | Dummy |
| Data Cycles | | | | | | |
| Action | read data byte by 4 byte address | read data byte by 4 byte address | read data byte by 2 x I/O with 4 byte address | Read data byte by Dual Output with 4 byte address | read data byte by 4 x I/O with 4 byte address | Read data byte by Quad Output with 4 byte address |

| Command (byte) | PP4B | 4PP4B | BE4B (block erase 64KB) | BE32K4B (block erase 32KB) | SE4B (Sector erase 4KB) |
|----------------|---|--|---|---|---|
| Mode | SPI/QPI | SPI | SPI/QPI | SPI/QPI | SPI/QPI |
| Address Bytes | 4 | 4 | 4 | 4 | 4 |
| 1st byte | 12 (hex) | 3E (hex) | DC (hex) | 5C (hex) | 21 (hex) |
| 2nd byte | ADD1 | ADD1 | ADD1 | ADD1 | ADD1 |
| 3rd byte | ADD2 | ADD2 | ADD2 | ADD2 | ADD2 |
| 4th byte | ADD3 | ADD3 | ADD3 | ADD3 | ADD3 |
| 5th byte | ADD4 | ADD4 | ADD4 | ADD4 | ADD4 |
| 6th byte | | | | | |
| Data Cycles | 1-256 | 1-256 | | | |
| Action | to program the selected page with 4byte address | Quad input to program the selected page with 4byte address | to erase the selected (64KB) block with 4byte address | to erase the selected (32KB) block with 4byte address | to erase the selected (4KB) sector with 4byte address |

Register/Setting Commands

| Command (byte) | WREN (write enable) | WRDI (write disable) | RDSR (read status register) | RDCR (read configuration register) | WRSR (write status/ configuration register) | RDEAR (read extended address register) | WREAR (write extended address register) |
|----------------|---------------------------------------|---|---|--|---|--|---|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| 1st byte | 06 (hex) | 04 (hex) | 05 (hex) | 15 (hex) | 01 (hex) | C8 (hex) | C5 (hex) |
| 2nd byte | | | | | Values | | |
| 3rd byte | | | | | Values | | |
| 4th byte | | | | | | | |
| 5th byte | | | | | | | |
| Data Cycles | | | | | 1-2 | | 1 |
| Action | sets the (WEL) write enable latch bit | resets the (WEL) write enable latch bit | to read out the values of the status register | to read out the values of the configuration register | to write new values of the status/ configuration register | read extended address register | write extended address register |

| Command (byte) | WPSEL (Write Protect Selection) | EQIO (Enable QPI) | RSTQIO (Reset QPI) | EN4B (enter 4-byte mode) | EX4B (exit 4-byte mode) | PGM/ERS Suspend (Suspends Program/ Erase) | PGM/ERS Resume (Resumes Program/ Erase) |
|----------------|---|-----------------------|----------------------|---|---|---|---|
| Mode | SPI/QPI | SPI | QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| 1st byte | 68 (hex) | 35 (hex) | F5 (hex) | B7 (hex) | E9 (hex) | B0 (hex) | 30 (hex) |
| 2nd byte | | | | | | | |
| 3rd byte | | | | | | | |
| 4th byte | | | | | | | |
| 5th byte | | | | | | | |
| Data Cycles | | | | | | | |
| Action | to enter and enable individual block protect mode | Entering the QPI mode | Exiting the QPI mode | to enter 4-byte mode and set 4BYTE bit as "1" | to exit 4-byte mode and clear 4BYTE bit to be "0" | | |

| Command (byte) | DP (Deep power down) | RDP (Release from deep power down) | SBL (Set Burst Length) | RDFBR (read fast boot register) | WRFBR (write fast boot register) | ESFBR (erase fast boot register) |
|----------------|-----------------------------|------------------------------------|------------------------|---------------------------------|----------------------------------|----------------------------------|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI | SPI | SPI | SPI |
| 1st byte | B9 (hex) | AB (hex) | C0 (hex) | 16(hex) | 17(hex) | 18(hex) |
| 2nd byte | | | | | | |
| 3rd byte | | | | | | |
| 4th byte | | | | | | |
| 5th byte | | | | | | |
| Data Cycles | | | | 1-4 | 4 | |
| Action | enters deep power down mode | release from deep power down mode | to set Burst length | | | |

ID/Security Commands

| Command (byte) | RDID (read identification) | RES (read electronic ID) | REMS (read electronic manufacturer & device ID) | QPIID (QPI ID Read) | RDSFDP | ENSO (enter secured OTP) | EXSO (exit secured OTP) |
|----------------|---|------------------------------|---|---------------------|--------------------------------------|--------------------------------------|-------------------------------------|
| Mode | SPI | SPI/QPI | SPI | QPI | SPI/QPI | SPI/QPI | SPI/QPI |
| Address Bytes | 0 | 0 | 0 | 0 | 3 | 0 | 0 |
| 1st byte | 9F (hex) | AB (hex) | 90 (hex) | AF (hex) | 5A (hex) | B1 (hex) | C1 (hex) |
| 2nd byte | | x | x | | ADD1 | | |
| 3rd byte | | x | x | | ADD2 | | |
| 4th byte | | | ADD1 ^(Note 1) | | ADD3 | | |
| 5th byte | | | | | Dummy (8) | | |
| Action | outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID | to read out 1-byte Device ID | output the Manufacturer ID & Device ID | ID in QPI interface | n bytes read out until CS# goes high | to enter the 4K-bit secured OTP mode | to exit the 4K-bit secured OTP mode |

| Command (byte) | RDSCUR (read security register) | WRSCUR (write security register) | GBLK (gang block lock) | GBULK (gang block unlock) | WRLR (write Lock register) | RDLR (read Lock register) | WRPASS (write password register) | RDPASS (read password register) |
|----------------|------------------------------------|---|--------------------------|---------------------------|----------------------------|---------------------------|----------------------------------|---------------------------------|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI | SPI/QPI | SPI | SPI | SPI | SPI |
| Address Bytes | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1st byte | 2B (hex) | 2F (hex) | 7E (hex) | 98 (hex) | 2C (hex) | 2D (hex) | 28 (hex) | 27 (hex) |
| 2nd byte | | | | | | | | |
| 3rd byte | | | | | | | | |
| 4th byte | | | | | | | | |
| 5th byte | | | | | | | | |
| Data Cycles | | | | | 2 | 2 | 1-8 | 1-8 |
| Action | to read value of security register | to set the lock-down bit as "1" (once lock-down, cannot be updated) | whole chip write protect | whole chip unprotect | | | | |

| Command (byte) | PASSULK (password unlock) | WRSPB (SPB bit program) | ESSPB (all SPB bit erase) | RDSPB (read SPB status) | SPBLK (SPB lock set) | RDSPBLK (SPB lock register read) | WRDPB (write DPB register) | RDDPB (read DPB register) |
|----------------|---------------------------|-------------------------|---------------------------|-------------------------|----------------------|----------------------------------|----------------------------|---------------------------|
| Mode | SPI | SPI | SPI | SPI | SPI | SPI | SPI | SPI |
| Address Bytes | 0 | 4 | 0 | 4 | 0 | 0 | 4 | 4 |
| 1st byte | 29 (hex) | E3 (hex) | E4 (hex) | E2 (hex) | A6 (hex) | A7 (hex) | E1 (hex) | E0 (hex) |
| 2nd byte | | ADD1 | | ADD1 | | | ADD1 | ADD1 |
| 3rd byte | | ADD2 | | ADD2 | | | ADD2 | ADD2 |
| 4th byte | | ADD3 | | ADD3 | | | ADD3 | ADD3 |
| 5th byte | | ADD4 | | ADD4 | | | ADD4 | ADD4 |
| Data Cycles | 8 | | | 1 | | 2 | 1 | 1 |
| Action | | | | | | | | |

Reset Commands

| Command (byte) | NOP (No Operation) | RSTEN (Reset Enable) | RST (Reset Memory) |
|----------------|--------------------|----------------------|--------------------|
| Mode | SPI/QPI | SPI/QPI | SPI/QPI |
| 1st byte | 00 (hex) | 66 (hex) | 99 (hex) |
| 2nd byte | | | |
| 3rd byte | | | |
| 4th byte | | | |
| 5th byte | | | |
| Action | | | |

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1 which is different from 1 x I/O condition.

Note 2: ADD=00H will output the manufacturer ID first and AD=01H will output device ID first.

Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 4: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

Note 5: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in. Please note the number after "ADD" are based on 3-byte address mode, for 4-byte address mode, which will be increased.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 7. Write Enable (WREN) Sequence (SPI Mode)

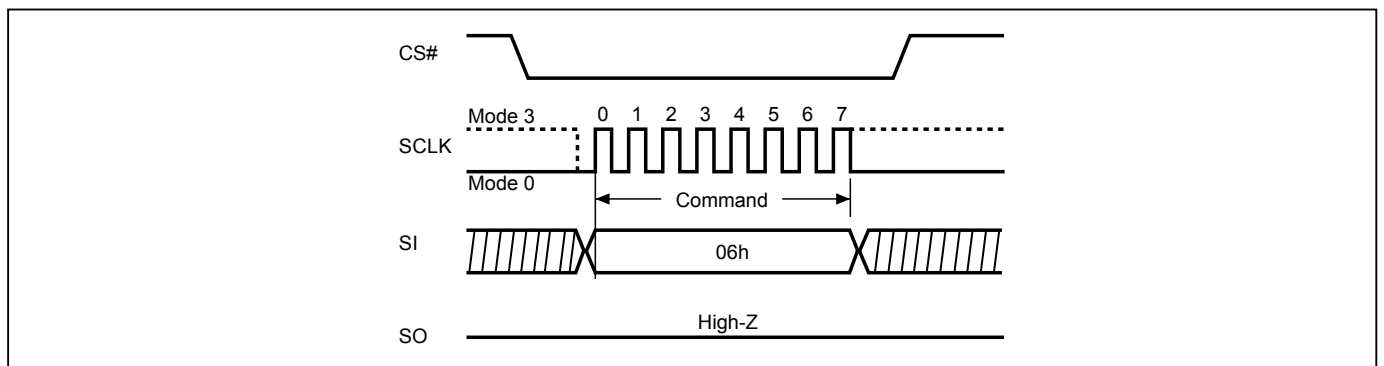
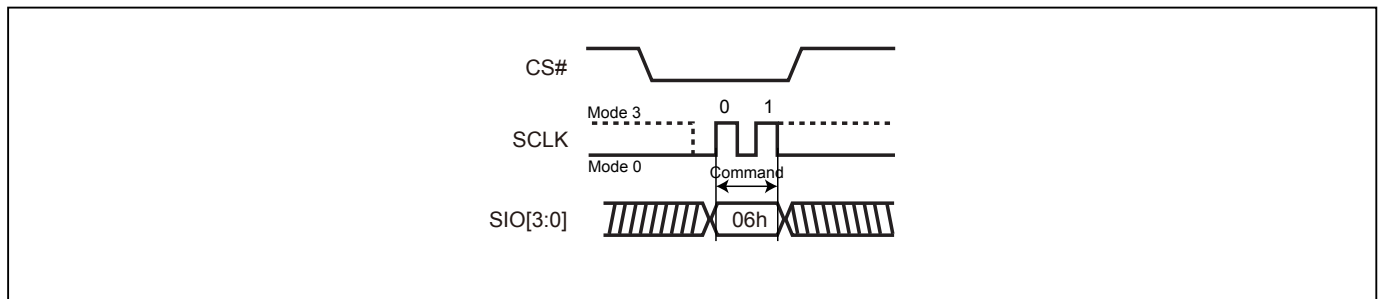


Figure 8. Write Enable (WREN) Sequence (QPI Mode)



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR command completion
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WREAR command completion
- WRLR command completion
- WRPASS command completion
- SPBLK command completion
- WRSPB command completion
- ESSPB command completion
- WRDPB command completion
- WRFBR command completion
- ESFBR command completion

Figure 9. Write Disable (WRDI) Sequence (SPI Mode)

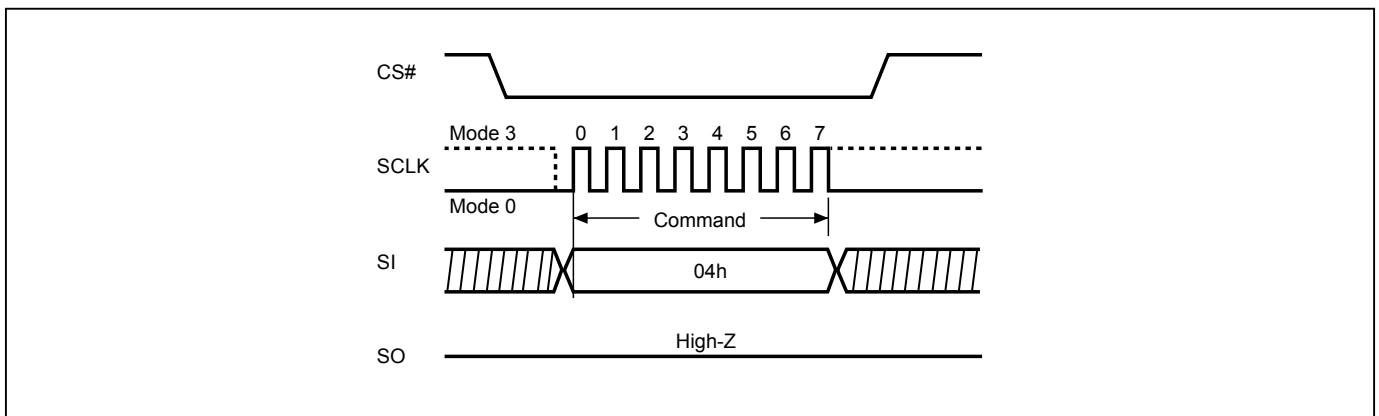
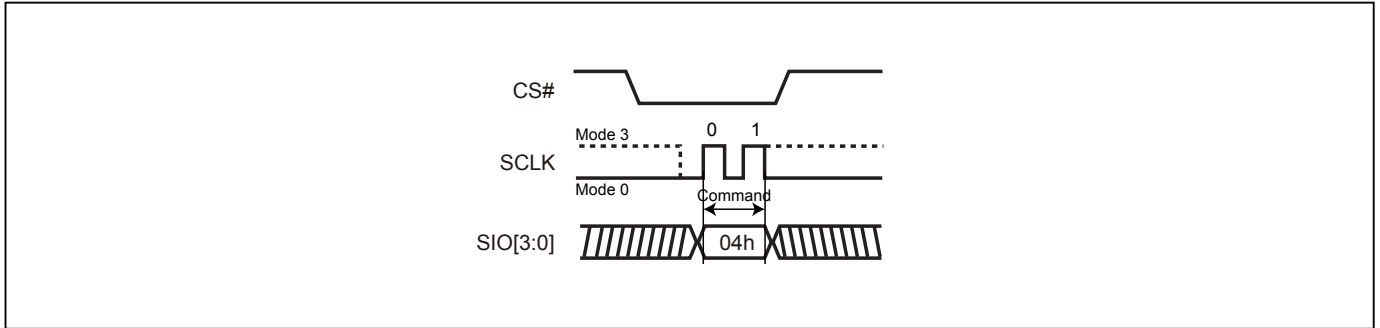


Figure 10. Write Disable (WRDI) Sequence (QPI Mode)



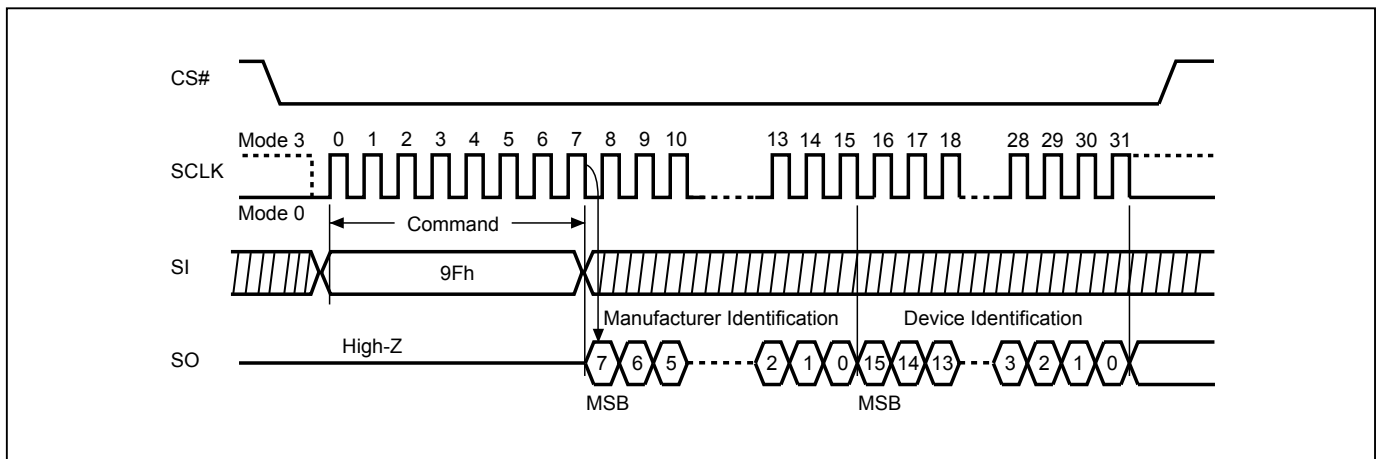
9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as [Table 6 ID Definitions](#).

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 11. Read Identification (RDID) Sequence (SPI mode only)



9-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2} , and Chip Select (CS#) must remain High for at least $t_{RES2(max)}$, as specified in [Table 19](#) AC Characteristics. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as [Table 6](#) ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of t_{RES2} to transit to standby mode, and CS# must remain to high at least $t_{RES2(max)}$. Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 12. Read Electronic Signature (RES) Sequence (SPI Mode)

