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# MX25L25645G

3V, 256M-BIT [x 1/x 2/x 4]  
CMOS MXSMIO<sup>®</sup> (SERIAL MULTI I/O)  
FLASH MEMORY

## ***Key Features***

- *Protocol Support - Single I/O, Dual I/O and Quad I/O*
  - *Support DTR (Double Transfer Rate) Mode*
  - *Support clock frequency up to 133MHz*
-

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**3V 256M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O)  
FLASH MEMORY****1. FEATURES****GENERAL**

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 268,435,456 x 1 bit structure  
or 134,217,728 x 2 bits (two I/O mode) structure  
or 67,108,864 x 4 bits (four I/O mode) structure
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V
- Fast read for SPI mode
  - Support clock frequency up to 133MHz for all protocols
  - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Support DTR (Double Transfer Rate) Mode
  - Configurable dummy cycle number for fast read operation
- Quad Peripheral Interface (QPI) available
- Equal Sectors with 4K byte each,  
or Equal Blocks with 32K byte each  
or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

**SOFTWARE FEATURES**

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions

  - Individual sector protection function (Solid Protect)

- Additional 4K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

**HARDWARE FEATURES**

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware Write Protection or Serial Data Input/Output for 4 x I/O read mode
- RESET#/SIO3
  - Hardware Reset pin or Serial Data Input/Output for 4 x I/O read mode
- RESET#
  - Hardware Reset pin
- NC/SIO3
  - NC or Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-pins SOP (200mil)
  - 8-land WSON (8x6mm, 6x5mm)
  - 24-ball BGA (4x6 ball array)
  - 24-Ball BGA (5x5 ball array)
  - **All devices are RoHS Compliant and Halogen-free**

## 2. GENERAL DESCRIPTION

MX25L25645G is 256Mb bits Serial NOR Flash memory, which is configured as 33,554,432 x 8 internally. When it is in two or four I/O mode, the structure becomes 134,217,728 bits x 2 or 67,108,864 bits x 4.

MX25L25645G features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# and RESET# pin (of the 8-pin packages) become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25L25645G MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25L25645G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

**Table 1. Read performance Comparison**

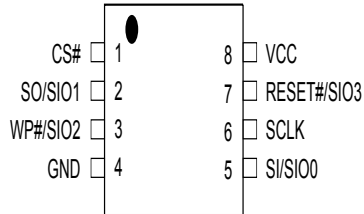
Numbers of Dummy Cycles	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual IO Fast Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	80*	54	-
6	-	-	-	-	80*	54*
8	120*/133R	120*/133R	120*/133R	120/133R	84/104R	70/80R
10	-	-	-	-	120/133R	84/100R

**Notes:**

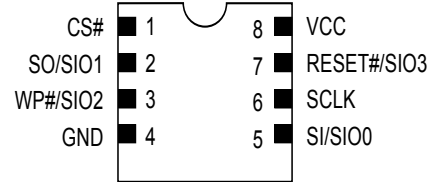
1. \* mean default status.
2. R mean VCC range = 3.0V-3.6V.

### 3. PIN CONFIGURATIONS

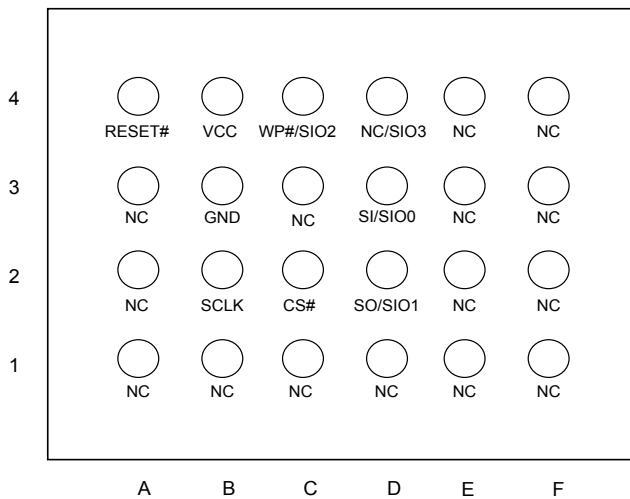
#### 8-PIN SOP (200mil)



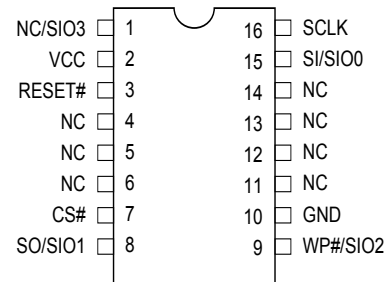
#### 8-WSON (8x6mm, 6x5mm)



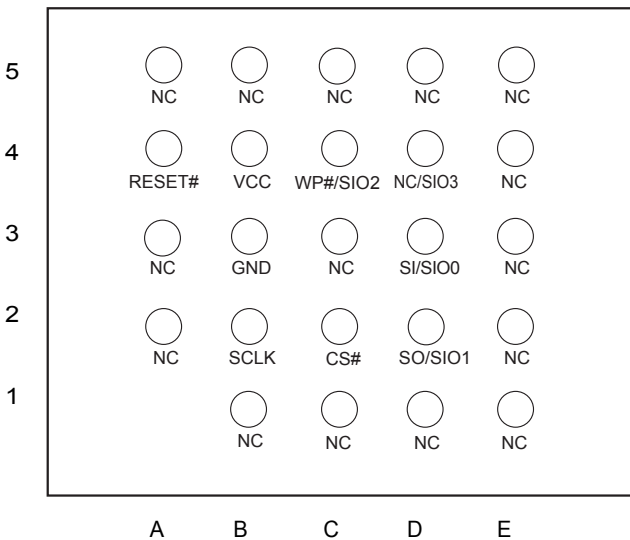
#### 24-Ball BGA (4x6 ball array)



#### 16-PIN SOP (300mil)



#### 24-Ball BGA (5x5 ball array)



### 4. PIN DESCRIPTION

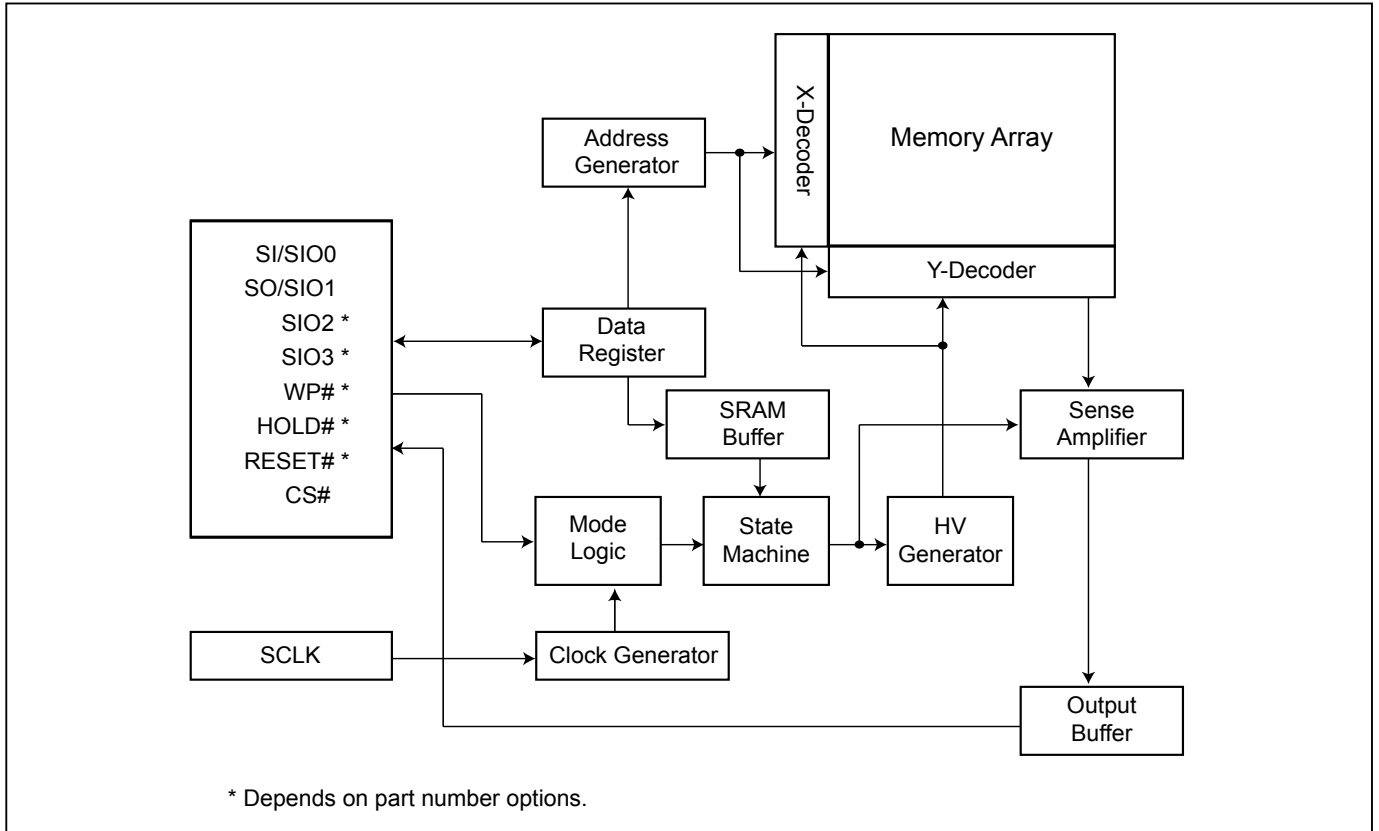
SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
RESET#/SIO3	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC or Serial Data Input & Output (for 4xI/O read mode)
RESET#*	Hardware Reset Pin Active low
VCC	+ 3V Power Supply
GND	Ground
NC	No Connection

**\*Note:** The pin of RESET#, RESET#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration.

However, the internal pull up function will be disabled if the system has physical connection to RESET#, RESET#/SIO3 or WP#/SIO2 pin.



**5. BLOCK DIAGRAM**



## 6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

**I. Block lock protection**

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as "[Table 2. Protected Area Sizes](#)", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

**Table 2. Protected Area Sizes**

**Protected Area Sizes (T/B bit = 0)**

Status bit				Protect Level
BP3	BP2	BP1	BP0	256Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 511 <sup>th</sup> )
0	0	1	0	2 (2 blocks, protected block 510 <sup>th</sup> -511 <sup>th</sup> )
0	0	1	1	3 (4 blocks, protected block 508 <sup>th</sup> -511 <sup>th</sup> )
0	1	0	0	4 (8 blocks, protected block 504 <sup>th</sup> -511 <sup>th</sup> )
0	1	0	1	5 (16 blocks, protected block 496 <sup>th</sup> -511 <sup>th</sup> )
0	1	1	0	6 (32 blocks, protected block 480 <sup>th</sup> -511 <sup>th</sup> )
0	1	1	1	7 (64 blocks, protected block 448 <sup>th</sup> -511 <sup>th</sup> )
1	0	0	0	8 (128 blocks, protected block 384 <sup>th</sup> -511 <sup>th</sup> )
1	0	0	1	9 (256 blocks, protected block 256 <sup>th</sup> -511 <sup>th</sup> )
1	0	1	0	10 (512 blocks, protected all)
1	0	1	1	11 (512 blocks, protected all)
1	1	0	0	12 (512 blocks, protected all)
1	1	0	1	13 (512 blocks, protected all)
1	1	1	0	14 (512 blocks, protected all)
1	1	1	1	15 (512 blocks, protected all)

**Protected Area Sizes (T/B bit = 1)**

Status bit				Protect Level
BP3	BP2	BP1	BP0	256Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0 <sup>th</sup> )
0	0	1	0	2 (2 blocks, protected block 0 <sup>th</sup> -1 <sup>st</sup> )
0	0	1	1	3 (4 blocks, protected block 0 <sup>th</sup> -3 <sup>rd</sup> )
0	1	0	0	4 (8 blocks, protected block 0 <sup>th</sup> -7 <sup>th</sup> )
0	1	0	1	5 (16 blocks, protected block 0 <sup>th</sup> -15 <sup>th</sup> )
0	1	1	0	6 (32 blocks, protected block 0 <sup>th</sup> -31 <sup>st</sup> )
0	1	1	1	7 (64 blocks, protected block 0 <sup>th</sup> -63 <sup>rd</sup> )
1	0	0	0	8 (128 blocks, protected block 0 <sup>th</sup> -127 <sup>th</sup> )
1	0	0	1	9 (256 blocks, protected block 0 <sup>th</sup> -255 <sup>th</sup> )
1	0	1	0	10 (512 blocks, protected all)
1	0	1	1	11 (512 blocks, protected all)
1	1	0	0	12 (512 blocks, protected all)
1	1	0	1	13 (512 blocks, protected all)
1	1	1	0	14 (512 blocks, protected all)
1	1	1	1	15 (512 blocks, protected all)

**II. Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to ["Table 12. Security Register Definition"](#) for security register bit definition and ["Table 3. 4K-bit Secured OTP Definition"](#) for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

**Table 3. 4K-bit Secured OTP Definition**

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010-xxx1FF	3968-bit	N/A	

## 7. Memory Organization

**Table 4. Memory Organization**

Block(64K-byte)	Block(32K-byte)	Sector	Address Range		
511	1023	8191	1FFF000h	1FFFFFFh	
		⋮	⋮	⋮	
		8184	1FF8000h	1FF8FFFh	
		8183	1FF7000h	1FF7FFFh	
	1022	⋮	⋮	⋮	⋮
		8176	1FF0000h	1FF0FFFh	
		8175	1FEF000h	1FEFFFFh	
		⋮	⋮	⋮	
510	1021	8168	1FE8000h	1FE8FFFh	
		8167	1FE7000h	1FE7FFFh	
		⋮	⋮	⋮	
		8160	1FE0000h	1FE0FFFh	
	1020	8159	1FDF000h	1FDFFFFh	
		⋮	⋮	⋮	
		8152	1FD8000h	1FD8FFFh	
		8151	1FD7000h	1FD7FFFh	
509	1019	⋮	⋮	⋮	
		8144	1FD0000h	1FD0FFFh	
		⋮	⋮	⋮	
		8144	1FD0000h	1FD0FFFh	
	1018	⋮	⋮	⋮	⋮
		⋮	⋮	⋮	⋮
		⋮	⋮	⋮	⋮
		⋮	⋮	⋮	⋮

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

2	5	47	002F000h	002FFFFh	
		⋮	⋮	⋮	
		40	0028000h	0028FFFh	
		39	027000h	0027FFFh	
	4	⋮	⋮	⋮	⋮
		32	0020000h	0020FFFh	
		31	001F000h	001FFFFh	
		⋮	⋮	⋮	
1	3	24	0018000h	0018FFFh	
		23	0017000h	0017FFFh	
		⋮	⋮	⋮	
		16	0010000h	0010FFFh	
	2	15	000F000h	000FFFFh	
		⋮	⋮	⋮	
		8	0008000h	0008FFFh	
		7	0007000h	0007FFFh	
0	1	⋮	⋮	⋮	
		⋮	⋮	⋮	
		⋮	⋮	⋮	
		0	0000000h	0000FFFh	
	0	⋮	⋮	⋮	⋮
		⋮	⋮	⋮	⋮
		⋮	⋮	⋮	⋮
		⋮	⋮	⋮	⋮

individual block lock/unlock unit:64K-byte

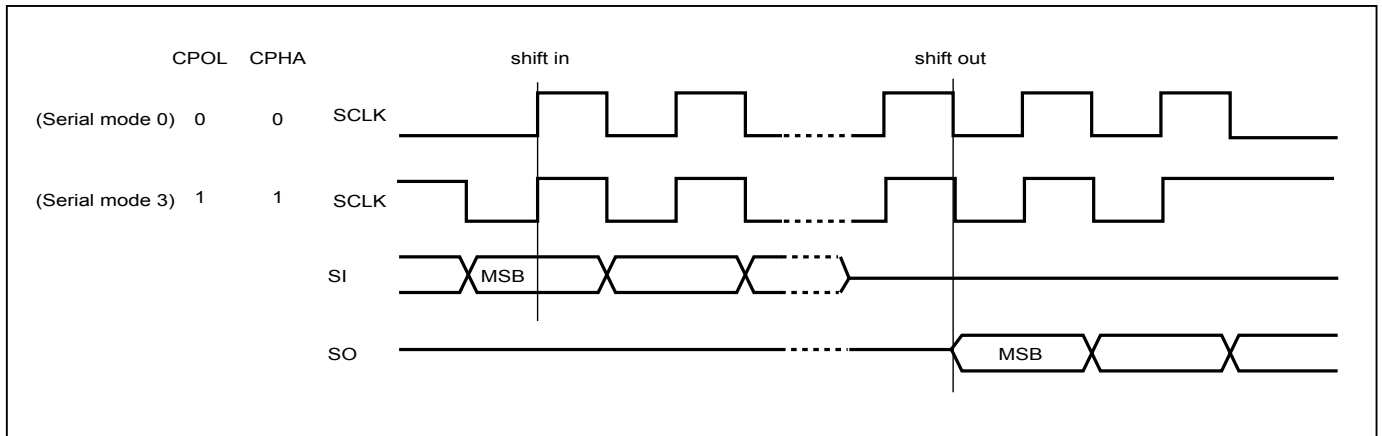
individual 16 sectors lock/unlock unit:4K-byte



## 8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "[Figure 1. Serial Modes Supported](#)".
5. For the following instructions: RDID, RDSR, RDSCUR, READ/READ4B, FAST\_READ/FAST\_READ4B, 2READ/2READ4B, DREAD/DREAD4B, 4READ/4READ4B, QREAD/QREAD4B, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDEAR, RDCR, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, PP/PP4B, 4PP/4PP4B, DP, ENSO, EXSO, WRSCUR, EN4B, EX4B, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

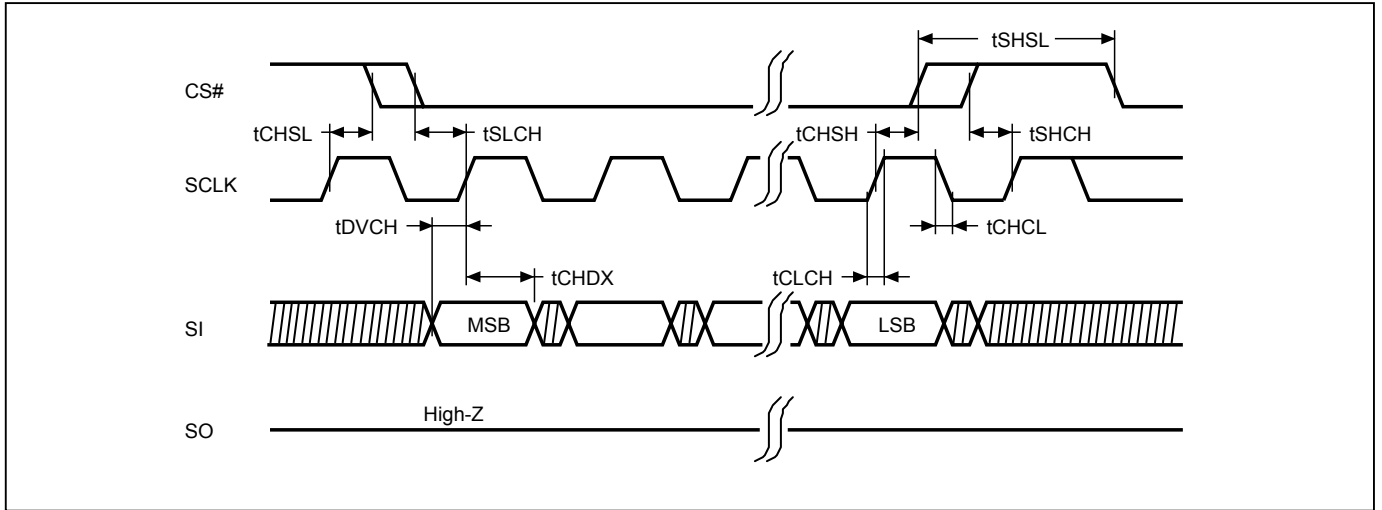
**Figure 1. Serial Modes Supported**



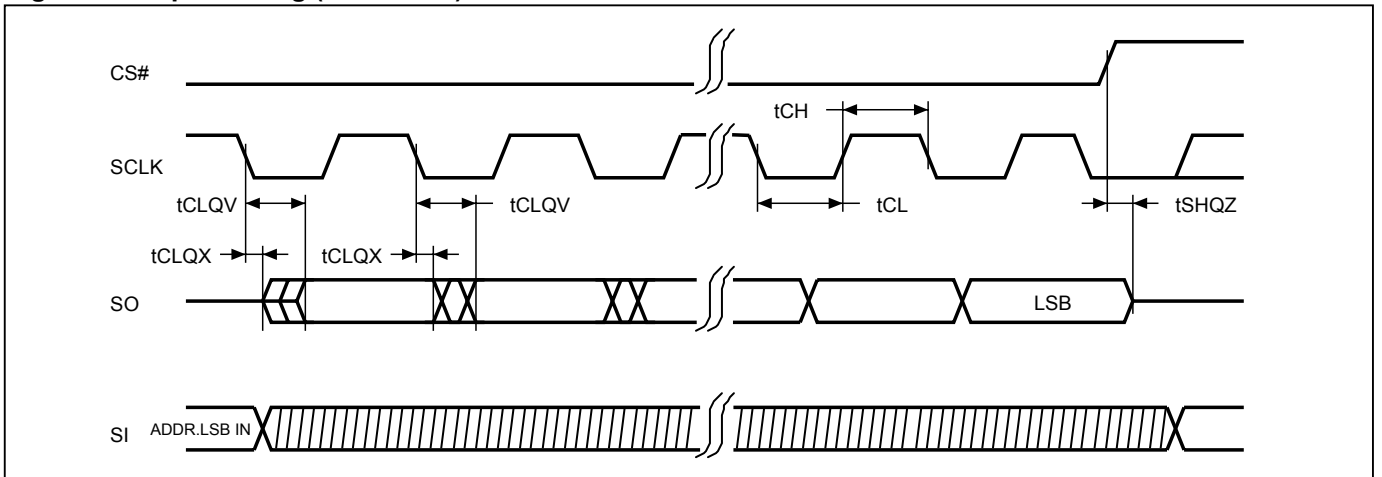
**Note:**

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

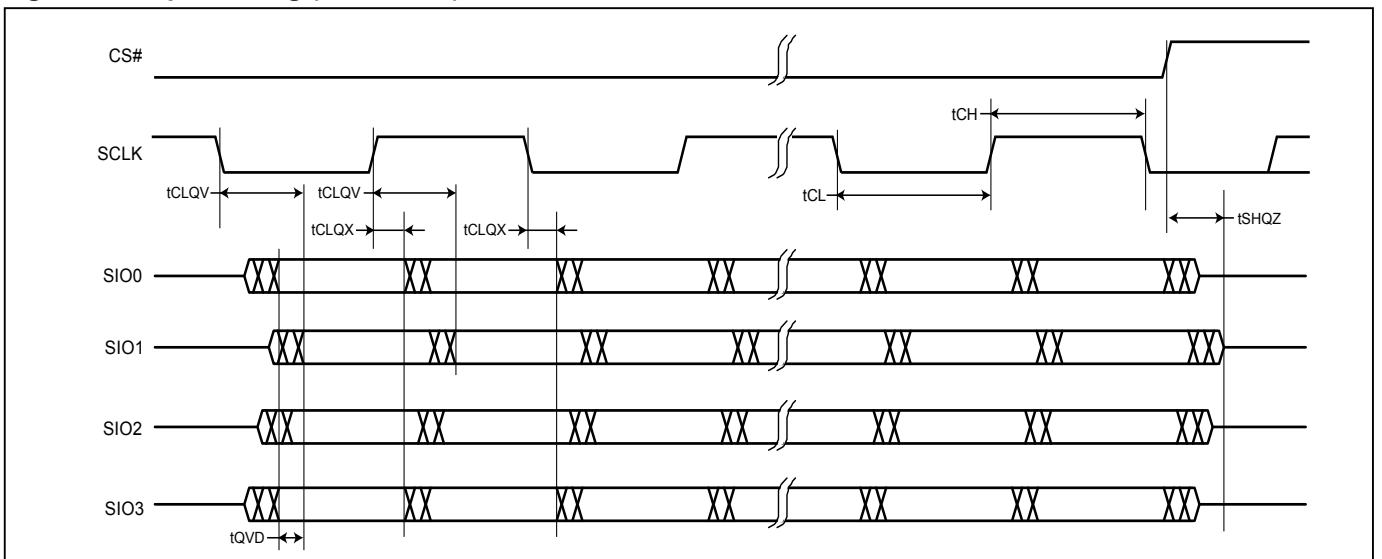
**Figure 2. Serial Input Timing**



**Figure 3. Output Timing (STR mode)**



**Figure 4. Output Timing (DTR mode)**



## 8-1. 256Mb Address Protocol

The original 24 bit address protocol of Serial NOR Flash can only access density size below 128Mb. For the memory device of 256Mb and above, the 32bit address is requested for access higher memory size. The MX25L25645G provides three different methods to access the whole 256Mb density:

**(1)Command entry 4-byte address mode:** Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register bit. After 4BYTE bit has been set, the number of address cycle become 32-bit.

**(2)Extended Address Register (EAR):** configure the memory device into two 128Mb segments to select which one is active through the EAR bit "0".

**(3)4-byte Address Command Set:** When issuing 4-byte address command set, 4-byte address (A31-A0) is requested after the instruction code. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

### Enter 4-Byte Address Mode

In 4-byte Address mode, all instructions are 32-bits address clock cycles. By using EN4B and EX4B to enable and disable the 4-byte address mode.

When 4-byte address mode is enabled, the EAR<0> becomes "don't care" for all instructions requiring 4-byte address. The EAR function will be disabled when 4-byte mode is enabled.

### Extended Address Register (Configurable)

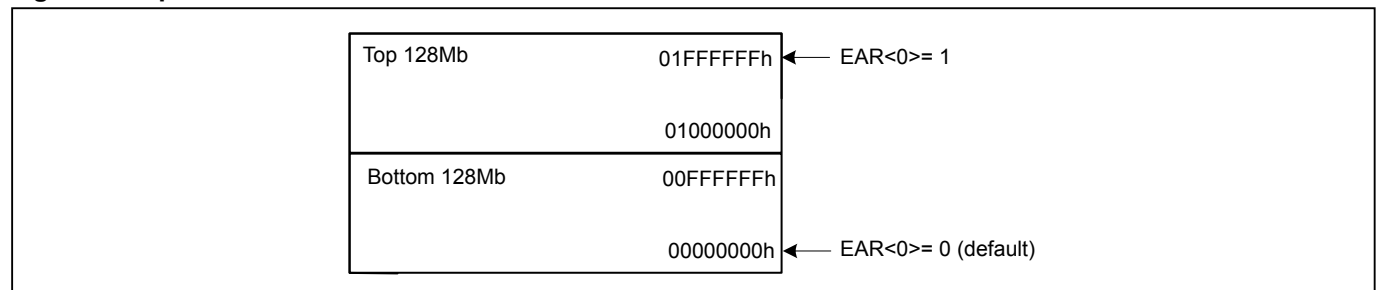
The device provides an 8-bit volatile register for extended Address Register: it identifies the extended address (A31~A24) above 128Mb density by using original 3-byte address.

### Extended Address Register (EAR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A31	A30	A29	A28	A27	A26	A25	A24

For the MX25L25645G the A31 to A25 are Don't Care. During EAR, reading these bits will read as 0. The bit 0 is default as "0".

**Figure 5. Top and Bottom 128M bits**



When under EAR mode, Read, Program, Erase operates in the selected segment by using 3-byte address mode.

For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected top or bottom 128Mb, but it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment.

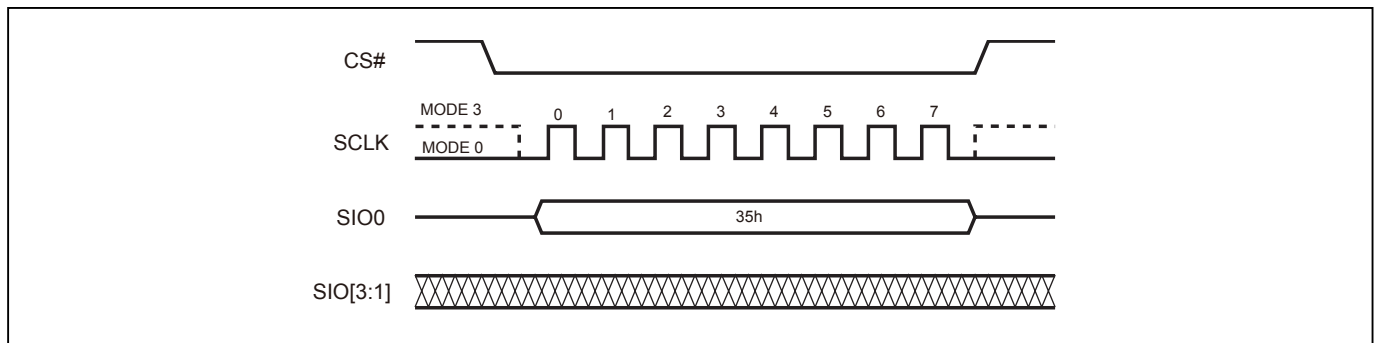
## 8-2. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

### Enable QPI mode

By issuing EQIO (35h) command, the QPI mode is enabled. After QPI mode is enabled, the device enters quad mode (4-4-4) without QE bit status changed.

**Figure 6. Enable QPI Sequence**



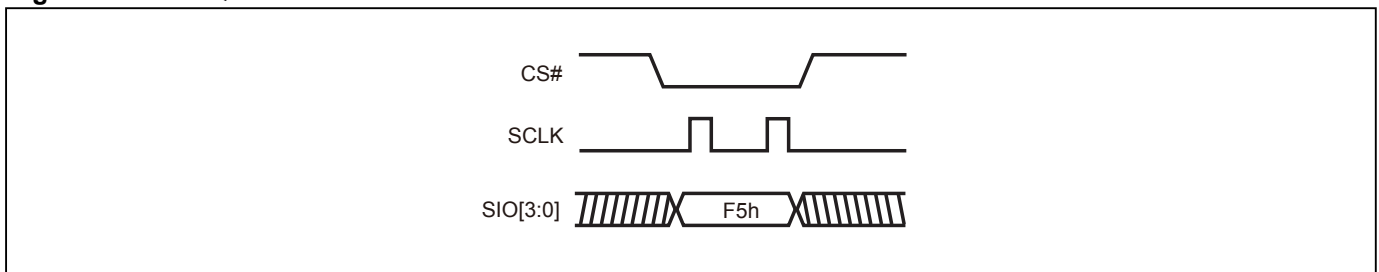
### Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

#### Note:

For EQIO and RSTQIO commands, CS# high width has to follow "From Write/Erase/Program to Read Status Register" tSHSL specification for next instruction, as defined in ["Table 25. AC CHARACTERISTICS \(Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V\)"](#).

**Figure 7. Reset QPI Mode**



## 9. COMMAND DESCRIPTION

**Table 5. Command Set**

### Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I 2O read)	4READ	QREAD (1I 4O read)	4DTRD (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	3/4	3/4
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)	ED (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	Quad I/O read for bottom 128Mb with 6 dummy cycles	n bytes read out by Quad output until CS# goes high	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	0
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte		ADD1	ADD1	ADD1	ADD1	
3rd byte		ADD2	ADD2	ADD2	ADD2	
4th byte		ADD3	ADD3	ADD3	ADD3	
5th byte						
Data Cycles	1-256	1-256				
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

\* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.



**Read/Write Array Commands (4 Byte Address Command Set)**

Command (byte)	READ4B	FAST READ4B	2READ4B	DREAD4B	4READ4B	QREAD4B
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI
Address Bytes	4	4	4	4	4	4
1st byte	13 (hex)	0C (hex)	BC (hex)	3C (hex)	EC (hex)	6C (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte		Dummy	Dummy	Dummy	Dummy	Dummy
Data Cycles						
Action	read data byte by 4 byte address	read data byte by 4 byte address	read data byte by 2 x I/O with 4 byte address	Read data byte by Dual Output with 4 byte address	read data byte by 4 x I/O with 4 byte address	Read data byte by Quad Output with 4 byte address

Command (byte)	4DTRD4B (Quad I/O DT Read)	PP4B	4PP4B	BE4B (block erase 64KB)	BE32K4B (block erase 32KB)	SE4B (Sector erase 4KB)
Mode	SPI/QPI	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3/4	4	4	4	4	4
1st byte	EE (hex)	12 (hex)	3E (hex)	DC (hex)	5C (hex)	21 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte	Dummy*					
Data Cycles		1-256	1-256			
Action	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high	to program the selected page with 4byte address	Quad input to program the selected page with 4byte address	to erase the selected (64KB) block with 4byte address	to erase the selected (32KB) block with 4byte address	to erase the selected (4KB) sector with 4byte address

**Register/Setting Commands**

Command (byte)	WREN (write enable)	WRDI (write disable)	FMEN (factory mode enable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/configuration register)	RDEAR (read extended address register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	06 (hex)	04 (hex)	41 (hex)	05 (hex)	15 (hex)	01 (hex)	C8 (hex)
2nd byte						Values	
3rd byte						Values	
4th byte							
5th byte							
Data Cycles						1-2	
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	enable factory mode	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/configuration register	read extended address register

Command (byte)	WREAR (write extended address register)	WPSEL (Write Protect Selection)	EQIO (Enable QPI)	RSTQIO (Reset QPI)	EN4B (enter 4-byte mode)	EX4B (exit 4-byte mode)	PGM/ERS Suspend (Suspends Program/Erase)
Mode	SPI/QPI	SPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	C5 (hex)	68 (hex)	35 (hex)	F5 (hex)	B7 (hex)	E9 (hex)	B0 (hex)
2nd byte							
3rd byte							
4th byte							
5th byte							
Data Cycles	1						
Action	write extended address register	to enter and enable individual block protect mode	Entering the QPI mode	Exiting the QPI mode	to enter 4-byte mode and set 4BYTE bit as "1"	to exit 4-byte mode and clear 4BYTE bit to be "0"	

Command (byte)	PGM/ERS Resume (Resumes Program/Erase)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	30 (hex)	B9 (hex)	AB (hex)	C0 (hex)
2nd byte				
3rd byte				
4th byte				
5th byte				
Data Cycles				
Action		enters deep power down mode	release from deep power down mode	to set Burst length

**ID/Security Commands**

Command (byte)	RDID (read identification)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	0	0	3	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1		
3rd byte		x	x		ADD2		
4th byte			ADD1		ADD3		
5th byte					Dummy (8)		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID (Note 2)	ID in QPI interface	Read SFDP mode	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	WRSPB (SPB bit program)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	GBLK (gang block lock)	GBULK (gang block unlock)
Mode	SPI/QPI	SPI/QPI	SPI	SPI	SPI	SPI	SPI
Address Bytes	0	0	4	0	4	0	0
1st byte	2B (hex)	2F (hex)	E3 (hex)	E4 (hex)	E2 (hex)	7E (hex)	98 (hex)
2nd byte			ADD1		ADD1		
3rd byte			ADD2		ADD2		
4th byte			ADD3		ADD3		
5th byte			ADD4		ADD4		
Data Cycles					1		
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)				whole chip write protect	whole chip unprotect

Command (byte)	WRLR (write lock register)	RDLR (read lock register)	WRDPB (write DPB register)	RDDPB (read DPB register)
Mode	SPI	SPI	SPI	SPI
Address Bytes	0	0	4	4
1st byte	2C (hex)	2D (hex)	E1 (hex)	E0 (hex)
2nd byte			ADD1	ADD1
3rd byte			ADD2	ADD2
4th byte			ADD3	ADD3
5th byte			ADD4	ADD4
Data Cycles	2	2	1	1
Action				

**Reset Commands**

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			<i>(Note 3)</i>

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

Note 4: The number in parentheses after "Dummy" stands for how many clock cycles it has.

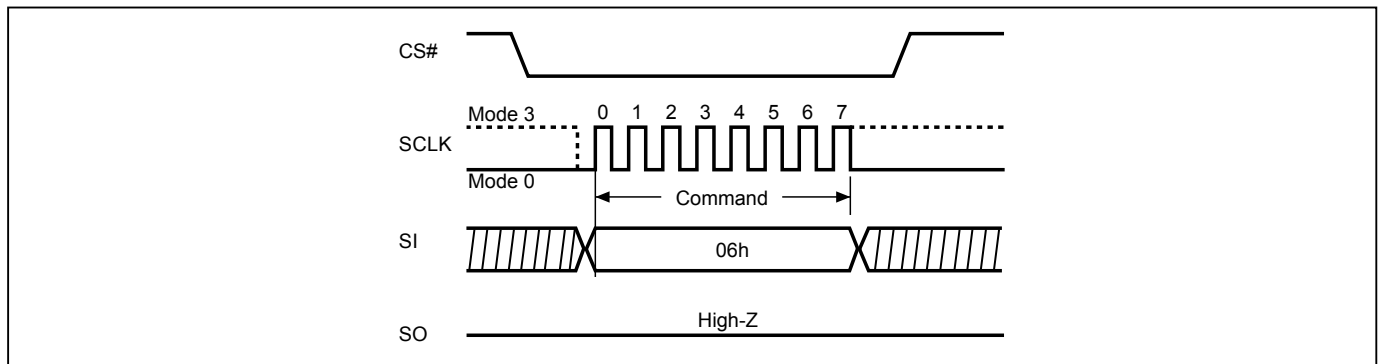
### 9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

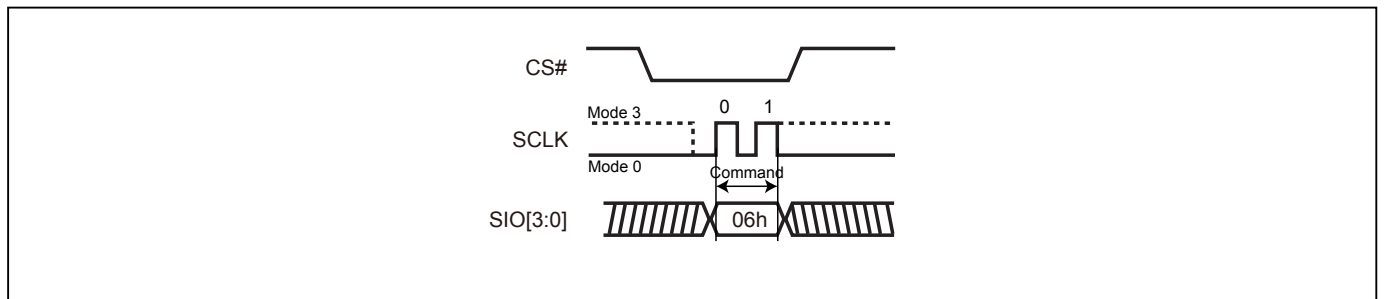
The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

**Figure 8. Write Enable (WREN) Sequence (SPI Mode)**



**Figure 9. Write Enable (WREN) Sequence (QPI Mode)**





## 9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

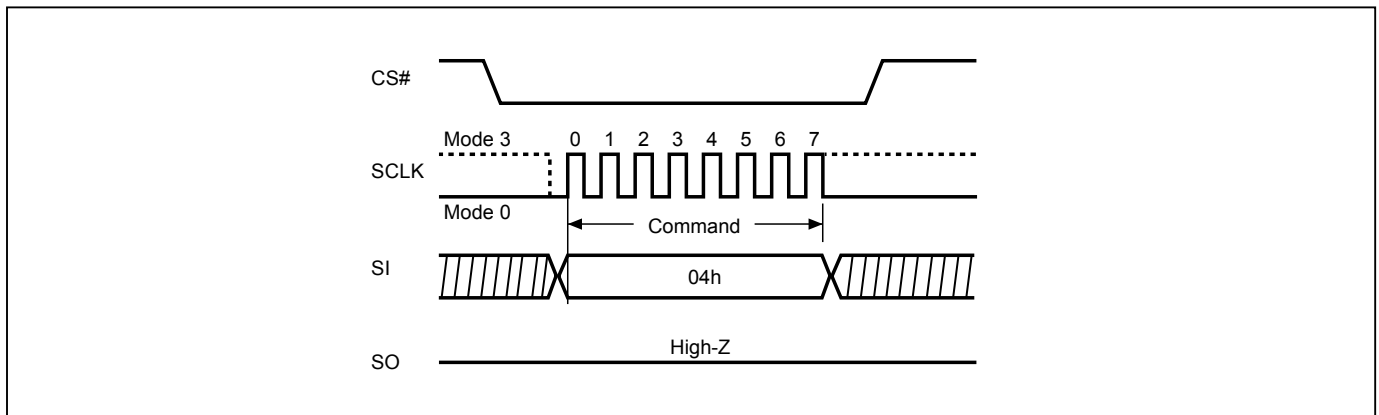
The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

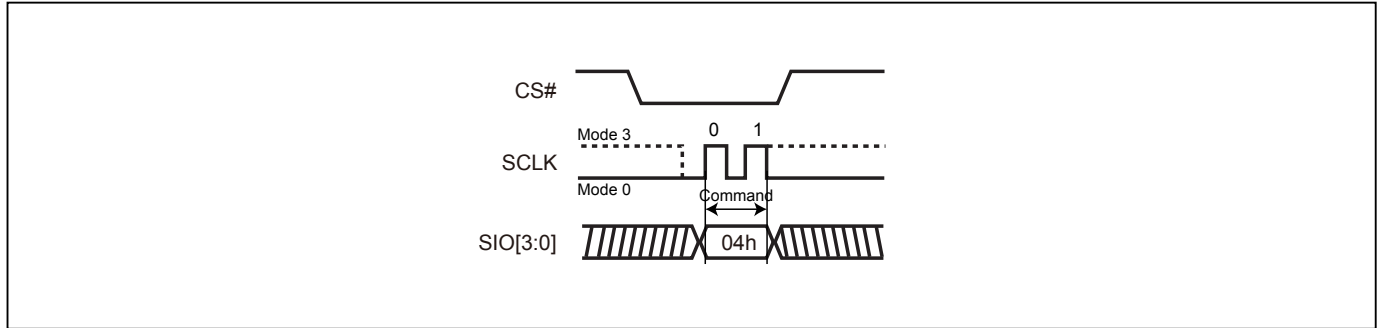
The WEL bit is reset by following situations:

- Power-up
- RESET# pin driven low
- WRDI command completion
- WRSR command completion
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WREAR command completion
- WRLR command completion
- WRSPB command completion
- WRDPB command completion
- ESSPB command completion

**Figure 10. Write Disable (WRDI) Sequence (SPI Mode)**



**Figure 11. Write Disable (WRDI) Sequence (QPI Mode)**



### 9-3. Factory Mode Enable (FMEN)

The Factory Mode Enable (FMEN) instruction is for enhance Program and Erase performance for increase factory production throughput. The FMEN instruction need to combine with the instructions which are intended to change the device content, like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→sending FMEN instruction code→ CS# goes high. A valid factory mode operation need to included three sequences: WREN instruction → FMEN instruction→ Program or Erase instruction.

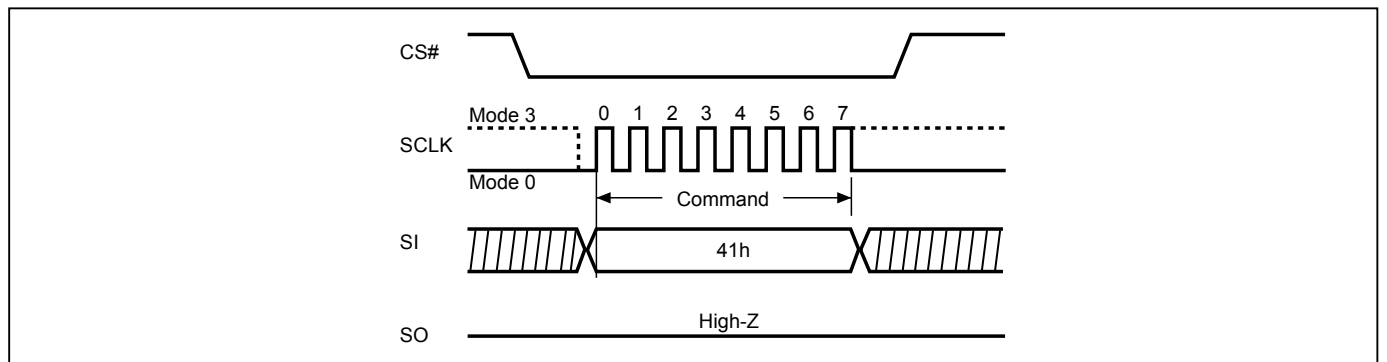
Suspend command is not acceptable under factory mode.

The FMEN is reset by following situations

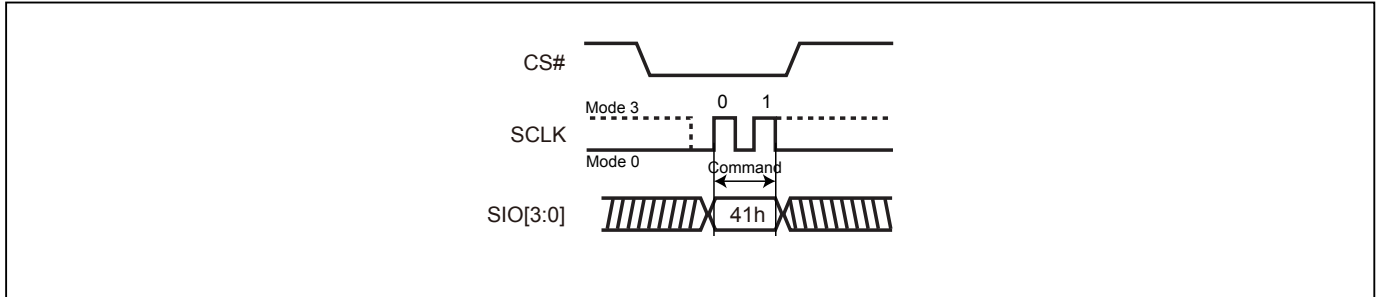
- Power-up
- Reset# pin driven low
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- Softreset command completion

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

**Figure 12. Factory Mode Enable (FMEN) Sequence (SPI Mode)**



**Figure 13. Factory Mode Enable (FMEN) Sequence (QPI Mode)**



**9-4. Read Identification (RDID)**

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as [Table 6 ID Definitions](#).

The sequence of issuing RDID instruction is: CS# goes low → sending RDID instruction code → 24-bits ID data out on SO → to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

**Figure 14. Read Identification (RDID) Sequence (SPI mode only)**

