Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MX25L3233F

3V, 32M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Hold Feature*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Auto Erase and Auto Program Algorithms*
- *Program Suspend/Resume & Erase Suspend/Resume*

Contents

Figures

32M-BIT [x 1 / x 2 / x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 33,554,432 x 1 bit structure
  or 16,777,216 x 2 bits (two I/O read mode) structure
  or 8,388,608 x 4 bits (four I/O mode) structure
- 1024 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 128 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 64 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.65 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  VCC = 2.65 to 3.6V
  - Normal read
    - 50MHz
  - Fast read
    - FAST_READ, DREAD, QREAD:
      133MHz with 8 dummy cycles
    - 2READ:
      104MHz with 4 dummy cycle,
      133MHz with 8 dummy cycle
    - 4READ:
      104MHz with 6 dummy cycle,
      133MHz with 10 dummy cycle
    - Configurable dummy cycle number for 2READ and 4READ operation
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
- Low Power Consumption
- Typical 100,000 erase/program cycles
- 20 years data retention

KEY FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block Lock Protection
  The BP0-BP3 and T/B status bits define the site of the area to be protected against program and erase instructions.
- Additional 4K bits secured OTP
  - Features unique identifier
  - Factory locked identifiable and customer lockable
- Auto Erase and Auto Program Algorithms
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Program/Erase Resume
- Electronic Identification
  - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
  - RES command for 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L3233F is 32Mb bits Serial NOR Flash memory, which is configured as 4,194,304 x 8 internally. When it is in four I/O mode, the structure becomes 8,388,608 bits x 4. When it is in two I/O mode, the structure becomes 16,777,216 bits x 2.

MX25L3233F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L3233F, MXSMIO® (Serial Multi I/O) flash memory, provides sequential read operation on the whole chip and multi-I/O features.

When it is in quad I/O mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis. Erase command is executed on 4K-byte sector, 32K-byte/64K-byte block, or whole chip basis.

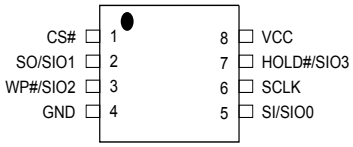
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

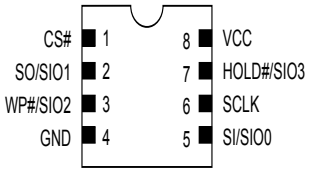
The MX25L3233F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

3. PIN CONFIGURATION

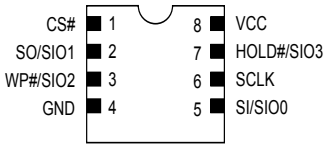
8-PIN SOP (150mil)/8-PIN SOP (200mil)



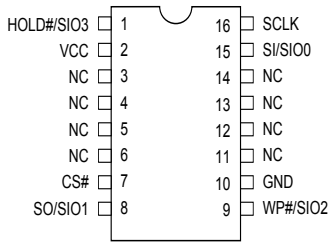
8-LAND USON (4x3mm)



8-WSON (6x5mm)



16-PIN SOP (300mil)



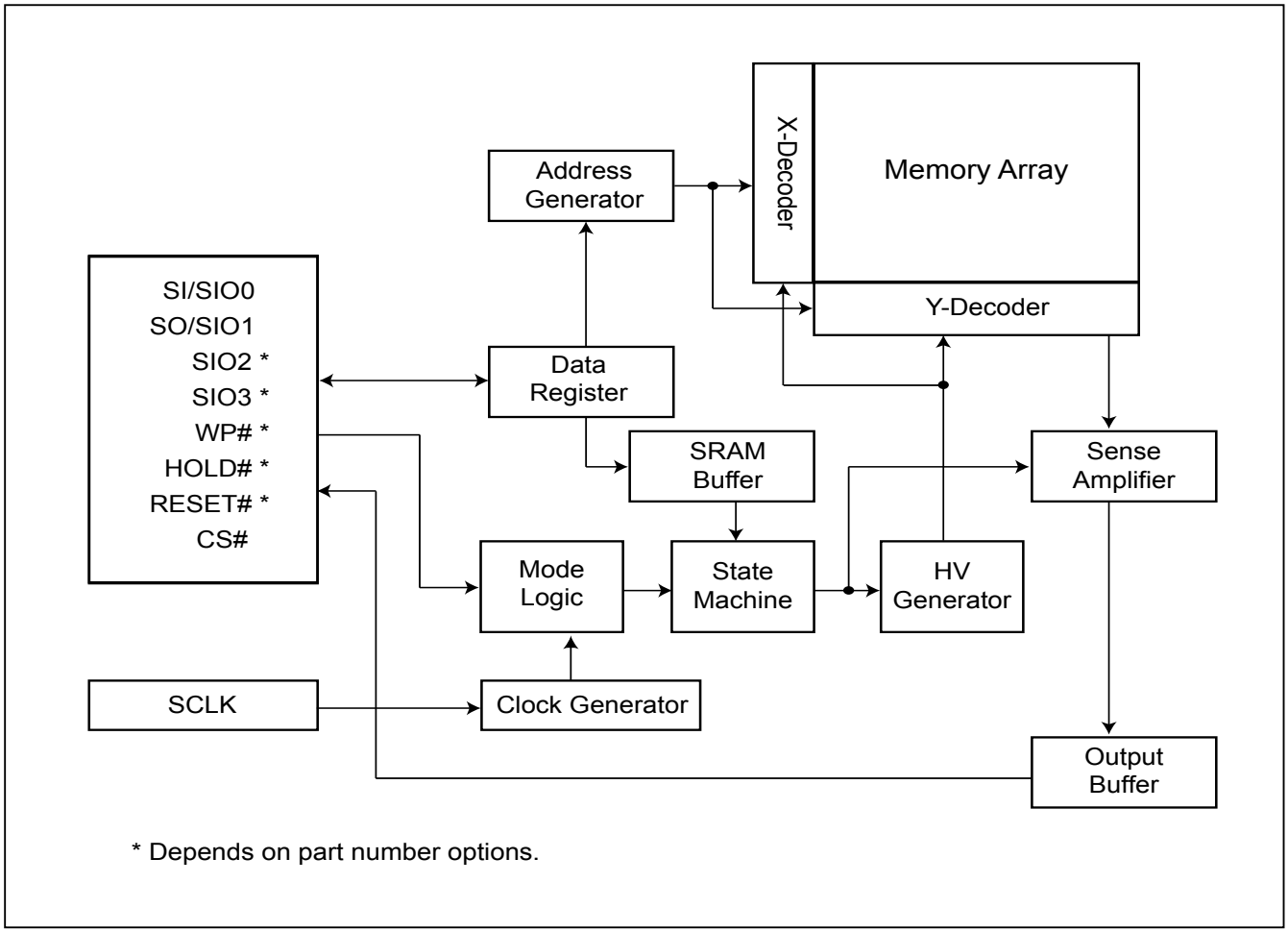
4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection Active Low or Serial Data Input & Output (for 4xI/O mode)
HOLD#/ SIO3	To pause the device without deselecting the device or Serial data Input/Output for 4 x I/O mode
VCC	+ 3.0V Power Supply
GND	Ground
NC	No Connection

Note:

1. The pin of HOLD#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to HOLD#/SIO3 or WP#/SIO2 pin.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

I. Block lock protection

- The Software Protected Mode (SPM) uses (TB, BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of *"Table 1. Protected Area Sizes"*, the protected areas are more flexible which may protect various areas by setting value of TB, BP0-BP3 bits.

- The Hardware Protected Mode (HPM) uses WP#/SIO2 to protect the (BP3, BP2, BP1, BP0, TB) bits and SRWD bit.

Table 1. Protected Area Sizes

Protected Area Sizes (TB bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	32Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 63rd)
0	0	1	0	2 (2blocks, block 62nd-63rd)
0	0	1	1	3 (4blocks, block 60th-63rd)
0	1	0	0	4 (8blocks, block 56th-63rd)
0	1	0	1	5 (16blocks, block 48th-63rd)
0	1	1	0	6 (32blocks, block 32nd-63rd)
0	1	1	1	7 (64blocks, protect all)
1	0	0	0	8 (64blocks, protect all)
1	0	0	1	9 (64blocks, protect all)
1	0	1	0	10 (64blocks, protect all)
1	0	1	1	11 (64blocks, protect all)
1	1	0	0	12 (64blocks, protect all)
1	1	0	1	13 (64blocks, protect all)
1	1	1	0	14 (64blocks, protect all)
1	1	1	1	15 (64blocks, protect all)

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	32Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, block 0th-3rd)
0	1	0	0	4 (8blocks, block 0th-7th)
0	1	0	1	5 (16blocks, block 0th-15th)
0	1	1	0	6 (32blocks, block 0th-31st)
0	1	1	1	7 (64blocks, protect all)
1	0	0	0	8 (64blocks, protect all)
1	0	0	1	9 (64blocks, protect all)
1	0	1	0	10 (64blocks, protect all)
1	0	1	1	11 (64blocks, protect all)
1	1	0	0	12 (64blocks, protect all)
1	1	0	1	13 (64blocks, protect all)
1	1	1	0	14 (64blocks, protect all)
1	1	1	1	15 (64blocks, protect all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. **Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 10. Security Register Definition"* for security register bit definition and *"Table 2. 4K-bit Secured OTP Definition"* for address range definition.

Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 2. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx1FF	4096-bit	Determined by Factory	Determined by customer

7. MEMORY ORGANIZATION

Table 3. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
63	127	1023	3FF000h	3FFFFFh
		⋮		
		1016	3F8000h	3F8FFFh
	126	1015	3F7000h	3F7FFFh
		⋮		
		1008	3F0000h	3F0FFFh
62	125	1007	3EF000h	3EFFFFh
		⋮		
		1000	3E8000h	3E8FFFh
	124	999	3E7000h	3E7FFFh
		⋮		
		992	3E0000h	3E0FFFh
61	123	991	3DF000h	3DFFFFh
		⋮		
		984	3D8000h	3D8FFFh
	122	983	3D7000h	3D7FFFh
		⋮		
		976	3D0000h	3D0FFFh
		⋮		
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

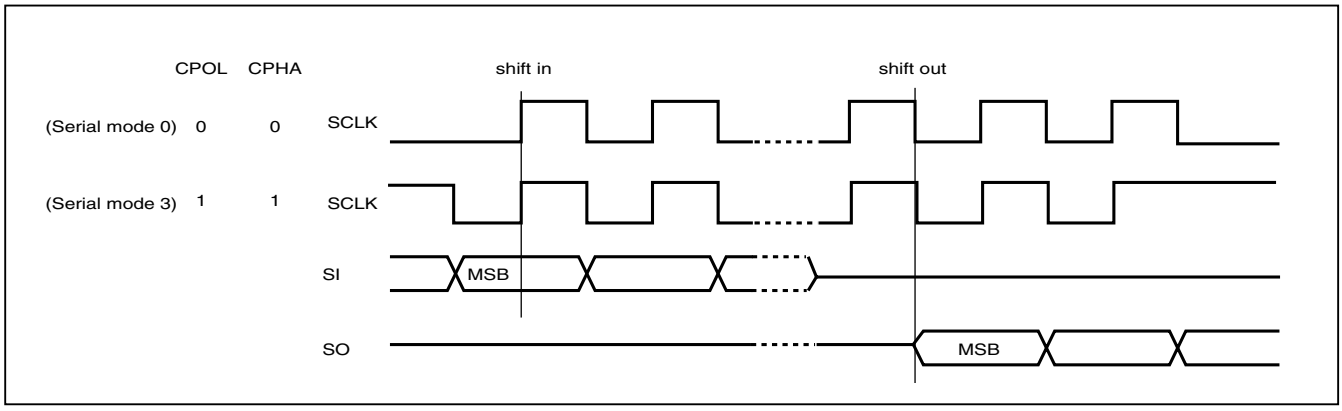
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock(SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported (for Normal Serial mode)"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 4READ, QREAD, 2READ, DREAD, RDCR, RES, and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, CE, PP, 4PP, Suspend, Resume, NOP, RSTEN, RST, ENSO, EXSO, WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



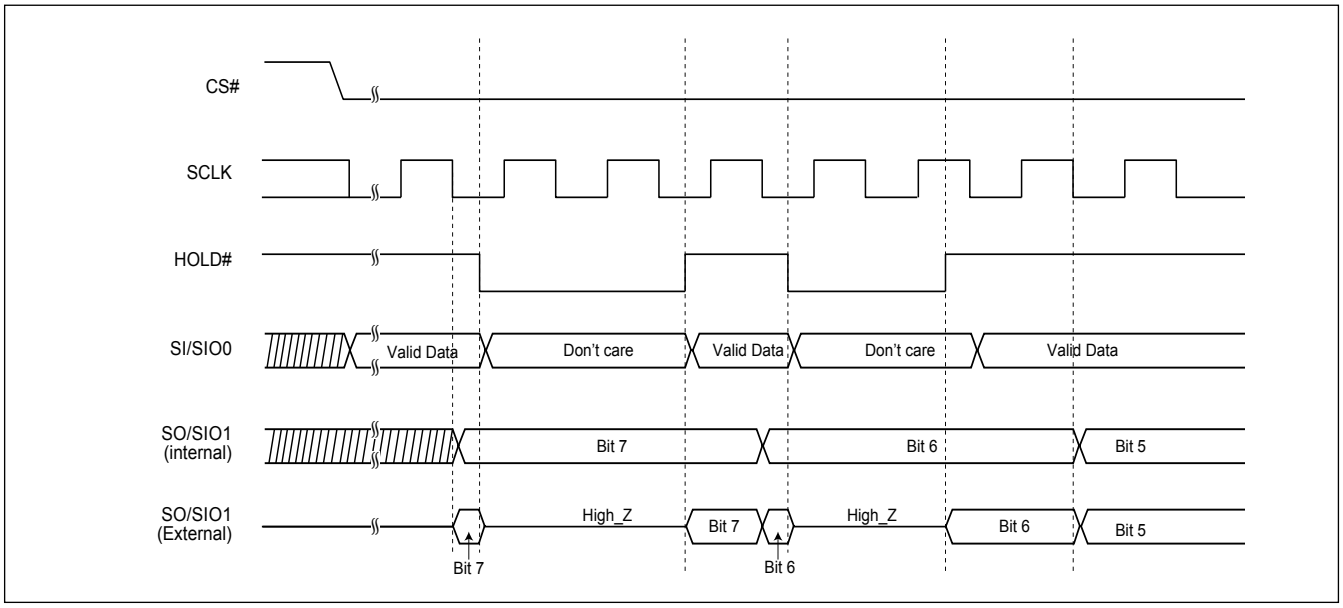
Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

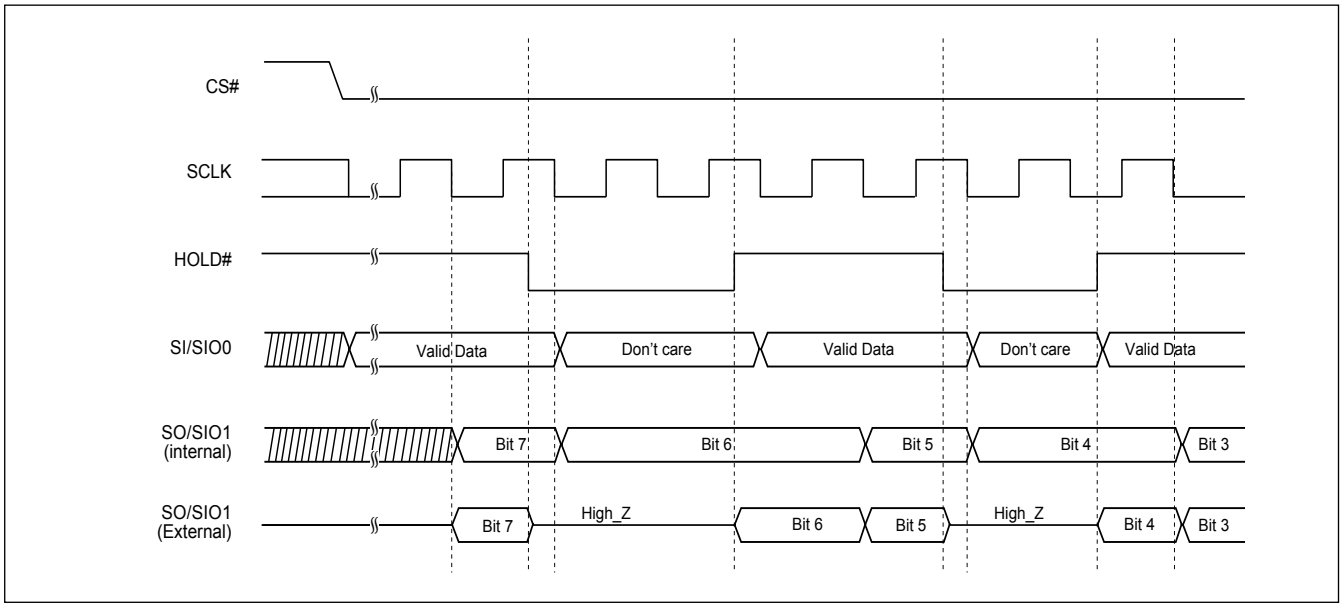
9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 2. Hold Condition Operation





During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

10. COMMAND DESCRIPTION

Table 4. Command Sets

Read Commands

I/O	1	1	2	2	4	4
Command	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	4READ (4 x I/O read command)	QREAD (1I/4O read command)
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	A[23:16]	A[23:16]	A[23:16]	A[23:16]	A[23:16]	A[23:16]
3rd byte	A[15:8]	A[15:8]	A[15:8]	A[15:8]	A[15:8]	A[15:8]
4th byte	A[7:0]	A[7:0]	A[7:0]	A[7:0]	A[7:0]	A[7:0]
5th byte		Dummy(8)	Dummy*	Dummy(8)	Dummy*	Dummy(8)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual Output until CS# goes high	Quad I/O read with configurable dummy cycles	

Note: *Dummy cycle number will be different, depending on the bit6 (DC) setting of Configuration Register. Please refer to *"Table 6. Configuration Register"*.

Other Commands

Command	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	4PP (quad page program)	SE (sector erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	38 (hex)	20 (hex)
2nd byte					Values	A[23:16]	A[23:16]
3rd byte					Values	A[15:8]	A[15:8]
4th byte						A[7:0]	A[7:0]
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the configuration/ status register	quad input to program the selected page	to erase the selected sector

Command	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)	PP (page program)	DP (Deep power down)	RDP (Release from deep power down)	PGM/ERS Suspend (Suspends Program/ Erase)
1st byte	52 (hex)	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	75/B0 (hex)
2nd byte	A[23:16]	A[23:16]		A[23:16]			
3rd byte	A[15:8]	A[15:8]		A[15:8]			
4th byte	A[7:0]	A[7:0]		A[7:0]			
Action	to erase the selected 32KB block	to erase the selected 64KB block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode	program/erase operation is interrupted by suspend command

Command	PGM/ERS Resume (Resumes Program/ Erase)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO (enter secured OTP)
1st byte	7A/30 (hex)	9F (hex)	AB (hex)	90 (hex)	B1 (hex)
2nd byte			x	x	
3rd byte			x	x	
4th byte			x	ADD	
Action	to continue performing the suspended program/erase sequence	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode

Command (byte)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	RSTEN (Reset Enable)	RST (Reset Memory)	RDSFDP	SBL (Set Burst Length)
1st byte	C1 (hex)	2B (hex)	2F (hex)	66 (hex)	99 (hex)	5A (hex)	C0/77 (hex)
2nd byte						A[23:16]	
3rd byte						A[15:8]	Value
4th byte						A[7:0]	
5th byte						Dummy(8)	
Action	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)		*(Note 2)*	n bytes read out until CS# goes high	to set Burst length

Command (byte)	NOP (No Operation)
1st byte	00 (hex)
2nd byte	
3rd byte	
4th byte	
5th byte	
Action	

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 2: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

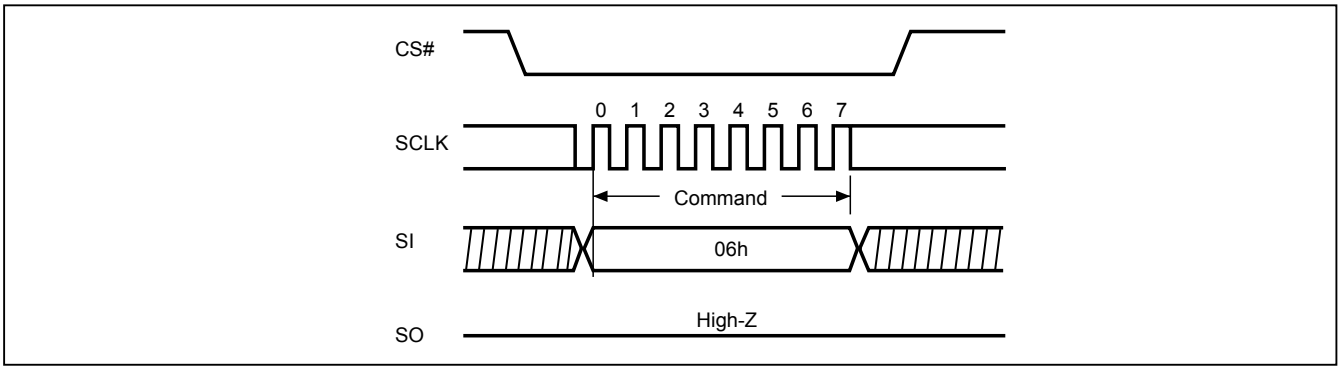
10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE, BE32K, CE, and WRSR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

The SIO[3:1] are don't care.

Figure 3. Write Enable (WREN) Sequence (Command 06h)

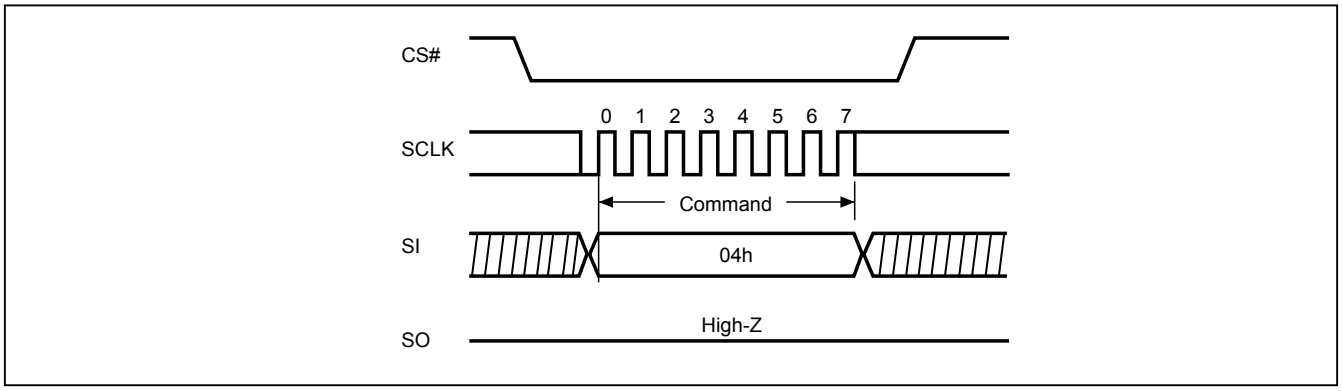


10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:
- Power-up
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion

Figure 4. Write Disable (WRDI) Sequence (Command 04h)



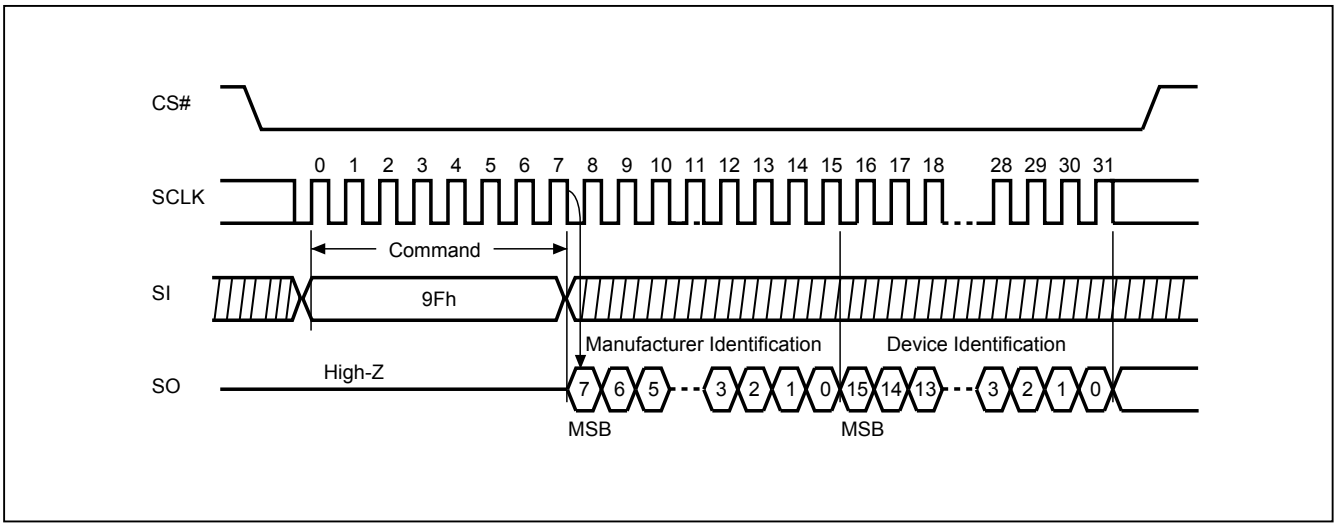
10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as table of *"Table 9. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 5. Read Identification (RDID) Sequence (Command 9Fh)



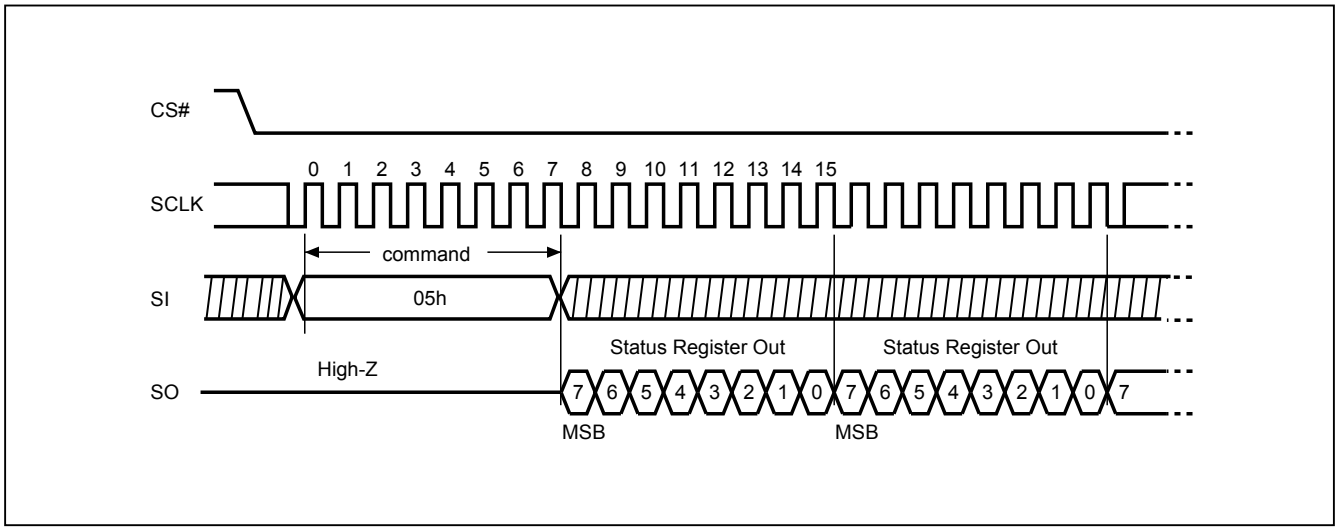
10-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

The SIO[3:1] are don't care.

Figure 6. Read Status Register (RDSR) Sequence (Command 05h)



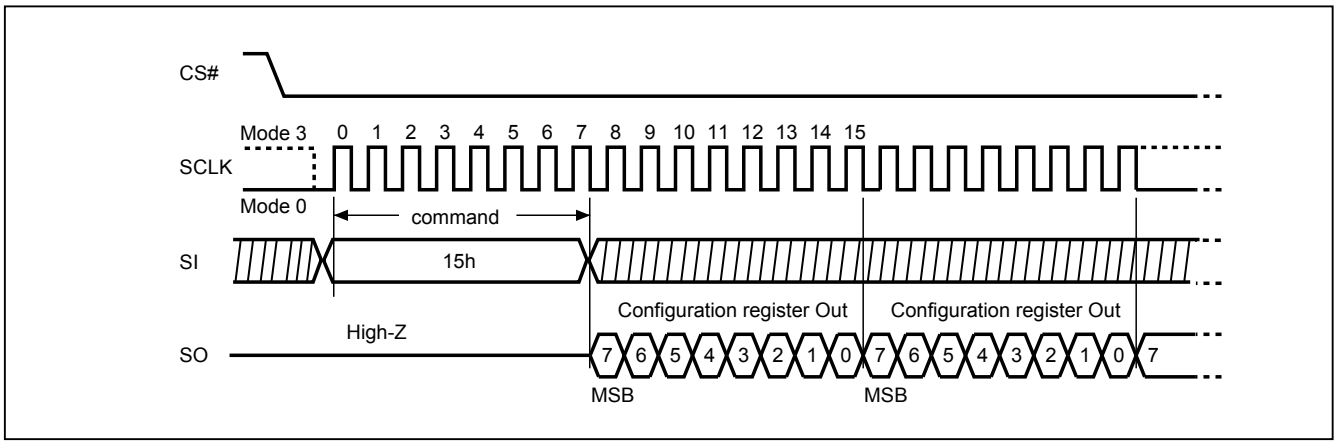
10-5. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

The SIO[3:1] are don't care.

Figure 7. Read Configuration Register (RDCR) Sequence



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to "1" by the WREN instruction. WEL needs to be set to "1" before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to "0" when a program or erase operation completes. To ensure that both WIP and WEL are "0" and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be "0" before checking that WEL is also "0". If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to "0".

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 1. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit is a non-volatile bit with a factory default of "0". When QE is "0", Quad mode commands are ignored; pins WP#/SIO2 and HOLD#/SIO3 function as WP# and HOLD#, respectively. When QE is "1", Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands. Pins WP#/SIO2 and HOLD#/SIO3 function as SIO2 and SIO3, respectively, and their alternate pin functions are disabled. Enabling Quad mode also disables the HPM and HOLD features.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 5. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	1= Quad Enable 0=not Quad Enable	*(note 1)*	*(note 1)*	*(note 1)*	*(note 1)*	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to the *"Table 1. Protected Area Sizes"*.

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit

The output driver strength ODS bit are volatile bits, which indicate the output driver level of the device. The Output Driver Strength is defaulted=1 when delivered from factory. To write the ODS bit requires the Write Status Register (WRSR) instruction to be executed.

TB bit

The Top/Bottom (TB) bit is a OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bit requires the Write Status Register (WRSR) instruction to be executed.

Table 6. Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	DC (Dummy Cycle)	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	ODS
x	2READ/ 4READ Dummy Cycle	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	0, Output driver strength=1 1, Output driver strength=1/4 (Default=0)
x	volatile	x	x	OTP	x	x	volatile

Note: Refer to *"Table 7. Dummy Cycle and Frequency Table"*, with "Don't Care" on other Reserved Configuration Registers.

Table 7. Dummy Cycle and Frequency Table

	DC	Numbers of Dummy Cycles	Freq. (MHz)
2READ	0 (default)	4	104
	1	8	133
4READ	0 (default)	6	104
	1	10	133