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# MX25L3239E

# HIGH PERFORMANCE

# SERIAL FLASH SPECIFICATION

# Contents

## 32M-BIT [x 1 / x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

# 1. FEATURES

### GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 33,554,432 x 1 bit structure or 8,388,608 x 4 bits (four I/O mode) structure
- 1024 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 128 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 64 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

### PERFORMANCE

- High Performance
  VCC = 2.7~3.6V
  - Normal read
    - 50MHz
  - Fast read
    - 1 I/O: 104MHz with 8 dummy cycles
    - 4 I/O: Up to 104MHz
    - Configurable dummy cycle number for 4 I/O read operation
  - Fast read (QPI Mode)
    - 4 I/O: 54MHz with 4 dummy cycles
    - 4 I/O: 86MHz with 6 dummy cycles
    - 4 I/O: 104MHz with 8 dummy cycles
  - Fast program time: 0.7ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 12us (typical)
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
  - Fast erase time: 30ms (typ.)/sector (4K-byte per sector) ; 0.25s(typ.) /block (64K-byte per block); 10s(typ.) / chip
- Low Power Consumption
  - Low active read current: 19mA(max.) at 104MHz, 10mA(max.) at 33MHz
  - Low active programming current: 15mA (typ.)
  - Low active sector erase current: 10mA (typ.)
  - Low standby current: 15uA (typ.)
  - Deep Power-down current: 1uA (typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

## SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - BP0-BP3 block group protect
  - Flexible individual block protect when OTP WPSEL=1
  - Additional 4K bits secured OTP for unique identifier
- Auto Erase and Auto Program Algorithms
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Program/Erase Resume
- Electronic Identification
  - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
  - RES command for 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

## HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 4 x I/O mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 4 x I/O mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O mode
- HOLD#/SIO3
  - To pause the device without deselecting the device or serial data Input/Output for 4 x I/O mode
- PACKAGE
  - 8-pin SOP (200mil)
  - 8-pin VSOP (200mil)
  - 8-WSON (6x5mm)
  - **All devices are RoHS Compliant and Halogen-free**

## 2. GENERAL DESCRIPTION

MX25L3239E is 32Mb bits serial Flash memory, which is configured as 4,194,304 x 8 internally. When it is in four I/O mode, the structure becomes 8,388,608 bits x 4. MX25L3239E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L3239E, MXSMIO® (Serial Multi I/O) flash memory, provides sequential read operation on whole chip and multi-I/O features.

When it is in quad I/O mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, and erase command is executed on sector (4K-byte), block (32K-byte/64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25L3239E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

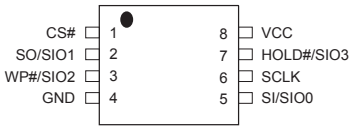
**Table 1. Additional Features**

| Numbers of Dummy Cycles | 4 I/O |
|---|---|
| 6 | 86* |
| 8 | 104 |

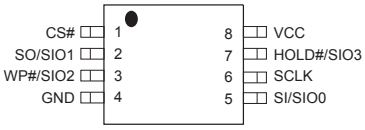
**Note:** *means default status

## 3. PIN CONFIGURATION

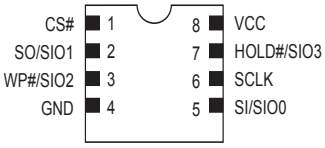
### 8-PIN SOP (200mil)




### 8-PIN VSOP (200mil)




### 8-WSON (6x5mm)

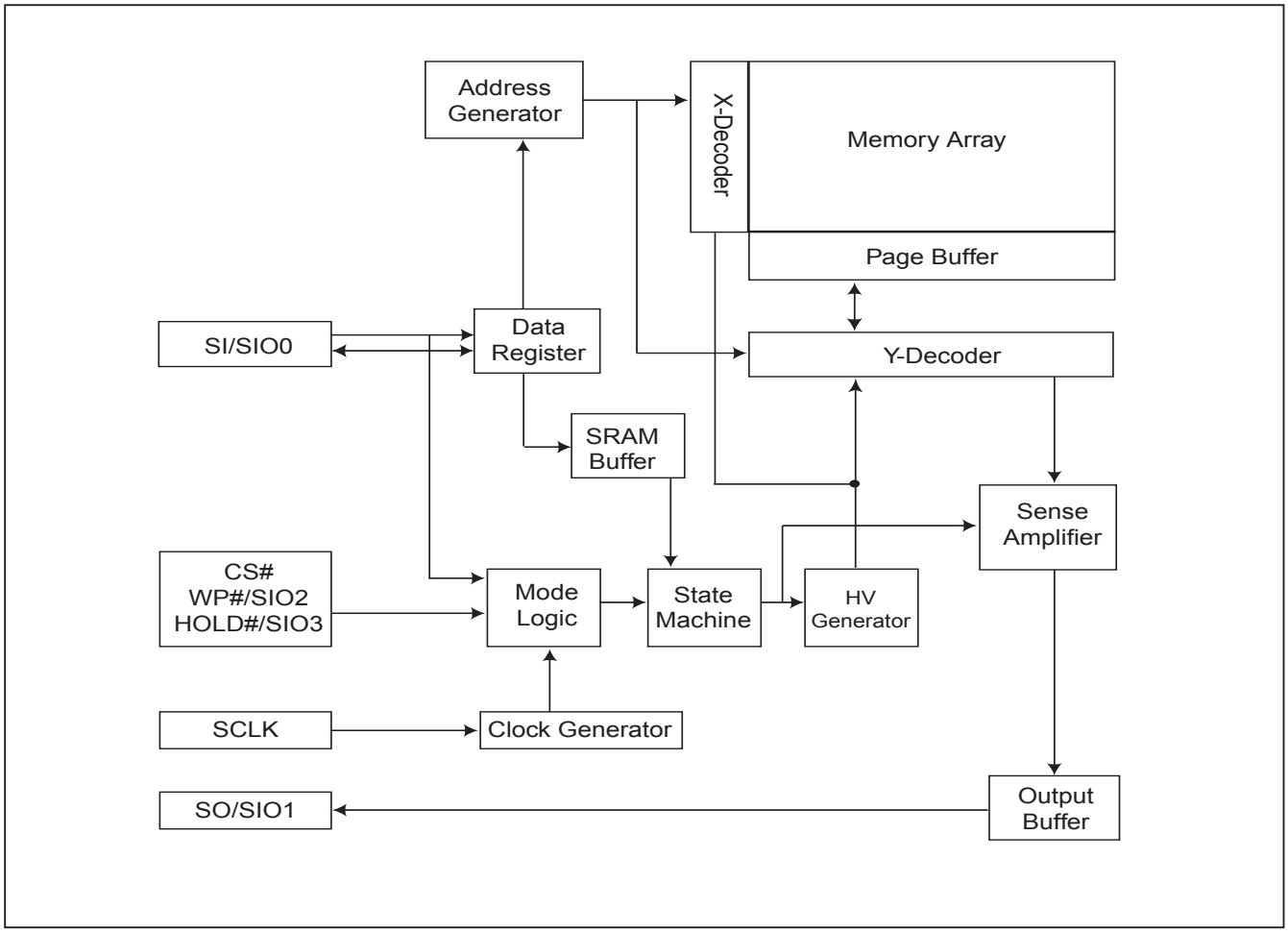



## 4. PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| CS# | Chip Select |
| SI/SIO0 | Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 4xI/O mode) |
| SO/SIO1 | Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 4xI/O mode) |
| SCLK | Clock Input |
| WP#/SIO2 | Write protection or Serial Data Input & Output (for 4xI/O mode) |
| HOLD#/ SIO3 | To pause the device without deselecting the device or Serial data Input/Output for 4 x I/O mode |
| VCC | + 3.0V Power Supply |
| GND | Ground |

**Note:**
1. The HOLD# pin is internal pull high.

## 5. BLOCK DIAGRAM



## 6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

**I. Block lock protection**

- The Software Protected Mode (SPM) uses (TB, BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various areas by setting value of TB, BP0-BP3 bits.

- The Hardware Protected Mode (HPM) uses WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O or QPI mode, the feature of HPM will be disabled.

- MX25L3239E provides individual block (or sector) write protect & unprotect. User may enter the mode with WPSEL command and conduct individual block (or sector) write protect with SBLK instruction, or SBULK for individual block (or sector) unprotect. Under the mode, user may conduct whole chip (all blocks) protect with GBLK instruction and unlock the whole chip with GBULK instruction.

**Table 2. Protected Area Sizes**

**Protected Area Sizes (TB bit = 0)**

| Status bit | | | | Protect Level |
|---|---|---|---|---|
| BP3 | BP2 | BP1 | BP0 | 32Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1block, block 63rd) |
| 0 | 0 | 1 | 0 | 2 (2blocks, block 62nd-63rd) |
| 0 | 0 | 1 | 1 | 3 (4blocks, block 60th-63rd) |
| 0 | 1 | 0 | 0 | 4 (8blocks, block 56th-63rd) |
| 0 | 1 | 0 | 1 | 5 (16blocks, block 48th-63rd) |
| 0 | 1 | 1 | 0 | 6 (32blocks, block 32nd-63rd) |
| 0 | 1 | 1 | 1 | 7 (64blocks, protect all) |
| 1 | 0 | 0 | 0 | 8 (64blocks, protect all) |
| 1 | 0 | 0 | 1 | 9 (64blocks, protect all) |
| 1 | 0 | 1 | 0 | 10 (64blocks, protect all) |
| 1 | 0 | 1 | 1 | 11 (64blocks, protect all) |
| 1 | 1 | 0 | 0 | 12 (64blocks, protect all) |
| 1 | 1 | 0 | 1 | 13 (64blocks, protect all) |
| 1 | 1 | 1 | 0 | 14 (64blocks, protect all) |
| 1 | 1 | 1 | 1 | 15 (64blocks, protect all) |

**Protected Area Sizes (TB bit = 1)**

| Status bit | | | | Protect Level |
|---|---|---|---|---|
| BP3 | BP2 | BP1 | BP0 | 32Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1block, block 0th) |
| 0 | 0 | 1 | 0 | 2 (2blocks, block 0th-1st) |
| 0 | 0 | 1 | 1 | 3 (4blocks, block 0th-3rd) |
| 0 | 1 | 0 | 0 | 4 (8blocks, block 0th-7th) |
| 0 | 1 | 0 | 1 | 5 (16blocks, block 0th-15th) |
| 0 | 1 | 1 | 0 | 6 (32blocks, block 0th-31st) |
| 0 | 1 | 1 | 1 | 7 (64blocks, protect all) |
| 1 | 0 | 0 | 0 | 8 (64blocks, protect all) |
| 1 | 0 | 0 | 1 | 9 (64blocks, protect all) |
| 1 | 0 | 1 | 0 | 10 (64blocks, protect all) |
| 1 | 0 | 1 | 1 | 11 (64blocks, protect all) |
| 1 | 1 | 0 | 0 | 12 (64blocks, protect all) |
| 1 | 1 | 0 | 1 | 13 (64blocks, protect all) |
| 1 | 1 | 1 | 0 | 14 (64blocks, protect all) |
| 1 | 1 | 1 | 1 | 15 (64blocks, protect all) |

**Note:** The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

**II. Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of *"Table 8. Security Register Definition"* for security register bit definition and table of *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

**Note:** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

**Table 3. 4K-bit Secured OTP Definition**

| Address range | Size | Standard Factory Lock | Customer Lock |
|---|---|---|---|
| xxx000~xxx00F | 128-bit | ESN (electrical serial number) | Determined by customer |
| xxx010~xxx1FF | 3968-bit | N/A | |

## 7. MEMORY ORGANIZATION

### Table 4. Memory Organization

| Block(64K-byte) | Block(32K-byte) | Sector (4K-byte) | Address Range | |
|---|---|---|---|---|
| 63 | 127 | 1023 | 3FF000h | 3FFFFFh |
| | | ⋮ | | |
| | | 1016 | 3F8000h | 3F8FFFh |
| | 126 | 1015 | 3F7000h | 3F7FFFh |
| | | ⋮ | | |
| | | 1008 | 3F0000h | 3F0FFFh |
| 62 | 125 | 1007 | 3EF000h | 3EFFFFh |
| | | ⋮ | | |
| | | 1000 | 3E8000h | 3E8FFFh |
| | 124 | 999 | 3E7000h | 3E7FFFh |
| | | ⋮ | | |
| | | 992 | 3E0000h | 3E0FFFh |
| 61 | 123 | 991 | 3DF000h | 3DFFFFh |
| | | ⋮ | | |
| | | 984 | 3D8000h | 3D8FFFh |
| | 122 | 983 | 3D7000h | 3D7FFFh |
| | | ⋮ | | |
| | | 976 | 3D0000h | 3D0FFFh |
| 2 | 5 | 47 | 02F000h | 02FFFFh |
| | | ⋮ | | |
| | | 40 | 028000h | 028FFFh |
| | 4 | 39 | 027000h | 027FFFh |
| | | ⋮ | | |
| | | 32 | 020000h | 020FFFh |
| 1 | 3 | 31 | 01F000h | 01FFFFh |
| | | ⋮ | | |
| | | 24 | 018000h | 018FFFh |
| | 2 | 23 | 017000h | 017FFFh |
| | | ⋮ | | |
| | | 16 | 010000h | 010FFFh |
| 0 | 1 | 15 | 00F000h | 00FFFFh |
| | | ⋮ | | |
| | | 8 | 008000h | 008FFFh |
| | 0 | 7 | 007000h | 007FFFh |
| | | ⋮ | | |
| | | 0 | 000000h | 000FFFh |

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

## 8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

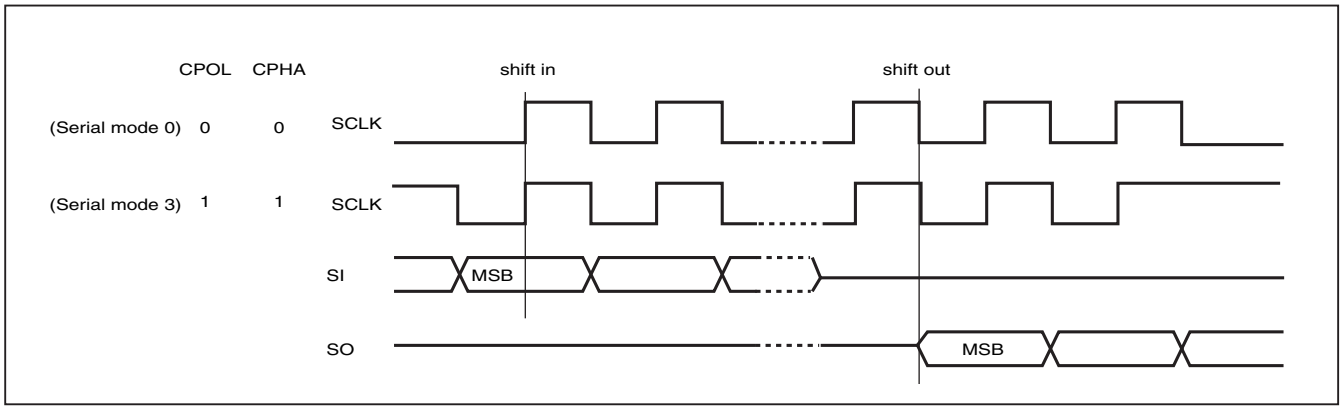
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported (for Normal Serial mode)"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, W4READ, 4READ, QREAD, RDBLOCK, RES, and QPIID, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, CE, PP, 4PP, WPSEL, SBLK, SBULK, GBLK, GBULK, Suspend, Resume, NOP, RSTEN, RST, EQIO, RSTQIO, ENSO, EXSO, WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

**Figure 1. Serial Modes Supported (for Normal Serial mode)**



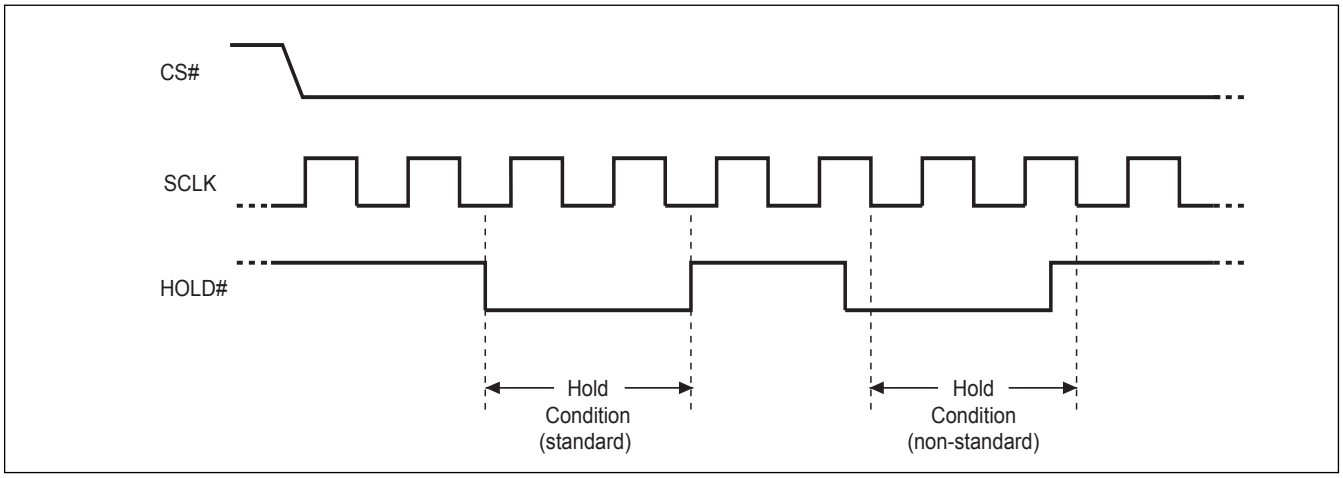

**Note:**
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

## 9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low( if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

**Figure 2. Hold Condition Operation**




The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

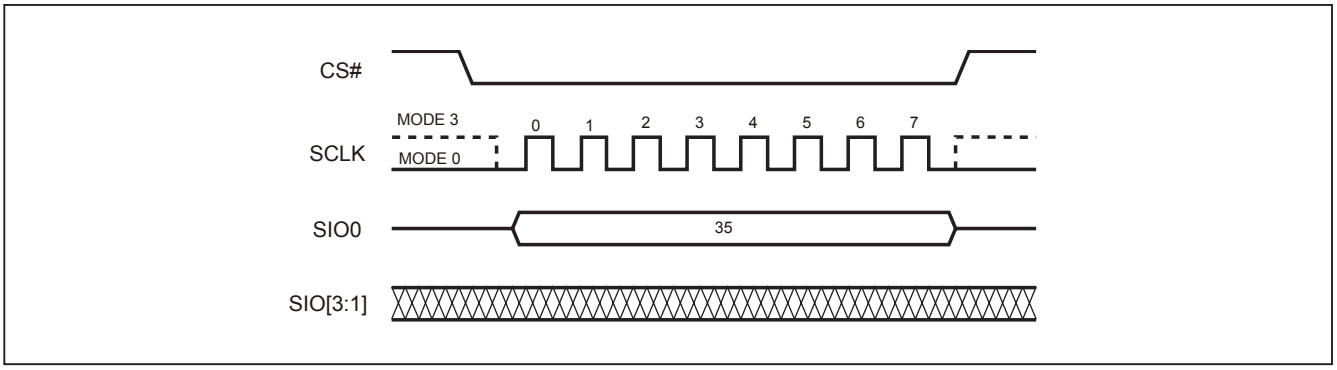
## 10. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

### 10-1. Enable QPI mode

By issuing 35H command, the QPI mode is enable.

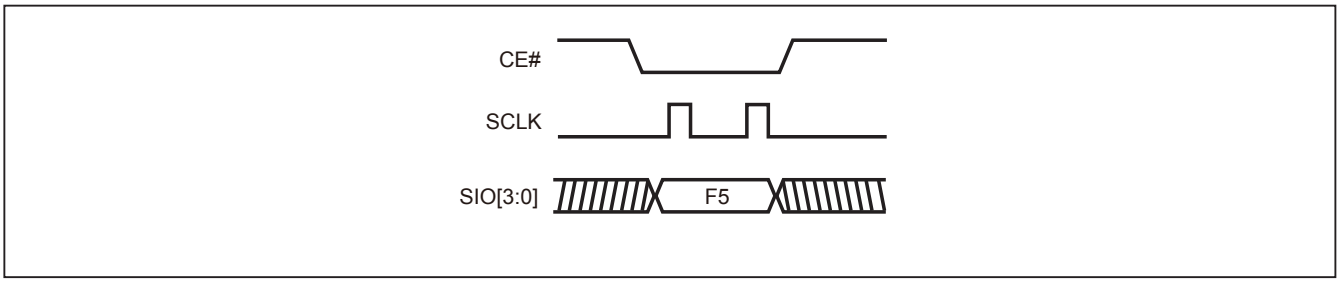
**Figure 3. Enable QPI Sequence (Command 35H)**




### 10-2. Reset QPI mode

By issuing F5H command, the device is reset to 1-I/O SPI mode.

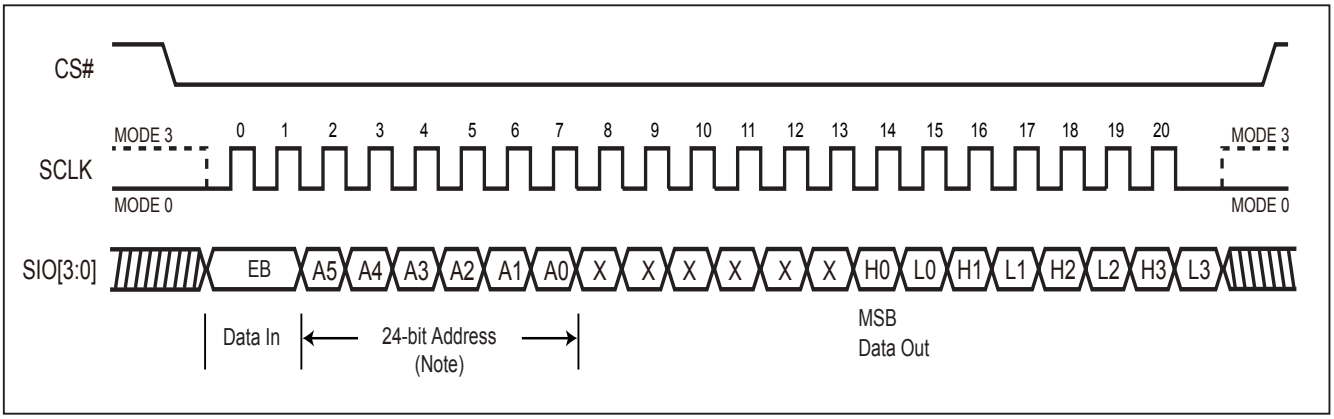
**Figure 4. Reset QPI Mode (Command F5H)**



### 10-3. Fast QPI Read mode (FASTRDQ)

To increase the code transmission speed, the device provides a "Fast QPI Read Mode" (FASTRDQ). By issuing command code EBH, the FASTRDQ mode is enable. The number of dummy cycle increase from 4 to 6 cycles. The read cycle frequency will increase from 54MHz to 86MHz.

**Figure 5. Fast QPI Read Mode (FASTRDQ) (Command EBH)**



## 11. COMMAND DESCRIPTION

### Table 5. Command Sets

**Read Commands**

| I/O | 1 | 1 | 4 | 4 | 4 | 4 | 4 |
|---|---|---|---|---|---|---|---|
| Read Mode | SPI | SPI | SPI | SPI | SPI | QPI | QPI |
| Command | READ (normal read) | FAST READ (fast read data) | W4READ | 4READ (4 x I/O read command) | QREAD (1I/4O read command) | FAST READ (fast read data) | 4READ (4 x I/O read command) |
| 1st byte | 03 (hex) | 0B (hex) | E7 (hex) | EB (hex) | 6B (hex) | 0B (hex) | EB (hex) |
| 2nd byte | ADD1(8) | ADD1(8) | ADD1(2) | ADD1(2) | ADD1(8) | ADD1(2) | ADD1(2) |
| 3rd byte | ADD2(8) | ADD2(8) | ADD2(2) | ADD2(2) | ADD2(8) | ADD2(2) | ADD2(2) |
| 4th byte | ADD3(8) | ADD3(8) | ADD3(2) | ADD3(2) | ADD3(8) | ADD3(2) | ADD3(2) |
| 5th byte | | Dummy(8) | Dummy(4) | Dummy* | Dummy(8) | Dummy(4) | Dummy* |
| Action | n bytes read out until CS# goes high | n bytes read out until CS# goes high | Quad I/O read with 4 dummy cycles | Quad I/O read with configurable dummy cycles | | n bytes read out until CS# goes high | Quad I/O read with configurable dummy cycles |

**Note:** *Dummy cycle number will be different, depending on the bit7 (DC) setting of Configuration Register. Please refer to *"Configuration Register"* Table.

## Other Commands

| Command | WREN* (write enable) | WRDI * (write disable) | RDSR * (read status register) | RDCR* (read configuration register) | WRSR* (write status/ configuration register) | 4PP (quad page program) | SE * (sector erase) |
|---|---|---|---|---|---|---|---|
| 1st byte | 06 (hex) | 04 (hex) | 05 (hex) | 15 (hex) | 01 (hex) | 38 (hex) | 20 (hex) |
| 2nd byte | | | | | Values | ADD1 | ADD1 |
| 3rd byte | | | | | Values | ADD2 | ADD2 |
| 4th byte | | | | | | ADD3 | ADD3 |
| Action | sets the (WEL) write enable latch bit | resets the (WEL) write enable latch bit | to read out the values of the status register | to read out the values of the configuration register | to write new values of the configuration/ status register | quad input to program the selected page | to erase the selected sector |

| Command | BE 32K * (block erase 32KB) | BE * (block erase 64KB) | CE * (chip erase) | PP * (page program) | DP (Deep power down) | RDP (Release from deep power down) | PGM/ERS Suspend * (Suspends Program/ Erase) |
|---|---|---|---|---|---|---|---|
| 1st byte | 52 (hex) | D8 (hex) | 60 or C7 (hex) | 02 (hex) | B9 (hex) | AB (hex) | 75 (hex) |
| 2nd byte | ADD1 | ADD1 | | ADD1 | | | |
| 3rd byte | ADD2 | ADD2 | | ADD2 | | | |
| 4th byte | ADD3 | ADD3 | | ADD3 | | | |
| Action | to erase the selected 32KB block | to erase the selected 64KB block | to erase whole chip | to program the selected page | enters deep power down mode | release from deep power down mode | program/erase operation is interrupted by suspend command |

| Command | PGM/ERS Resume * (Resumes Program/ Erase) | RDID (read identific-ation) | RES * (read electronic ID) | ENSO * (enter secured OTP) |
|---|---|---|---|---|
| 1st byte | 7A (hex) | 9F (hex) | AB (hex) | B1 (hex) |
| 2nd byte | | | x | |
| 3rd byte | | | x | |
| 4th byte | | | x | |
| Action | to continue performing the suspended program/erase sequence | outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID | to read out 1-byte Device ID | to enter the 4K-bit secured OTP mode |

| Command (byte) | EXSO * (exit secured OTP) | RDSCUR * (read security register) | WRSCUR * (write security register) | SBLK * (single block lock | SBULK * (single block unlock) | RDBLOCK * (block protect read) | GBLK * (gang block lock) |
|---|---|---|---|---|---|---|---|
| 1st byte | C1 (hex) | 2B (hex) | 2F (hex) | 36 (hex) | 39 (hex) | 3C (hex) | 7E (hex) |
| 2nd byte | | | | ADD1 | ADD1 | ADD1 | |
| 3rd byte | | | | ADD2 | ADD2 | ADD2 | |
| 4th byte | | | | ADD3 | ADD3 | ADD3 | |
| Action | to exit the 4K-bit secured OTP mode | to read value of security register | to set the lock-down bit as "1" (once lock-down, cannot be update) | individual block (64K-byte) or sector (4K-byte) write protect | individual block (64K-byte) or sector (4K-byte) unprotect | read individual block or sector write protect status | whole chip write protect |

| COMMAND (byte) | GBULK * (gang block unlock) | NOP * (No Operation) | RSTEN * (Reset Enable) | RST * (Reset Memory) | EQIO (Enable Quad I/O) | RSTQIO (Reset Quad I/O) | QPIID (QPI ID Read) |
|---|---|---|---|---|---|---|---|
| 1st byte | 98 (hex) | 00 (hex) | 66 (hex) | 99 (hex) | 35 (hex) | F5 (hex) | AF (hex) |
| 2nd byte | | | | | | | |
| 3rd byte | | | | | | | |
| 4th byte | | | | | | | |
| Action | whole chip unprotect | | | | Entering the QPI mode | Exiting the QPI mode | ID in QPI interface |

| COMMAND (byte) | SBL * (Set Burst Length) | WPSEL * (Write Protect Selection) | RDSFDP * |
|---|---|---|---|
| 1st byte | 77 (hex) | 68 (hex) | 5A (hex) |
| 2nd byte | Value | | ADD1(8) |
| 3rd byte | | | ADD2(8) |
| 4th byte | | | ADD3(8) |
| 5th byte | | | Dummy(8) |
| Action | to set Burst length | to enter and enable individal block protect mode | n bytes read out until CS# goes high |

Note 1: Command set highlighted with (*) are supported both in SPI and QPI mode.
Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 3: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

### 11-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE, BE32K, CE, WRSR, SBLK, SBULK, GBLK and GBULK, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

**Figure 6. Write Enable (WREN) Sequence (Command 06) (SPI Mode)**

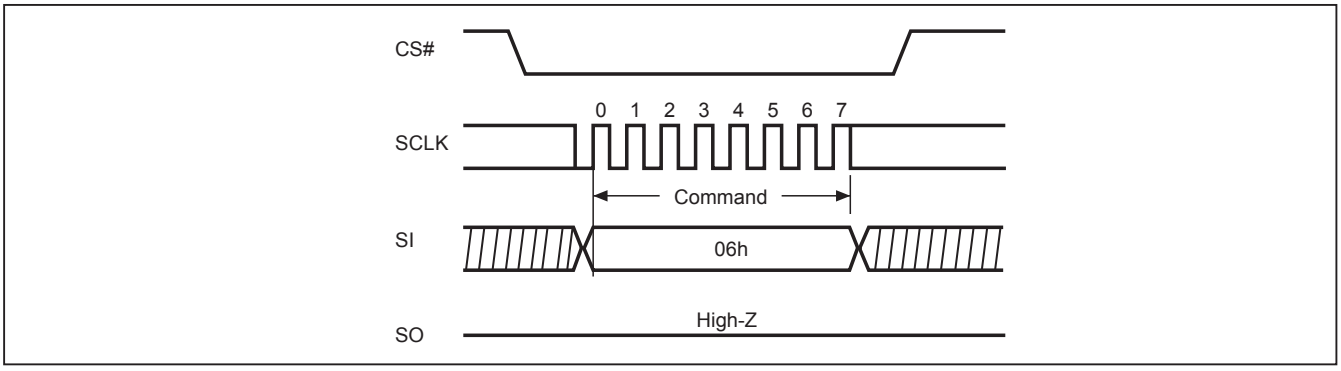
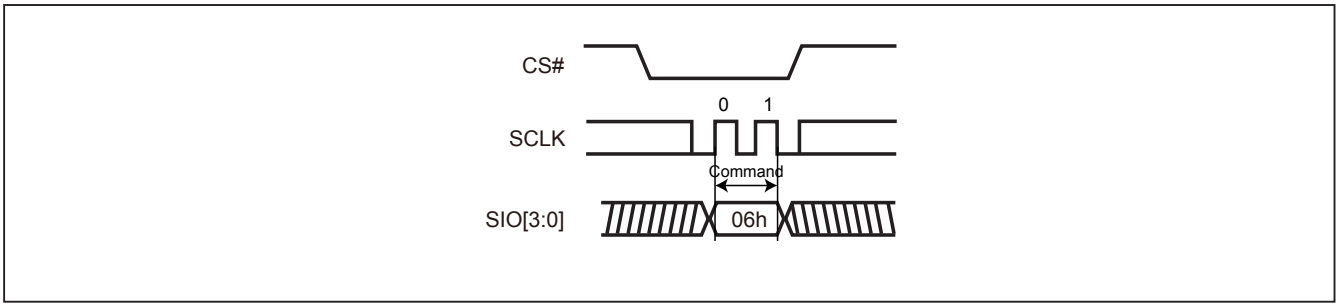



**Figure 7. Write Enable (WREN) Sequence (Command 06) (QPI Mode)**



### 11-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:
- Power-up
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- SBLK command completion
- SBULK command completion
- GBLK command completion
- GBULK command completion

**Figure 8. Write Disable (WRDI) Sequence (Command 04) (SPI Mode)**

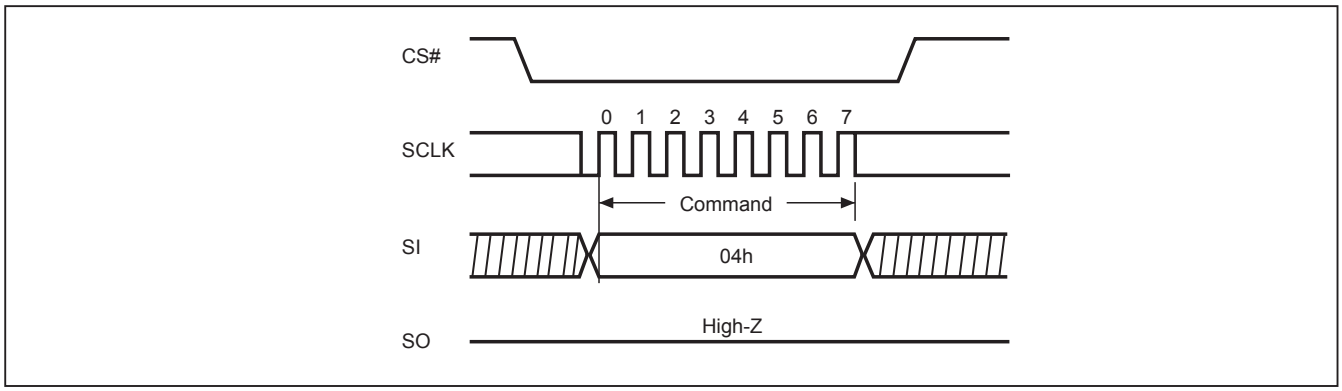
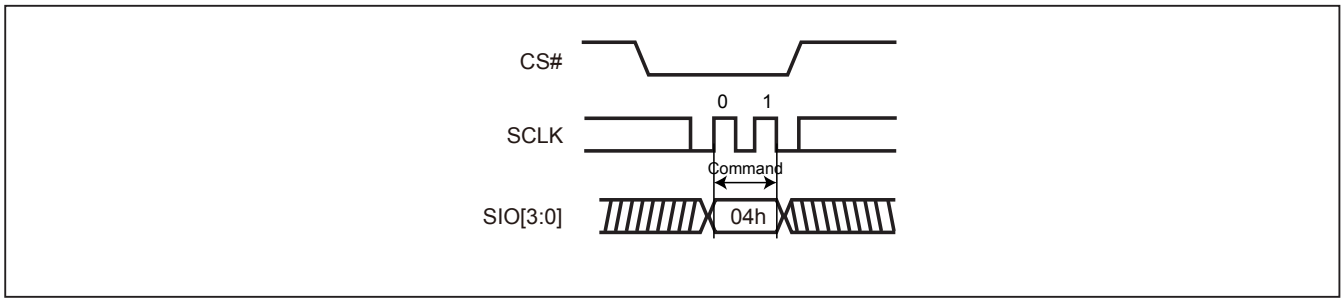



**Figure 9. Write Disable (WRDI) Sequence (Command 04) (QPI Mode)**



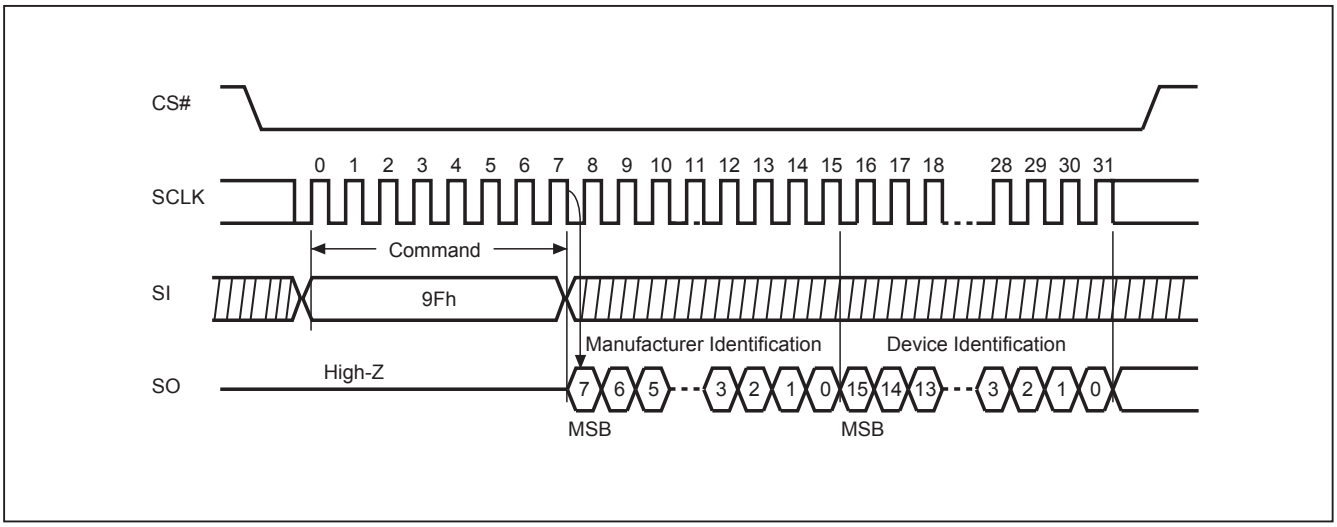
### 11-3. Read Identification (RDID)

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID is C2(hex), the memory type ID is 25(hex) as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of *"Table 7. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

**Figure 10. Read Identification (RDID) Sequence (Command 9F) (SPI mode only)**



### 11-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

**Figure 11. Read Status Register (RDSR) Sequence (Command 05) (SPI Mode)**

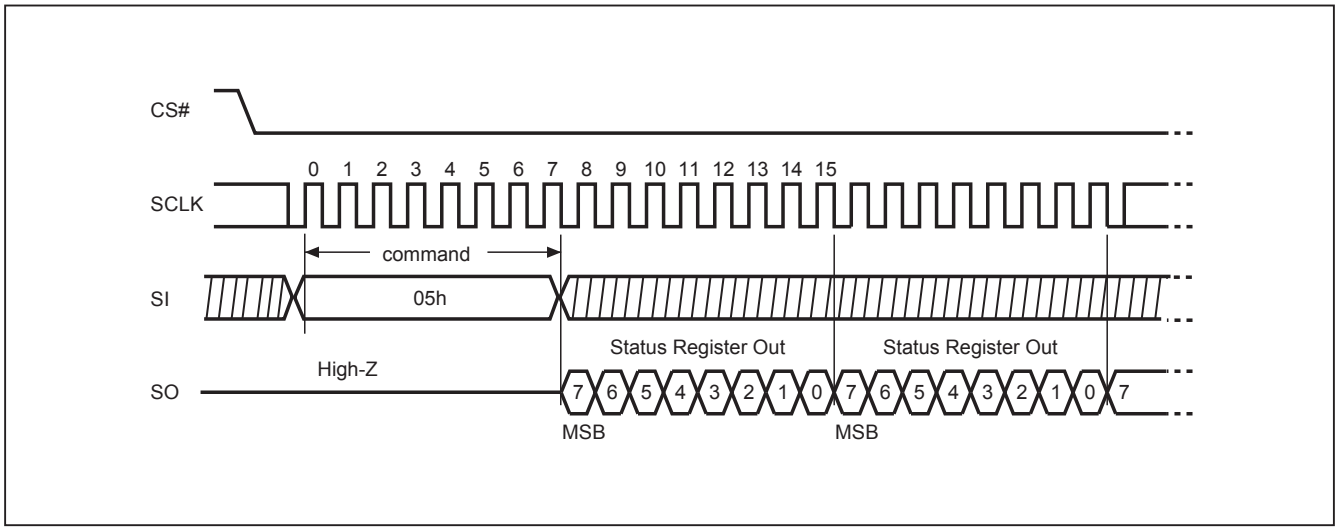
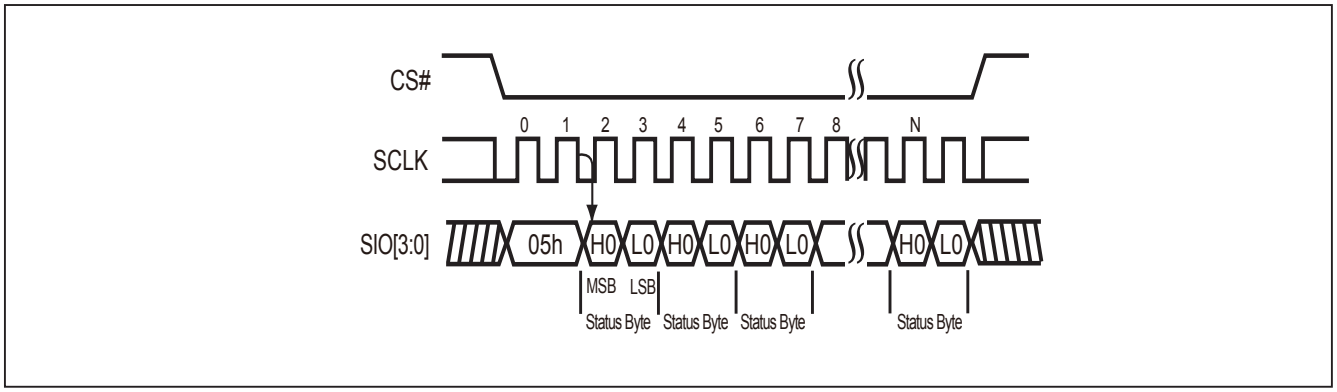



**Figure 12. Read Status Register (RDSR) Sequence (Command 05) (QPI Mode)**



### 11-5. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

**Figure 13. Read Configuration Register (RDCR) Sequence (SPI Mode)**

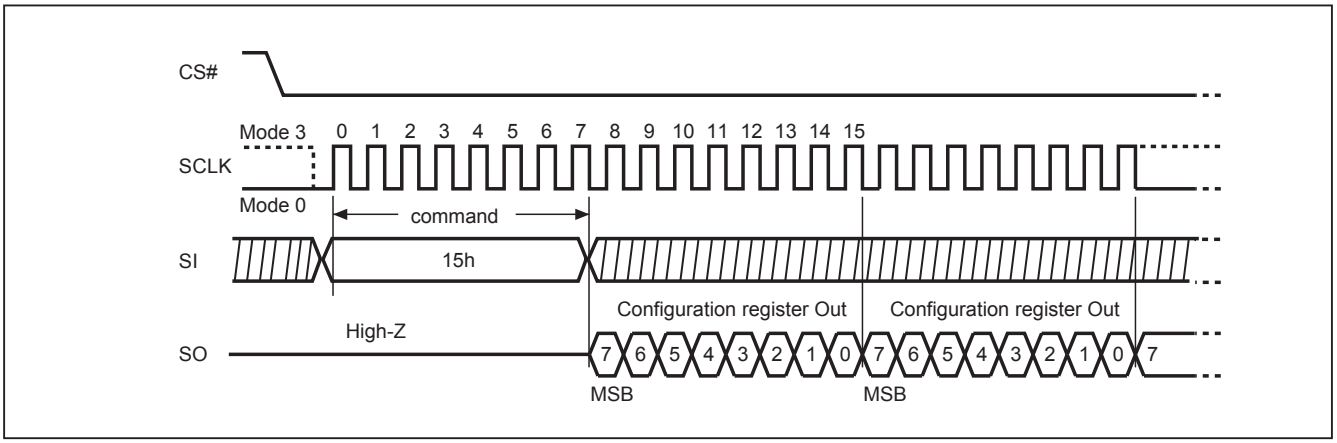
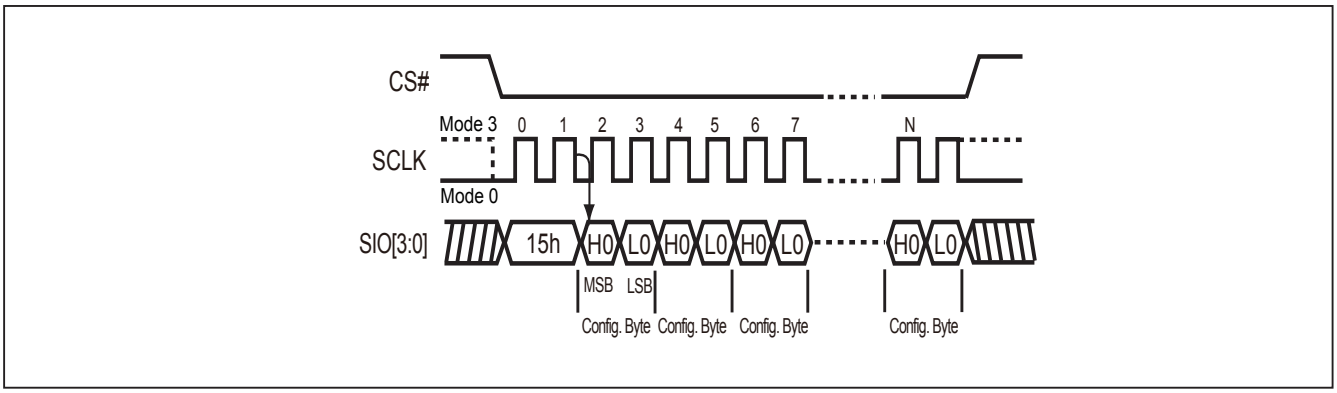



**Figure 14. Read Configuration Register (RDCR) Sequence (QPI Mode)**



### Status Register

The definition of the status register bits is as below:

**WIP bit.** The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

**WEL bit.** The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

**BP3, BP2, BP1, BP0 bits.** The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

**QE bit.** The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM will be disabled. While in QPI mode, QE bit is not required for setting.

**SRWD bit.** The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

**Status Register**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| SRWD (status register write protect) | QE (Quad Enable) | BP3 (level of protected block) | BP2 (level of protected block) | BP1 (level of protected block) | BP0 (level of protected block) | WEL (write enable latch) | WIP (write in progress bit) |
| 1=status register write disable | 1= Quad Enable 0=not Quad Enable | (note 1) | (note 1) | (note 1) | (note 1) | 1=write enable 0=not write enable | 1=write operation 0=not in write operation |
| Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

**Note:** see the *"Table 2. Protected Area Sizes"*.