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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MX25L512E

512K-BIT [x 1/x 2]
CMOS SERIAL NOR FLASH MEMORY

Key Features

- *Low Power Consumption*
- *2.7 to 3.6 volt for read, erase, and program operations*
- *Dual Output Mode (DREAD)*
- *Auto Erase and Auto Program Algorithm*
- *HOLD FEATURE*

Contents

512K-BIT [x 1/x 2] CMOS SERIAL FLASH

FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 524,288 x 1 bit structure or 262,144 x 2 bits (Dual Output mode) Structure
- 16 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast access time: 104MHz serial clock
  - Serial clock of Dual Output mode: 80MHz
  - Fast program time: 0.6ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 9us
  - Fast erase time: 40ms(typ.)/sector (4K-byte per sector); 0.4s(typ.) and 2s(max.)/chip
- Low Power Consumption
  - Low active read current: 12mA(max.) at 104MHz and 4mA(max.) at 33MHz
  - Low active programming current: 15mA (typ.)
  - Low active sector erase current: 9mA (typ.)
  - Low standby current: 15uA (typ.)
  - Deep power-down mode 2uA (typ.)
- Minimum 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Block Lock protection
  - The BP0~BP1 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 2-byte Device ID
  - RES command, 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Output for Dual output mode
- SO/SIO1
  - Serial Data Output or Serial Data Output for Dual output mode
- WP# pin
  - Hardware Write Protection
- HOLD# pin
  - Pause the chip without diselecting the chip
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-USON (2x3mm)
  - 8-pin TSSOP (173mil)
  - **All devices are RoHS Compliant and Halogen-free**

GENERAL DESCRIPTION

MX25L512E is a CMOS 524,288 bit serial Flash memory, which is configured as 65,536 x 8 internally. MX25L512E features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L512E provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector (4K-bytes).

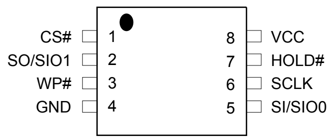
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

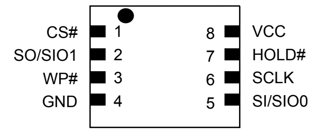
The MX25L512E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

PIN CONFIGURATIONS

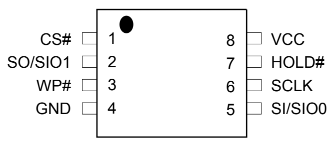
8-PIN SOP (150mil)



8-LAND USON (2x3mm)



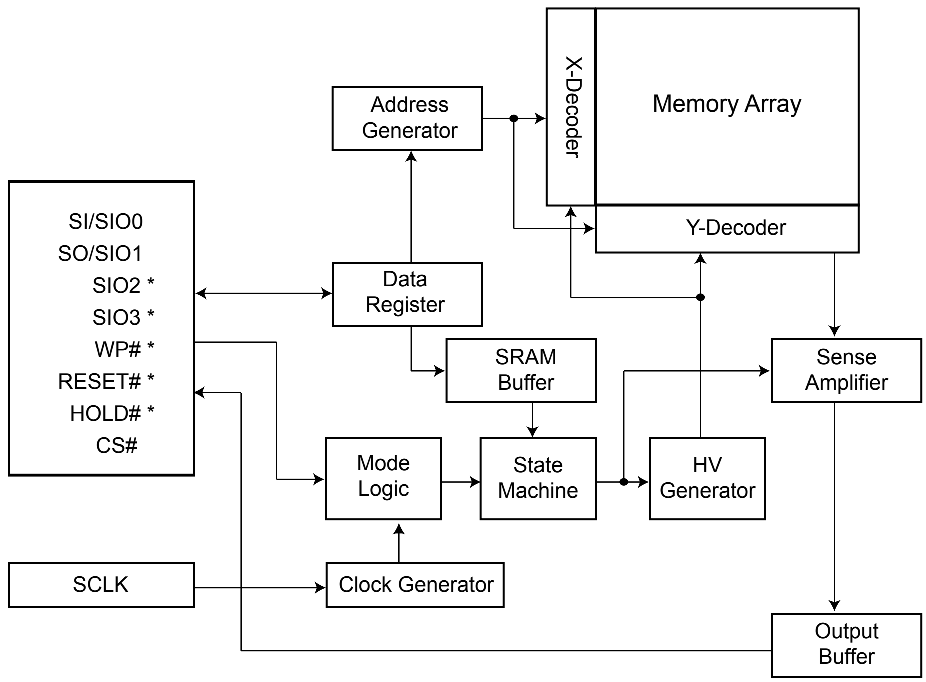
8-PIN TSSOP (173mil)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for Dual output mode)
SCLK	Clock Input
HOLD#	Hold, to pause the device without deselecting the device
WP#	Write Protection
VCC	+ 3.3V Power Supply
GND	Ground

BLOCK DIAGRAM



* Depends on part number options.

DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- **Valid command length checking:** The command length will be checked whether it is at byte base and completed on byte boundary.
- **Write Enable (WREN) command:** WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
- **Software Protection Mode (SPM):** by using BP0-BP1 bits to set the part of Flash protected from data change.
- **Hardware Protection Mode (HPM):** by using WP# going low to protect the BP0-BP1 bits and SRWD bit from data change.
- **Deep Power Down Mode:** By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power-down mode command (RDP) and Read Electronic Signature command (RES).

Table 1. Protected Area Sizes

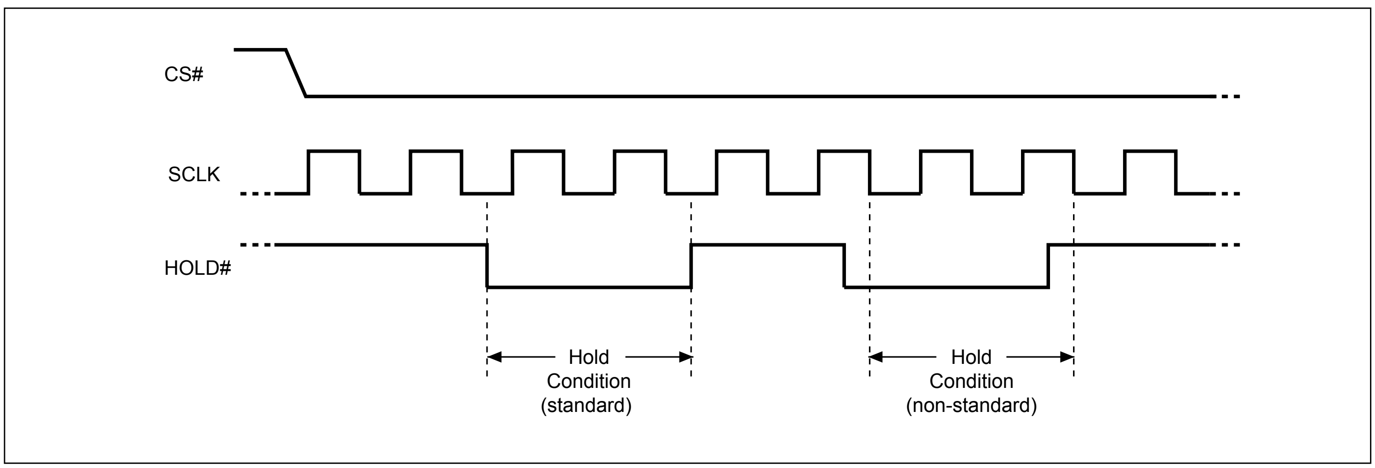
Status bit		Protect level	512b
BP1	BP0		
0	0	0 (none)	None
0	1	1 (All)	All
1	0	2 (All)	All
1	1	3 (All)	All

HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low(if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), and please refer to *Figure 1*.

Figure 1. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Table 2. Command Definition

COMMAND (byte)	WREN (Write Enable)	WRDI (Write Disable)	RDID (Read Identification)	RDSR (Read Status Register)	WRSR (Write Status Register)	READ (Read Data)
1st	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	03 (hex)
2nd						AD1
3rd						AD2
4th						AD3
5th						
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs manufacturer ID and 2-byte device ID	to read out the status register	to write new values to the status register	n bytes read out until CS# goes high

COMMAND (byte)	Fast Read (Fast Read Data)	RDSFDP (Read SFDP)	DREAD (Dual Output mode)	SE (Sector Erase)	BE (Block Erase) (2)	CE (Chip Erase)
1st	0B (hex)	5A (hex)	3B (hex)	20 (hex)	52 or D8 (hex)	60 or C7 (hex)
2nd	AD1	AD1	AD1	AD1	AD1	
3rd	AD2	AD2	AD2	AD2	AD2	
4th	AD3	AD3	AD3	AD3	AD3	
5th	Dummy	Dummy				
Action	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out until CS# goes high	to erase the selected sector	to erase the selected block	to erase the whole chip

COMMAND (byte)	PP (Page Program)	DP (Deep Power-down)	RDP (Release from Deep Power-down)	RES (Read Electronic ID)	REMS (Read Electronic Manufacturer & Device ID)
1st	02 (hex)	B9 (hex)	AB (hex)	AB (hex)	90 (hex)
2nd	AD1			x	x
3rd	AD2			x	x
4th	AD3			x	ADD(1)
5th					
Action	to program the selected page	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	Output the manufacturer ID and device ID

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

(2) BE command may erase whole 512Kb chip.

(3) It is not recommended to adopt any other code which is not in the command definition table above.

Table 3. Memory Organization

Sector	Address Range	
15	00F000h	00FFFFh
:	:	:
3	003000h	003FFFh
2	002000h	002FFFh
1	001000h	001FFFh
0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure the device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z. The CS# falling time needs to follow tCHCL spec. (Please refer to *Table 6. AC CHARACTERISTICS*)

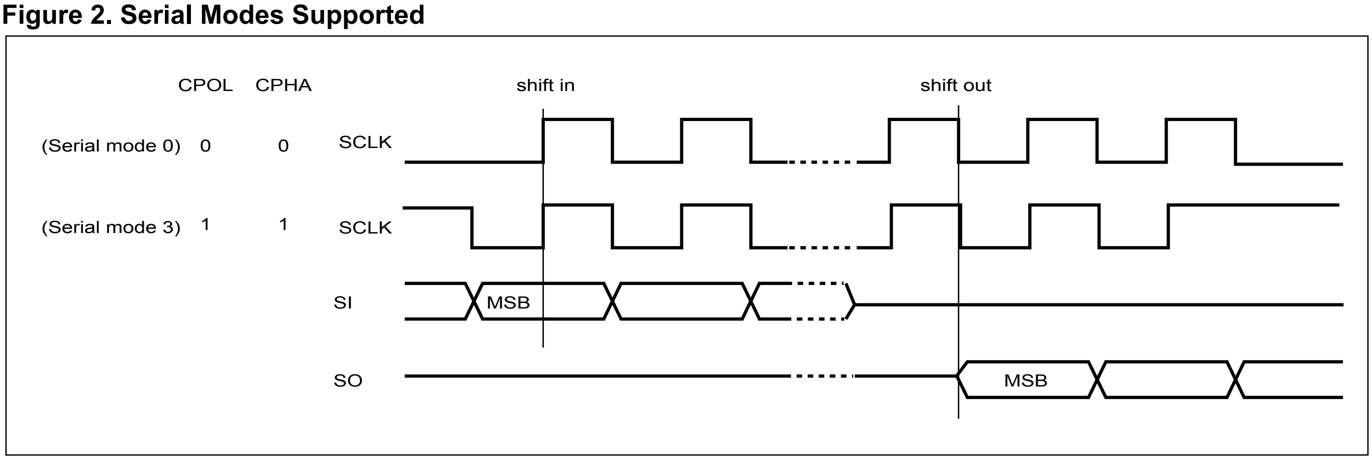
3. When correct command is inputted to this device, it enters active mode and keeps the active mode until next CS# rising edge. The CS# rising time needs to follow tCLCH spec. (Please refer to *Table 6. AC CHARACTERISTICS*)

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *Figure 2*.

5. For the following instructions: RDID, RDSR, READ, FAST_READ, RDSFDP, DREAD, RES and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP and DP the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 2. Serial Modes Supported



Note: *CPOL indicates clock polarity of Serial master:*
-CPOL=1 for SCLK high while idle,
-CPOL=0 for SCLK low while not transmitting.
CPHA indicates clock phase.
The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (Please refer to *Figure 11*)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (Please refer to *Figure 12*)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

(3) Read Identification (RDID)

RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID is as followings: 10(hex) for MX25L512E.

The sequence of issuing RDID instruction is: CS# goes low→sending RDID instruction code→24-bits ID data out on SO→to end RDID operation can use CS# to high at any time during data out. (Please refer to *Figure. 13*)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→sending RDSR instruction code→Status Register data out on SO (Please refer to *Figure. 14*)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction.

BP1, BP0 bits. The Block Protect (BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in *table 1*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed)

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP1, BP0) are read only.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	0	0	0	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable				*(Note 1)*	*(Note 1)*	1=write enable 0=not write enable	1=write operation 0=not in write operation

Notes: *1. Please refer to the table "Protected Area Sizes".*

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP1, BP0) bits to define the protected area of memory (as shown in *table 1*). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (Please refer to *Figure 15*)

The WRSR instruction has no effect on b6, b5, b4, b1, b0 of the status registers.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 4. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP1 bits can be changed.	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be programmed or erased.
Hardware protection mode (HPM)	The SRWD, BP0-BP1 of status register bits cannot be changed.	WP#=0, SRWD bit=1	The protected area cannot be programmed or erased.

Note: *1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in Table 1.*

As the table above showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP1, BP0. The protected area, which is defined by BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP1, BP0. The protected area, which is defined by BP1, BP0, is at software protected mode (SPM)

Note: *If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.*

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note: *to exit the hardware protected mode, it requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP1, BP0.*

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→ data out on SO→ to end READ operation can use CS# to high at any time during data out. (Please refer to *Figure. 16*)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→ 1-dummy byte address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *Figure. 17*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Dual Output Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits(interleave on 1I/2O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence is shown as *Figure 18*.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

The DREAD only performs read operation. Program/Erase /Read ID/Read status....operations do not support DREAD throughputs.

(9) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *table 3*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI → CS# goes high. (Please refer to *Figure 20*)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

(10) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *table 3*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code→ 3-byte address on SI → CS# goes high. (Please refer to *Figure 21*)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

(11) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (Please refer to *table 3*) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→ sending CE instruction code→ CS# goes high. (Please refer to *Figure 22*)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP1, BP0 all set to "0".

(12) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. The CS# must keep during the whole Page Program cycle. The CS#

must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to *Figure 19*)

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(13) Deep Power-down (DP)

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. (Please refer to *Figure 22*)

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Power-down mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Power-down (RDP) instruction, power-cycle, or reset.

(14) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in *Table 6*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of *ID Definitions*. This is not the same as RDID instruction. It is not recommended to use for new design. For new deisng, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as *Figure 24* and *Figure 25*.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in

Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be received, be decoded, and be executed instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

(15) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in Table of *ID Definitions*.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 26*. The Device ID values are listed in Table of *ID Definitions*. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table of ID Definitions

RDID Command	Manufacturer ID	Memory Type	Memory Density
	C2	20	10
RES Command	Electronic ID		
	05		
REMS Command	Manufacturer ID	Device ID	
	C2	05	

(16) Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

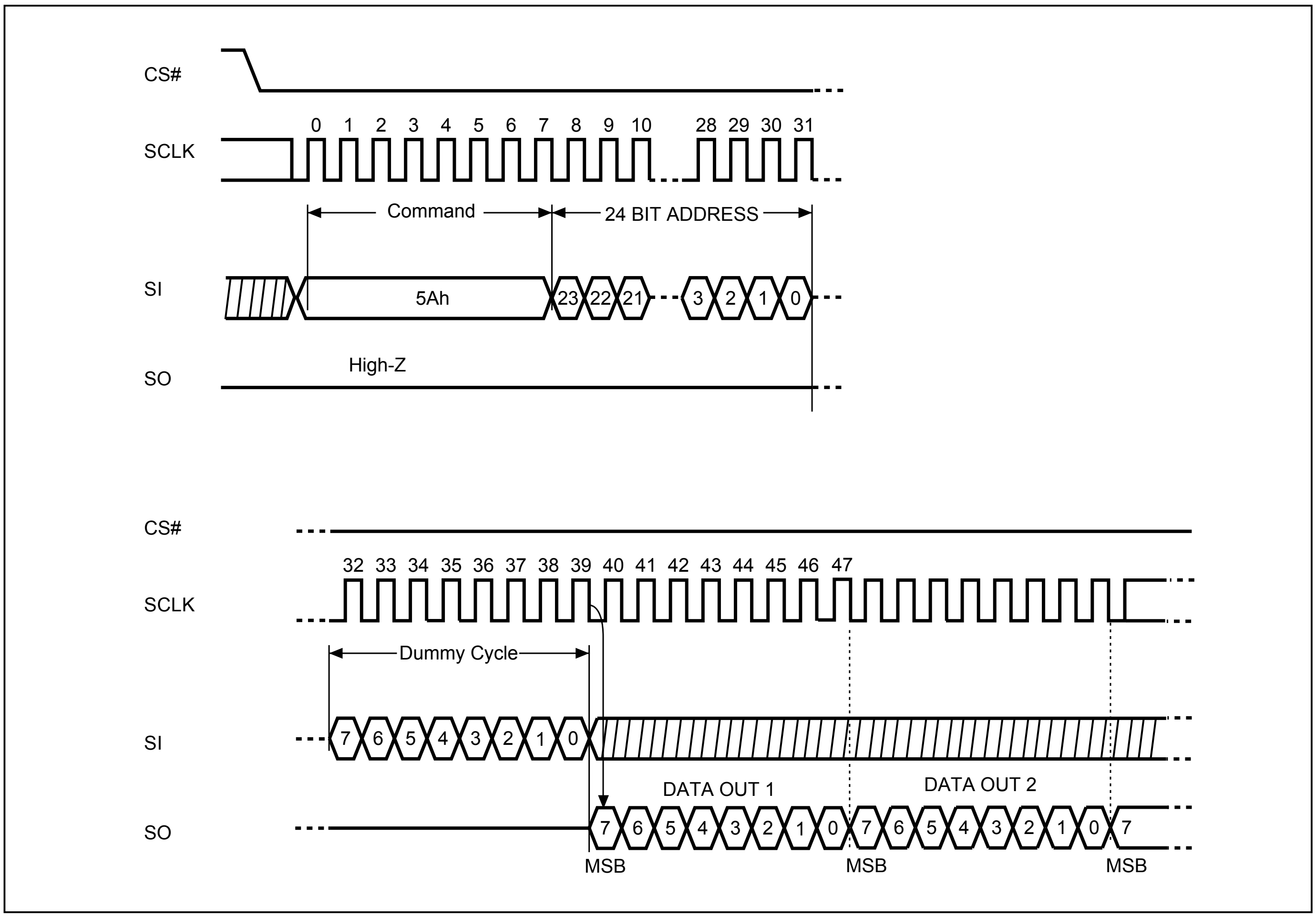


Table a. Signature and Parameter Identification Data Values

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	00h	00h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	01h	01h
Unused		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	09h	09h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Unused		0Fh	31:24	FFh	FFh
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	60h	60h
		15h	15:08	00h	00h
		16h	23:16	00h	00h
Unused		17h	31:24	FFh	FFh

Table b. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not support 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: use 50h opcode, 1: use 06h opcode Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not support 1=support	32h	16	1b	81h
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0=not support 1=support		19	0b	
(1-2-2) Fast Read	0=not support 1=support		20	0b	
(1-4-4) Fast Read	0=not support 1=support		21	0b	
(1-1-4) Fast Read	0=not support 1=support		22	0b	
Unused			23	1b	
Unused		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	0007 FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0000b: Wait states (Dummy Clocks) not support	38h	04:00	0 0000b	00h
(1-4-4) Fast Read Number of Mode Bits (Note4)	000b: Mode Bits not support		07:05	000b	
(1-4-4) Fast Read Opcode		39h	15:08	FFh	FFh
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ah	20:16	0 0000b	00h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3Bh	31:24	FFh	FFh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ch	04:00	0 1000b	08h
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3Dh	15:08	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Eh	20:16	0 0000b	00h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-2-2) Fast Read Opcode		3Fh	31:24	FFh	FFh
(2-2-2) Fast Read	0=not support 1=support	40h	00	0b	EEh
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43h:41h	31:08	FFh	FFh
Unused		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46h	20:16	0 000b	00h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47h	31:24	FFh	FFh
Unused		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4Ah	20:16	0 0000b	00h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4Bh	31:24	FFh	FFh
Sector Type 1 Size	Sector/block size = 2^N bytes (Note5) 0x00b: this sector type doesn't exist	4Ch	07:00	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	15:08	20h	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	4Eh	23:16	10h	10h
Sector Type 2 erase Opcode		4Fh	31:24	D8h	D8h
Sector Type 3 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	50h	07:00	00h	00h
Sector Type 3 erase Opcode		51h	15:08	FFh	FFh
Sector Type 4 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	52h	23:16	00h	00h
Sector Type 4 erase Opcode		53h	31:24	FFh	FFh

Table c. Parameter Table (1): Macronix Flash Parameter Tables

<table>
<tr><th>Description</th><th>Comment</th><th>Add (h)
(Byte)</th><th>DW Add
(Bit)</th><th>Data (h/b)
(Note1)</th><th>Data
(h)</th></tr>
<tr><td>Vcc Supply Maximum Voltage</td><td>2000h=2.000V
2700h=2.700V
3600h=3.600V</td><td>61h:60h</td><td>07:00
15:08</td><td>00h
36h</td><td>00h
36h</td></tr>
<tr><td>Vcc Supply Minimum Voltage</td><td>1650h=1.650V
2250h=2.250V
2350h=2.350V
2700h=2.700V</td><td>63h:62h</td><td>23:16
31:24</td><td>00h
27h</td><td>00h
27h</td></tr>
<tr><td>H/W Reset# pin</td><td>0=not support 1=support</td><td rowspan="9">65h:64h</td><td>00</td><td>0b</td><td rowspan="9">4FF6h</td></tr>
<tr><td>H/W Hold# pin</td><td>0=not support 1=support</td><td>01</td><td>1b</td></tr>
<tr><td>Deep Power Down Mode</td><td>0=not support 1=support</td><td>02</td><td>1b</td></tr>
<tr><td>S/W Reset</td><td>0=not support 1=support</td><td>03</td><td>0b</td></tr>
<tr><td>S/W Reset Opcode</td><td>Reset Enable (66h) should be issued before Reset Opcode</td><td>11:04</td><td>1111 1111b
(FFh)</td></tr>
<tr><td>Program Suspend/Resume</td><td>0=not support 1=support</td><td>12</td><td>0b</td></tr>
<tr><td>Erase Suspend/Resume</td><td>0=not support 1=support</td><td>13</td><td>0b</td></tr>
<tr><td>Unused</td><td></td><td>14</td><td>1b</td></tr>
<tr><td>Wrap-Around Read mode</td><td>0=not support 1=support</td><td>15</td><td>0b</td></tr>
<tr><td>Wrap-Around Read mode Opcode</td><td></td><td>66h</td><td>23:16</td><td>FFh</td><td>FFh</td></tr>
<tr><td>Wrap-Around Read data length</td><td>08h:support 8B wrap-around read
16h:8B&16B
32h:8B&16B&32B
64h:8B&16B&32B&64B</td><td>67h</td><td>31:24</td><td>FFh</td><td>FFh</td></tr>
<tr><td>Individual block lock</td><td>0=not support 1=support</td><td rowspan="10">6Bh:68h</td><td>00</td><td>0b</td><td rowspan="9">C7FEh</td></tr>
<tr><td>Individual block lock bit (Volatile/Nonvolatile)</td><td>0=Volatile 1=Nonvolatile</td><td>01</td><td>1b</td></tr>
<tr><td>Individual block lock Opcode</td><td></td><td>09:02</td><td>1111 1111b</td></tr>
<tr><td>Individual block lock Volatile protect bit default protect status</td><td>0=protect 1=unprotect</td><td>10</td><td>1b</td></tr>
<tr><td>Secured OTP</td><td>0=not support 1=support</td><td>11</td><td>0b</td></tr>
<tr><td>Read Lock</td><td>0=not support 1=support</td><td>12</td><td>0b</td></tr>
<tr><td>Permanent Lock</td><td>0=not support 1=support</td><td>13</td><td>0b</td></tr>
<tr><td>Unused</td><td></td><td>15:14</td><td>11b</td></tr>
<tr><td>Unused</td><td></td><td>31:16</td><td>FFh</td><td>FFh</td></tr>
<tr><td>Unused</td><td></td><td>6Fh:6Ch</td><td>31:00</td><td>FFh</td><td>FFh</td></tr>
</table>

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh.

POWER-ON STATE

The device is at the states as below when power-up:
- Standby mode *(please note it is not deep power-down mode)*
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level (Please refer to the figure of "*power-up timing*"):
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal Power-On Reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the time delay: tVSL after VCC reached VCC minimum level. Please refer to the figure of "*power-up timing*".

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Note:
- *To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)*