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MACRONIX  
INTERNATIONAL CO., LTD.

**MX25L6445E**

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**MX25L6445E**  
**HIGH PERFORMANCE**  
**SERIAL FLASH SPECIFICATION**

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**64M-BIT [x 1/x 2/x 4] CMOS MXSMIO™ (SERIAL MULTI I/O) FLASH MEMORY**

**FEATURES**

**GENERAL**

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 64Mb: 67,108,864 x 1 bit structure or 33,554,432 x 2 bits (two I/O mode) structure or 16,777,216 x 4 bits (four I/O mode) structure
- 2048 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 256 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 128 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

**PERFORMANCE**

- High Performance
  - VCC = 2.7~3.6V
  - Normal read
    - 50MHz
  - Fast read (Normal Serial Mode)
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 70MHz with 4 dummy cycles
    - 4 I/O: 70MHz with 6 dummy cycles
  - Fast read (Double Transfer Rate Mode)
    - 1 I/O: 50MHz with 6 dummy cycles
    - 2 I/O: 50MHz with 6 dummy cycles
    - 4 I/O: 50MHz with 8 dummy cycles
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Continuously Program mode (automatically increase address under word program mode)
  - Fast erase time: 60ms (typ.)/sector (4K-byte per sector) ; 0.7s(typ.) /block (64K-byte per block); 50s(typ.) /chip
- Low Power Consumption
  - Low active read current: 19mA(max.) at 104MHz, 15mA(max.) at 66MHz and 10mA(max.) at 33MHz
  - Low active programming current: 25mA (max.)
  - Low active erase current: 25mA (max.)
  - Low standby current: 50uA (max.)
  - Deep power down current: 20uA (max.)
- Typical 100,000 erase/program cycles
- 20 years data retention

**SOFTWARE FEATURES**

- Input Data Format
  - 1-byte Command code

- Advanced Security Features
  - BP0-BP3 block group protect
  - Flexible individual block protect when OTP WPSEL=1
  - Additional 4K bits secured OTP for unique identifier
- Auto Erase and Auto Program Algorithms
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
  - RES command for 1-byte Device ID
  - REMS, REMS2, REMS4 and REMS4D commands for 1-byte Manufacturer ID and 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

#### **HARDWARE FEATURES**

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O mode
- NC/SIO3
  - NC pin or serial data Input/Output for 4 x I/O mode
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-WSON (8 x 6mm)
  - 8-pin SOP (200mil)
  - **All devices are RoHS Compliant**

## GENERAL DESCRIPTION

MX25L6445E is 67,108,864 bits serial Flash memory, which is configured as 8,388,608 x 8 internally. When it is in two or four I/O mode, the structure becomes 33,554,432 bits x 2 or 16,777,216 bits x 4. The MX25L6445E features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L6445E provides high performance read mode, which may latch address and data on both rising and falling edge of clock. By using this high performance read mode, the data throughput may be doubling. Moreover, the performance may reach direct code execution, the RAM size of the system may be reduced and further saving system cost.

MX25L6445E, MXSMIO™ (Serial Multi I/O) flash memory, provides sequential read operation on the whole chip and multi-I/O features.

When it is in dual I/O mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in quad I/O mode, the SI pin, SO pin, WP# pin and NC pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Continuously Program mode and erase command are executed on 4K-byte sector, 32K-byte/64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via the WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 100uA DC current.

The MX25L6445E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

**Table 1. Additional Features**

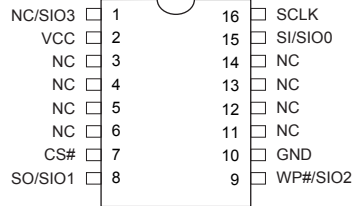
Additional Features Part Name	Protection and Security		Read Performance					
	Flexible or Individual block (or sector) protection	4K-bit secured OTP	1 I/O Read (104 MHz)	2 I/O Read (70 MHz)	4 I/O Read (70 MHz)	1 I/O DT Read (50 MHz)	2 I/O DT Read (50 MHz)	4 I/O DT Read (50 MHz)
MX25L6445E	V	V	V	V	V	V	V	V

Additional Features Part Name	Identifier					
	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	REMS4D (command: CF hex)	RDID (command: 9F hex)
MX25L6445E	16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 20 17 (hex)

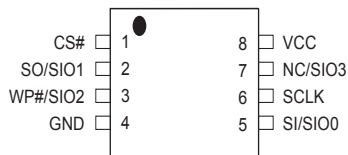


## PIN CONFIGURATION

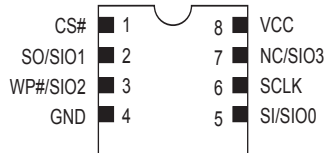
### 16-PIN SOP (300mil)



### 8-PIN SOP (200mil)

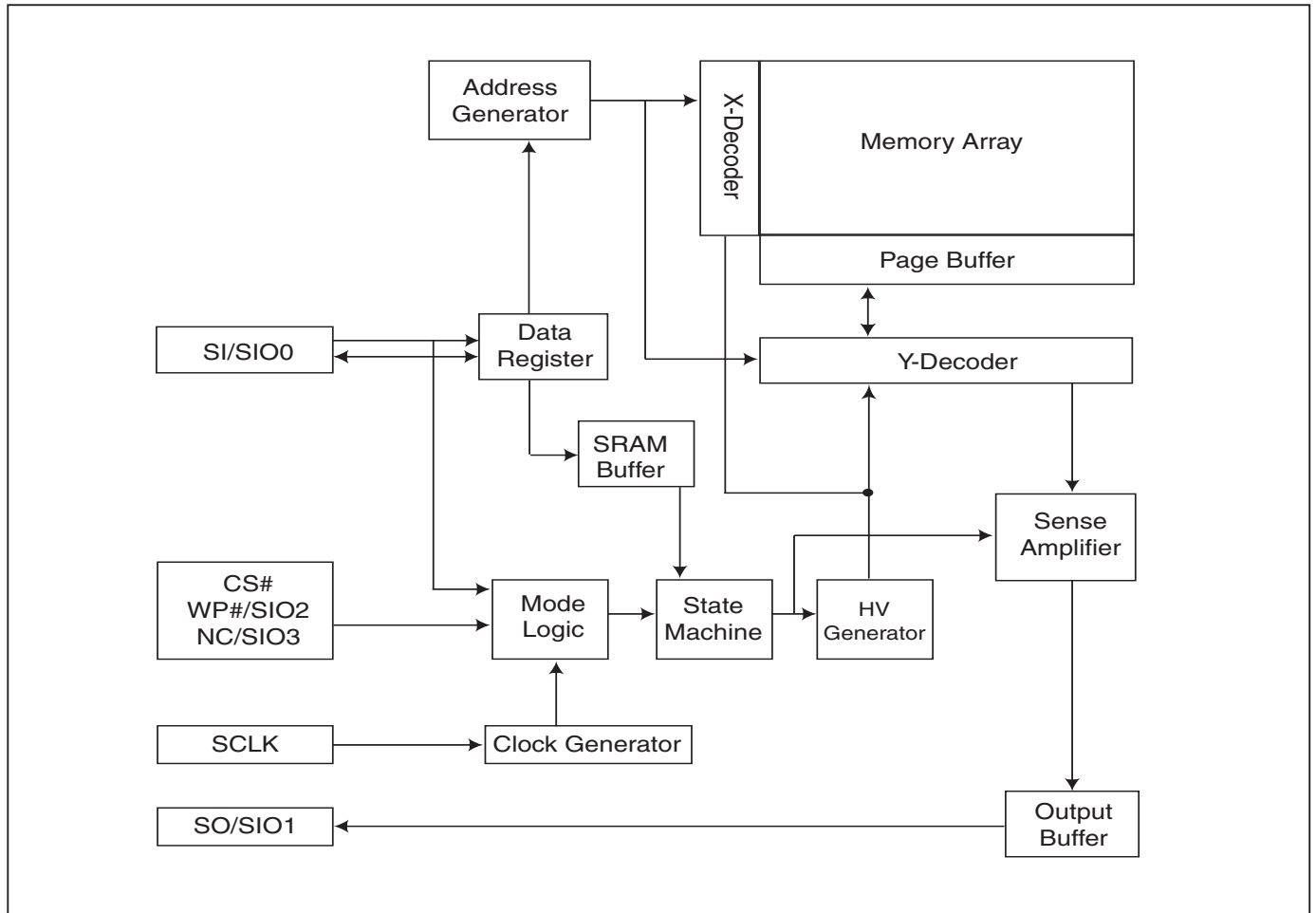


### 8-WSON (8x6mm)



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O mode)
NC/SIO3	NC pin (Not connect) or Serial Data Input & Output (for 4xI/O mode)
VCC	+ 3.3V Power Supply
GND	Ground
NC	No Connection

**BLOCK DIAGRAM**

## DATA PROTECTION

MX25L6445E is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the standby mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data. The WEL bit will return to reset stage under following situations:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP, 4PP) command completion
  - Continuously Program mode (CP) instruction completion
  - Sector Erase (SE) command completion
  - Block Erase (BE, BE32K) command completion
  - Chip Erase (CE) command completion
  - Single Block Lock/Unlock (SBLK/SBULK) instruction completion
  - Gang Block Lock/Unlock (GBLK/GBULK) instruction completion
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

### I. Block lock protection

- The Software Protected Mode (SPM) uses (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "[Protected Area Sizes](#)", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits. Please refer to table of "[Protected Area Sizes](#)".
- The Hardware Protected Mode (HPM) uses WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O mode, the feature of HPM will be disabled.
- MX25L6445E provides individual block (or sector) write protect & unprotect. User may enter the mode with WPSEL command and conduct individual block (or sector) write protect with SBLK instruction, or SBULK for individual block (or sector) unprotect. Under the mode, user may conduct whole chip (all blocks) protect with GBLK instruction and unlock the whole chip with GBULK instruction.

**Table 2. Protected Area Sizes**

Status bit				Protection Area
BP3	BP2	BP1	BP0	64Mb
0	0	0	0	0 (none)
0	0	0	1	1 (2 blocks, block 126th-127th)
0	0	1	0	2 (4 blocks, block 124th-127th)
0	0	1	1	3 (8 blocks, block 120th-127th)
0	1	0	0	4 (16 blocks, block 112nd-127th)
0	1	0	1	5 (32 blocks, block 96th-127th)
0	1	1	0	6 (64 blocks, block 64th-127th)
0	1	1	1	7 (128 blocks, all)
1	0	0	0	8 (128 blocks, all)
1	0	0	1	9 (128 blocks, all)
1	0	1	0	10 (128 blocks, all)
1	0	1	1	11 (128 blocks, all)
1	1	0	0	12 (128 blocks, all)
1	1	0	1	13 (128 blocks, all)
1	1	1	0	14 (128 blocks, all)
1	1	1	1	15 (128 blocks, all)

**Note:** The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

**II. Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker. Please refer to [Table 3. 4K-bit Secured OTP Definition](#).

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "[Security Register Definition](#)" for security register bit definition and table of "[4K-bit Secured OTP Definition](#)" for address range definition.
- **Note:** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

**Table 3. 4K-bit Secured OTP Definition**

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

## Memory Organization

**Table 4. Memory Organization**

	Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range		
<div><div></div><div>individual block lock/unlock unit:64K-byte</div></div>	127	255	2047	7FF000h	7FFFFFFh	<div><div></div><div>individual 16 sectors lock/unlock unit:4K-byte</div></div>
			⋮			
			2040	7F8000h	7F8FFFh	
		254	2039	7F7000h	7F7FFFh	
			⋮			
			2032	7F0000h	7F0FFFh	
	126	253	2031	7EF000h	7EFFFFh	
			⋮			
			2024	7E8000h	7E8FFFh	
		252	2023	7E7000h	7E7FFFh	
			⋮			
			2016	7E0000h	7E0FFFh	
125	251	2015	7DF000h	7DFFFFh		
		⋮				
		2008	7D8000h	7D8FFFh		
	250	2007	7D7000h	7D7FFFh		
		⋮				
		2000	7D0000h	7D0FFFh		

individual block  
lock/unlock unit:64K-byte

individual block  
lock/unlock unit:64K-byte

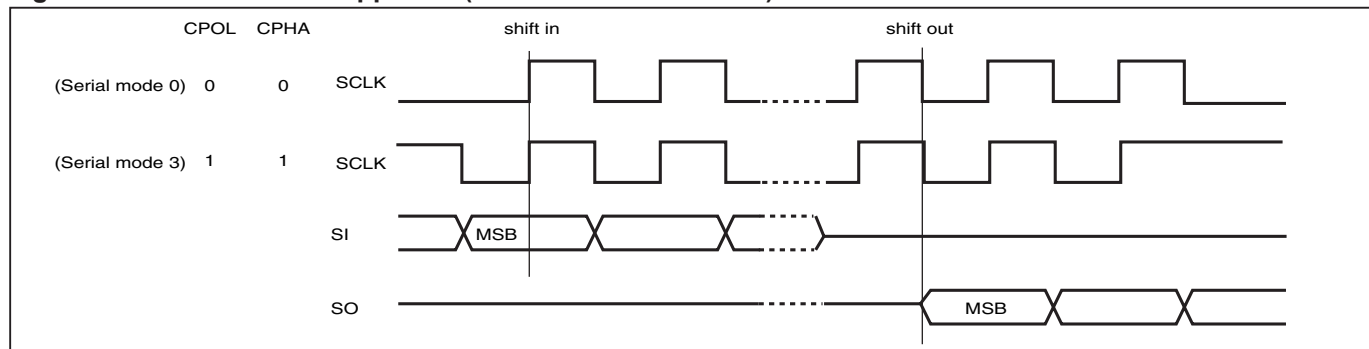
<div><div></div><div>individual block lock/unlock unit:64K-byte</div></div>	2	5	47	02F000h	02FFFFFFh	<div><div></div><div>individual 16 sectors lock/unlock unit:4K-byte</div></div>
			⋮			
			40	028000h	028FFFh	
		4	39	027000h	027FFFh	
			⋮			
			32	020000h	020FFFh	
	1	3	31	01F000h	01FFFFFFh	
			⋮			
			24	018000h	018FFFh	
		2	23	017000h	017FFFh	
			⋮			
			16	010000h	010FFFh	
0	1	15	00F000h	00FFFFFFh		
		⋮				
		8	008000h	008FFFh		
	0	7	007000h	007FFFh		
		⋮				
		0	000000h	000FFFh		



## DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.
4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as [Figure 1-1](#). For high performance (Double Transfer Rate Read serial mode), data is latched on both rising and falling edge of clock and data shifts out on both rising and falling edge of clock as [Figure 1-2](#).
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST\_READ, RDSFDP, 2READ, 4READ, FAST-DTRD, 2DTRD, 4DTRD, RDBLOCK, RES, REMS, REMS2, REMS4, and REMS4D the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, HPM, CE, PP, CP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK, ENSO, EXSO, WRSCUR, ENPLM, EXPLM, ESRY, DSRY and CLSR the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

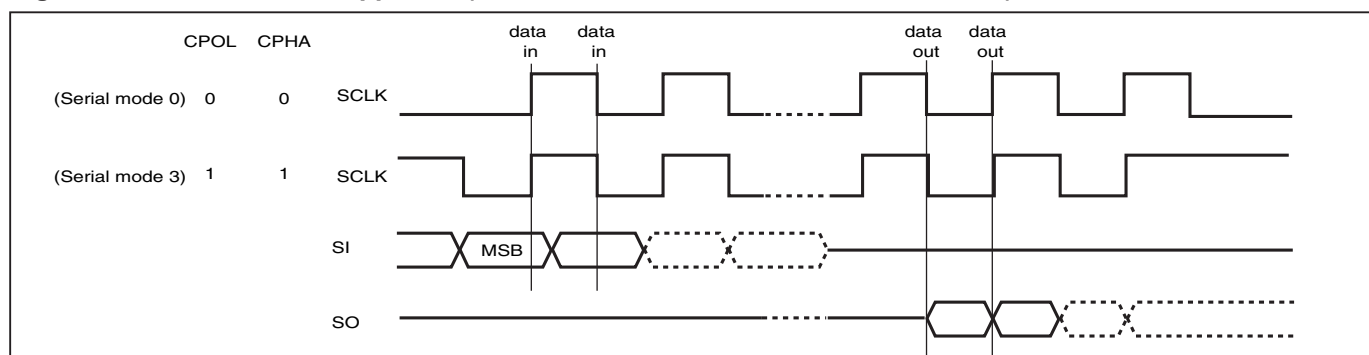
**Figure 1-1. Serial Modes Supported (for Normal Serial mode)**



### Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

**Figure 1-2. Serial Modes Supported (for Double Transfer Rate serial read mode)**



## COMMAND DESCRIPTION

**Table 5. Command Sets**

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	FASTDTRD (fast DT read)	2DTRD (Dual I/O DT Read)	4DTRD (Quad I/O DT Read)
Command (hex)	06	04	9F	05	01	0D	BD	ED
Input Cycles					Data(8)	ADD(12)	ADD(6)	ADD(3)
Dummy Cycles						6	6	1+7
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new values to the status register	n bytes read out (Double Transfer Rate) until CS# goes high	n bytes read out (Double Transfer Rate) by 2xI/O until CS# goes high	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

COMMAND (byte)	READ (read data)	FAST READ (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command) Note1	4READ (4 x I/O read command)	4PP (quad page program)	SE (sector erase)	BE (block erase 64KB)
Command (hex)	03	0B	5A	BB	EB	38	20	D8
Input Cycles	ADD(24)	ADD(24)	ADD(24)	ADD(12)	ADD(6)	ADD(6)+Data(512)	ADD(24)	ADD(24)
Dummy Cycles		8	8	4	2+4			
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	quad input to program the selected page	to erase the selected sector	to erase the selected 64KB block

COMMAND (byte)	BE 32K (block erase 32KB)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)
Command (hex)	52	60 or C7	02	AD	B9	AB	AB	90
Input Cycles	ADD(24)		ADD(24)+Data(2048)	ADD(24)+Data(16)				ADD(24)
Dummy Cycles							24	
Action	to erase the selected 32KB block	to erase whole chip	to program the selected page	continuously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID

COMMAND (byte)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	REMS4D (read ID for 4x I/O DT mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/ BY#)
Command (hex)	EF	DF	CF	B1	C1	2B	2F	70
Input Cycles	ADD(24)	ADD(24)	ADD(24)					
Dummy Cycles								
Action	output the Manufacturer ID & Device ID	output the Manufacturer ID & device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/ BY# during CP mode

COMMAND (byte)	DSRY (disable SO to output RY/ BY#)	CLSR (Clear SR Fail Flags)	HPM (High Performance Enable Mode)	WPSEL (write protection selection)	SBLK (single block lock) *Note 2	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)
Command (hex)	80	30	A3	68	36	39	3C	7E
Input Cycles					ADD(24)	ADD(24)	ADD(24)	
Dummy Cycles								
Action	to disable SO to output RY/ BY# during CP mode	clear security register bit 6 and bit 5	Quad I/O high Performance mode	to enter and enable individual block protect mode	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect

COMMAND (byte)	GBULK (gang block unlock)
Command (hex)	98
Input Cycles	
Dummy Cycles	
Action	whole chip unprotect

**Notes:**

1. It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
2. In individual block write protection mode, all blocks/sectors are locked as default.

**(1) Write Enable (WREN)**

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE, BE32K, CE, WRSR, SBLK, SBULK, GBLK and GBULK, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (Please refer to [Figure 11](#))

**(2) Write Disable (WRDI)**

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (Please refer to [Figure 12](#))

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP, 4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE, BE32K) instruction completion
- Chip Erase (CE) instruction completion
- Continuously Program mode (CP) instruction completion
- Single Block Lock/Unlock (SBLK/SBULK) instruction completion
- Gang Block Lock/Unlock (GBLK/GBULK) instruction completion

**(3) Read Identification (RDID)**

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of "[ID Definitions](#)". (Please refer to [Table 6](#))

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (Please refer to [Figure 13](#))

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

**(4) Read Status Register (RDSR)**

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO (Please refer to [Figure 14](#)).

The definition of the status register bits is as below:

**WIP bit.** The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

**WEL bit.** The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area.

**BP3, BP2, BP1, BP0 bits.** The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in Table 2) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

**QE bit.** The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM will be disabled.

**SRWD bit.** The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

**Status Register**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1= Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

**Note:** see the [Table 2 "Protected Area Size"](#) in page 11.



**(5) Write Status Register (WRSR)**

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in [Table 2](#)). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (Please refer to [Figure 15](#))

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

**Protection Modes**

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

**Note:** As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in [Table 2](#).

As the table above showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM):

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

**Note:**

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

If the system goes into four I/O mode, the feature of HPM will be disabled.

**(6) Read Data Bytes (READ)**

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency  $f_R$ . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low → sending READ instruction code → 3-byte address on SI → data out on SO → to end READ operation can use CS# to high at any time during data out. (Please refer to [Figure 16](#))

**(7) Read Data Bytes at Higher Speed (FAST\_READ)**

The FAST\_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency  $f_C$ . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST\_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST\_READ instruction is: CS# goes low → sending FAST\_READ instruction code → 3-byte address on SI → 1-dummy byte (default) address on SI → data out on SO → to end FAST\_READ operation can use CS# to high at any time during data out. (Please refer to [Figure 17](#))

While Program/Erase/Write Status Register cycle is in progress, FAST\_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**(8) Fast Double Transfer Rate Read (FASTDTRD)**

The FASTDTRD instruction is for doubling reading data out, signals are triggered on both rising and falling edge of clock. The address is latched on both rising and falling edge of SCLK, and data of each bit shifts out on both rising and falling edge of SCLK at a maximum frequency  $f_{C2}$ . The 2-bit address can be latched-in at one clock, and 2-bit data can be read out at one clock, which means one bit at rising edge of clock, the other bit at falling edge of clock. The first address byte can be at any location.

The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FASTDTRD instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FASTDTRD instruction is: CS# goes low → sending FASTDTRD instruction code (1bit per clock) → 3-byte address on SI (2-bit per clock) → 6-dummy clocks (default) on SI → data out on SO (2-bit per clock) → to end FASTDTRD operation can use CS# to high at any time during data out. (Please refer to [Figure 18](#))

While Program/Erase/Write Status Register cycle is in progress, FASTDTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**(9) 2 x I/O Read Mode (2READ)**

The 2READ instruction enables Double Transfer Rate of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maxi-

maximum frequency  $fT$ . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low → sending 2READ instruction → 24-bit address interleaved on SIO1 & SIO0 → 4-bit dummy cycle on SIO1 & SIO0 → data out interleaved on SIO1 & SIO0 → to end 2READ operation can use CS# to high at any time during data out (Please refer to [Figure 19 for 2 x I/O Read Mode Timing Waveform](#)).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

#### **(10) 2 x I/O Double Transfer Rate Read Mode (2DTRD)**

The 2DTRD instruction enables Double Transfer Rate throughput on dual I/O of Serial Flash in read mode. The address (interleaved on dual I/O pins) is latched on both rising and falling edge of SCLK, and data (interleaved on dual I/O pins) shift out on both rising and falling edge of SCLK at a maximum frequency  $fT2$ . The 4-bit address can be latched-in at one clock, and 4-bit data can be read out at one clock, which means two bits at rising edge of clock, the other two bits at falling edge of clock. The first address byte can be at any location.

The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2DTRD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2DTRD instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 2DTRD instruction is: CS# goes low → sending 2DTRD instruction (1-bit per clock) → 24-bit address interleaved on SIO1 & SIO0 (4-bit per clock) → 6-bit dummy clocks on SIO1 & SIO0 → data out interleaved on SIO1 & SIO0 (4-bit per clock) → to end 2DTRD operation can use CS# to high at any time during data out (Please refer to [Figure 20 for 2 x I/O Double Transfer Rate Read Mode Timing Waveform](#)).

While Program/Erase/Write Status Register cycle is in progress, 2DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

#### **(11) 4 x I/O Read Mode (4READ)**

The 4READ instruction enables quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleaved on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency  $fQ$ . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low → sending 4READ instruction → 24-bit address interleaved on SIO3, SIO2, SIO1 & SIO0 → 6 dummy cycles → data out interleaved on SIO3, SIO2, SIO1 & SIO0 → to end 4READ operation can use CS# to high at any time during data out (Please refer to [Figure 21 for 4 x I/O Read Mode Timing Waveform](#)).

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low → sending 4READ instruction → 3-bytes address interleaved on SIO3, SIO2, SIO1 & SIO0 → performance enhance toggling bit

P[7:0] → 4 dummy cycles → data out still CS# goes high → CS# goes low (reduce 4Read instruction) → 24-bit random access address (Please refer to [Figure 22 for 4x I/O Read Enhance Performance Mode timing waveform](#)).

In the performance-enhancing mode (Notes of [Figure 22](#)), P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h. These commands will reset the performance enhance mode. And afterwards CS# is raised and then lowered, the system then will return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### (12) 4 x I/O Double Transfer Rate Read Mode (4DTRD)

The 4DTRD instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4DTRD instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK at a maximum frequency fQ2. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4DTRD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4DTRD instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

The sequence of issuing 4DTRD instruction is: CS# goes low → sending 4DTRD instruction (1-bit per clock) → 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0 (8-bit per clock) → 8 dummy clocks → data out interleave on SIO3, SIO2, SIO1 & SIO0 (8-bit per clock) → to end 4DTRD operation can use CS# to high at any time during data out (Please refer to [Figure 23 for 4 x I/O Read Mode Double Transfer Rate Timing Waveform](#)).

Another sequence of issuing enhanced mode of 4DTRD instruction especially useful in random access is: CS# goes low → sending 4DTRD instruction (1-bit per clock) → 3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 (8-bit per clock) → performance enhance toggling bit P[7:0] → 7 dummy clocks → data out (8-bit per clock) still CS# goes high → CS# goes low (eliminate 4 Read instruction) → 24-bit random access address (Please refer to [Figure 24 for 4x I/O Double Transfer Rate read enhance performance mode timing waveform](#)).

While Program/Erase/Write Status Register cycle is in progress, 4DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### (13) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see [Table 4](#)) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code → 3-byte address on SI → CS# goes high. (Please refer to Figure 25)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the

sector is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

#### **(14) Block Erase (BE)**

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see [Table 4](#)) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high. (Please refer to [Figure 26](#))

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

#### **(15) Block Erase (BE32K)**

The Block Erase (BE32) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32). Any address of the block (see [Table 4](#)) is a valid address for Block Erase (BE32) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32 instruction is: CS# goes low → sending BE32 instruction code → 3-byte address on SI → CS# goes high. (Please refer to [Figure 26](#))

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

#### **(16) Chip Erase (CE)**

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high. (Please refer to [Figure 27](#))

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected, the Chip Erase (CE) instruction will not be executed, but WEL will be reset.



**(17) Page Program (PP)**

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (the eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the requested page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to [Figure 28](#))

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary( the latest eighth bit of data being latched in), otherwise, the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

**(18) 4 x I/O Page Program (4PP)**

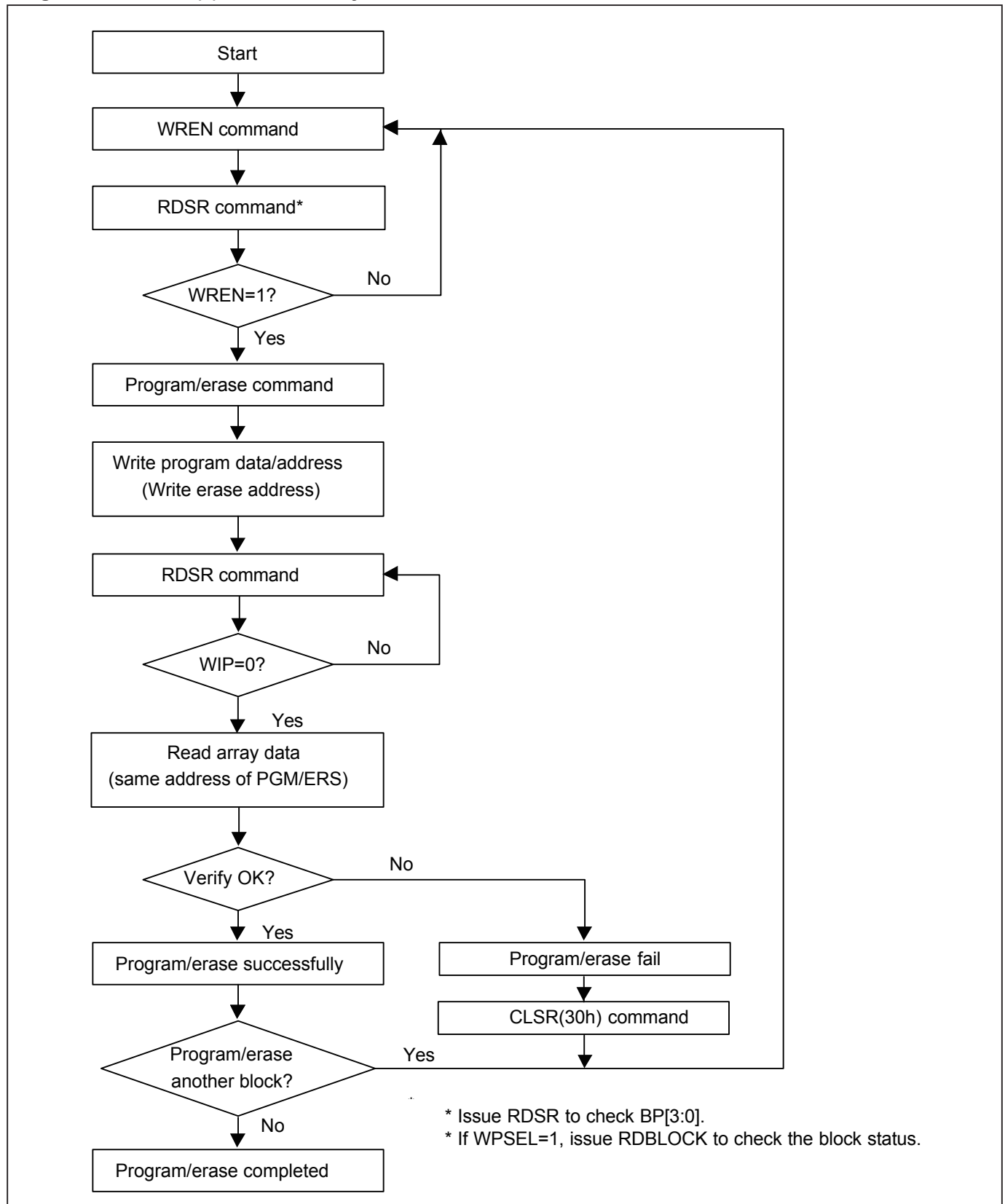
The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3, which can raise programer performance and and the effectiveness of application of lower clock less than 20MHz. For system with faster clock, the Quad page program cannot provide more performance, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 20MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high. (Please refer to [Figure 29](#))

If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

The Program/Erase function instruction function flow is as follows:

**Program/Erase Flow(1) with read array data**



**Program/Erase Flow(2) without read array data**

