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MX25R4035F

ULTRA LOW POWER, 4M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

Key Features

- *Ultra Low Power Mode and High Performance Mode*
- *Wide Range VCC* 1.65V-3.6V *for Read, Erase and Program Operations*
- *Unique ID and Secure OTP Support*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Program Suspend/Resume & Erase Suspend/Resume*

Contents

Ultra Low Power 4M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 4,194,304 x 1 bit structure or 2,097,152 x 2 bits (two I/O mode) structure or 1048,576 x 4 bits (four I/O mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K/64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - Operation Voltage: 1.65V-3.6V for Read, Erase and Program Operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast read
    - 1 I/O: 108MHz with 8 dummy cycles
    - 2 I/O: 104MHz with 4 dummy cycles, equivalent to 208MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast program and erase time
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
- Ultra Low Power Consumption
- Minimum 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
- Additional 8K bits secured OTP
  - Features unique identifier.
  - Factory locked identifiable and customer lockable
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend and Program/Erase Resume
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode
- Support Unique ID (Please contact local Macronix sales for detail information)

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- RESET#/SIO3 * or HOLD#/SIO3 *
  - Hardware Reset pin or Serial input & Output for 4 x I/O read mode
    or
  - HOLD feature, to pause the device without deselecting the device or Serial input & Output for 4 x I/O read mode
  *** Depends on part number options**
- PACKAGE
  - 8-pin SOP (150mil/200mil)
  - 8-land USON (2x3mm)
  - 8-land WSON (6x5mm)
  - 8-ball WLCSP (3-2-3 Ball Array)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25R4035F is 4Mb bits Serial NOR Flash memory, which is configured as 524,288 x 8 internally. When it is in four I/O mode, the structure becomes 1048,576 bits x 4 or 2,097,152 bits x 2.

MX25R4035F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and RESET#/HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25R4035F MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

The MX25R4035F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

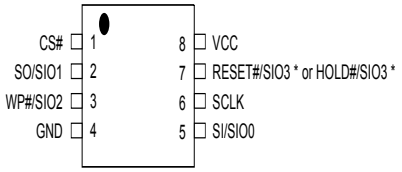
Table 1. Additional Feature

Protection and Security	MX25R4035F
Flexible Block Protection (BP0-BP3)	V
8K-bit security OTP	V

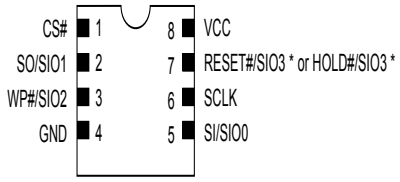
Fast Read Performance	Ultra Low Power Mode (Configuration Register-2 bit1= 0)					High Performance Mode (Configuration Register-2 bit1= 1)				
I/O	1 I/O	1I/2O	2 I/O	1I/4O	4 I/O	1 I/O	1I/2O	2 I/O	1I/4O	4 I/O
Dummy Cycle	8	8	4	8	6	8	8	4	8	6
Frequency	33MHz	16MHz	16MHz	16MHz	16MHz	108MHz	104MHz	104MHz	104MHz	104MHz

3. PIN CONFIGURATIONS

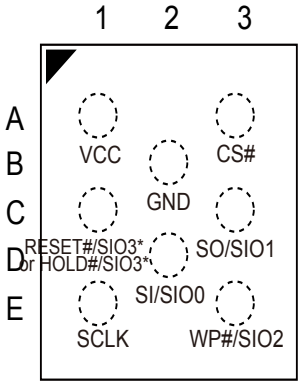
8-PIN SOP (150mil/200mil)



8-LAND USON (2x3mm), WSON (6x5mm)



3-2-3 Ball Array 8-BALL BGA (WLCSP) TOP View



* Depends on part number options.

4. PIN DESCRIPTION

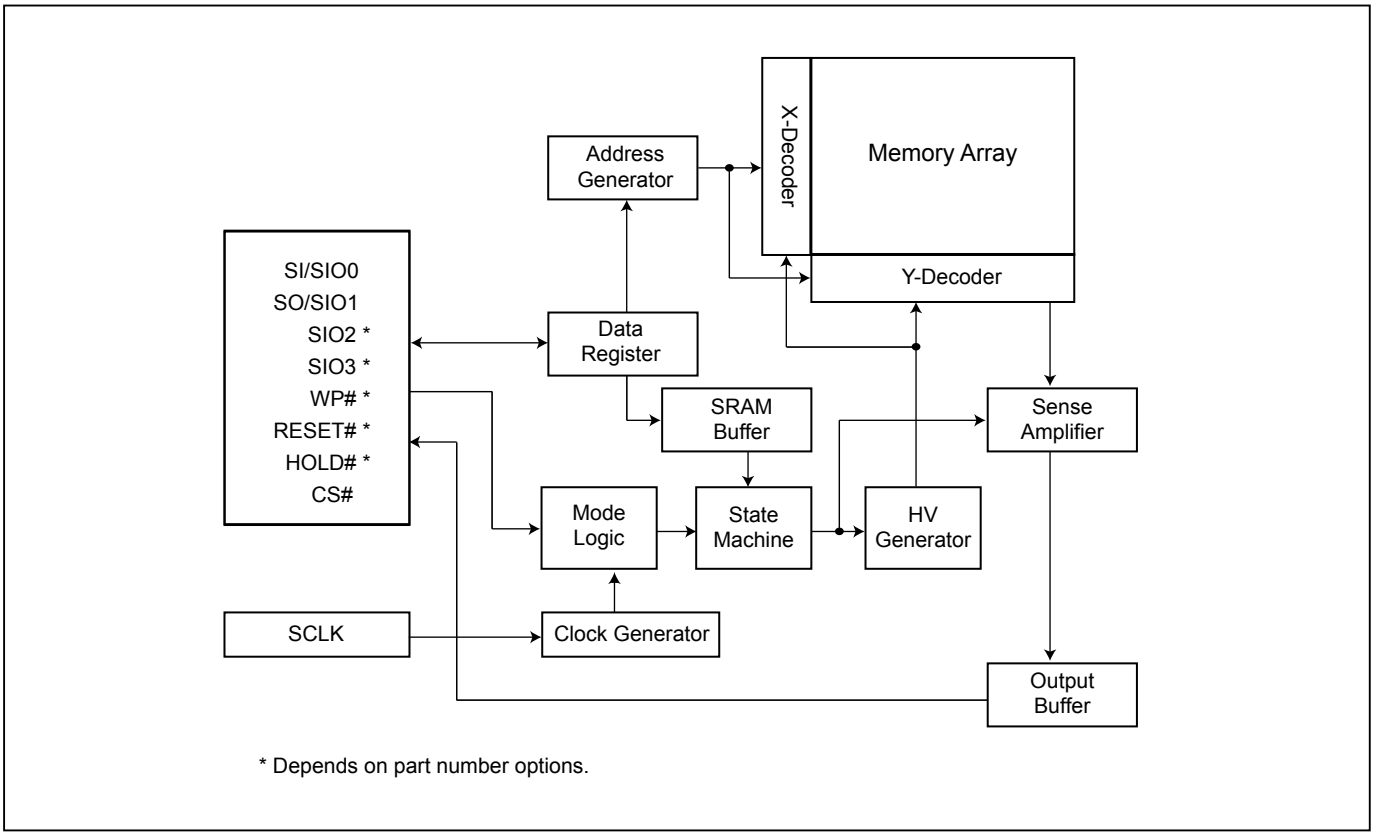
SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
RESET#/SIO3 *	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)
HOLD#/SIO3 *	To pause the device without deselecting the device or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground

* Depends on part number options.

Note:

1. The pin of RESET#/SIO3, HOLD#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to RESET#/ SIO3, HOLD#/SIO3 or WP#/SIO2 pin.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except toggling the CS#. For more detail please see *"10-24. Deep Power-down (DP)"*.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect (SRWD) bit. If the system goes into four I/O mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes (TB bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 7th)
0	0	1	0	2 (2blocks, block 6th-7th)
0	0	1	1	3 (4blocks, block 4th-7th)
0	1	0	0	4 (8blocks, protect all)
0	1	0	1	5 (8blocks, protect all)
0	1	1	0	6 (8blocks, protect all)
0	1	1	1	7 (8blocks, protect all)
1	0	0	0	8 (8blocks, protect all)
1	0	0	1	9 (8blocks, protect all)
1	0	1	0	10 (8blocks, protect all)
1	0	1	1	11 (8blocks, protect all)
1	1	0	0	12 (8blocks, protect all)
1	1	0	1	13 (8blocks, protect all)
1	1	1	0	14 (8blocks, protect all)
1	1	1	1	15 (8blocks, protect all)

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, block 0th-3th)
0	1	0	0	4 (8blocks, protect all)
0	1	0	1	5 (8blocks, protect all)
0	1	1	0	6 (8blocks, protect all)
0	1	1	1	7 (8blocks, protect all)
1	0	0	0	8 (8blocks, protect all)
1	0	0	1	9 (8blocks, protect all)
1	0	1	0	10 (8blocks, protect all)
1	0	1	1	11 (8blocks, protect all)
1	1	0	0	12 (8blocks, protect all)
1	1	0	1	13 (8blocks, protect all)
1	1	1	0	14 (8blocks, protect all)
1	1	1	1	15 (8blocks, protect all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. Additional 8K-bit secured OTP for unique identifier: to provide 8K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

The 8K-bit secured OTP area is composed of two rows of 4K-bit. Customer could lock the first 4K-bit OTP area and factory could lock the other.

- Security register bit 0 indicates whether the 2nd 4K-bit is locked by factory or not.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of *"Table 8. Security Register Definition"* for security register bit definition and table of *"Table 3. 8K-bit Secured OTP Definition"* for address range definition.

- To program 8K-bit secured OTP by entering secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting secured OTP mode by writing EXSO command.

Note: Once lock-down whatever by factory or customer, the corresponding secured area cannot be changed any more. While in 8K-bit Secured OTP mode, array access is not allowed.

Table 3. 8K-bit Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Customer
xxx200~xxx3FF	4096-bit	Determined by Factory

7. MEMORY ORGANIZATION

Table 4. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
7	15	127	07F000h	07FFFFh
	|	:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
	|	:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
	|	:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
	|	:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
	|	:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
	|	:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
	|	:	:	:
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
	|	:	:	:
	0	2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

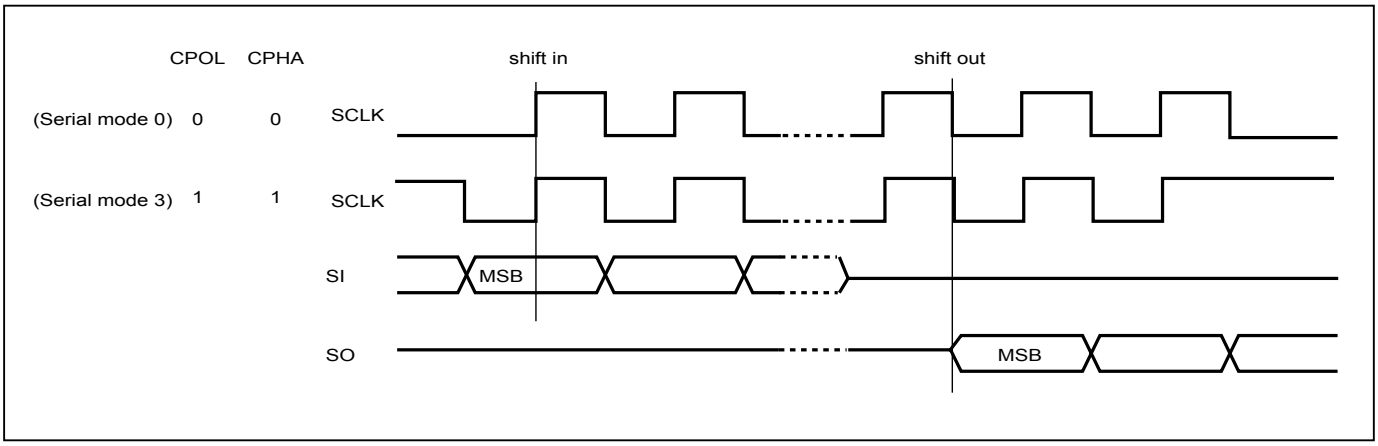
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDCR, RDSCUR, READ, FAST_READ, DREAD, 2READ, 4READ, QREAD, RDSFDP, RES, REMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, SUSPEND, RESUME, NOP, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

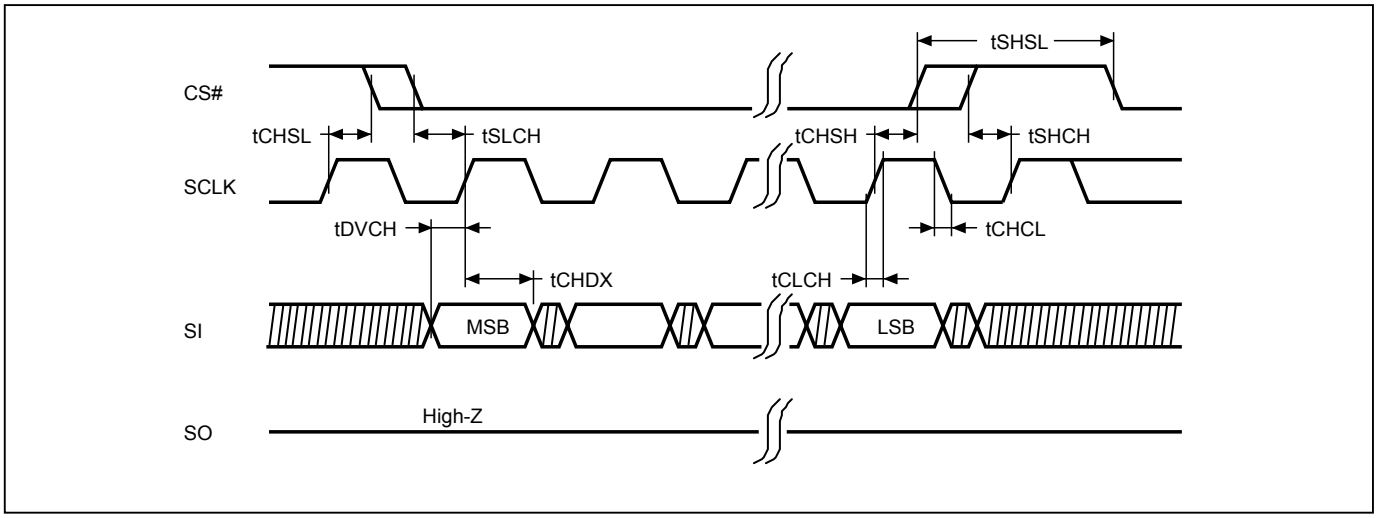
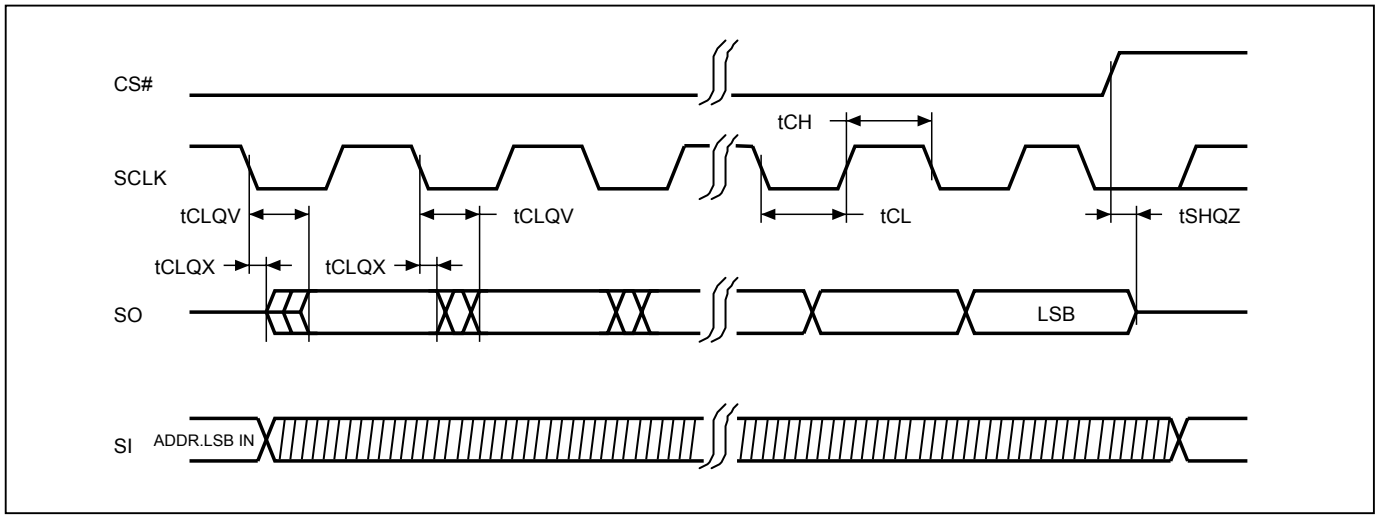


Figure 3. Output Timing

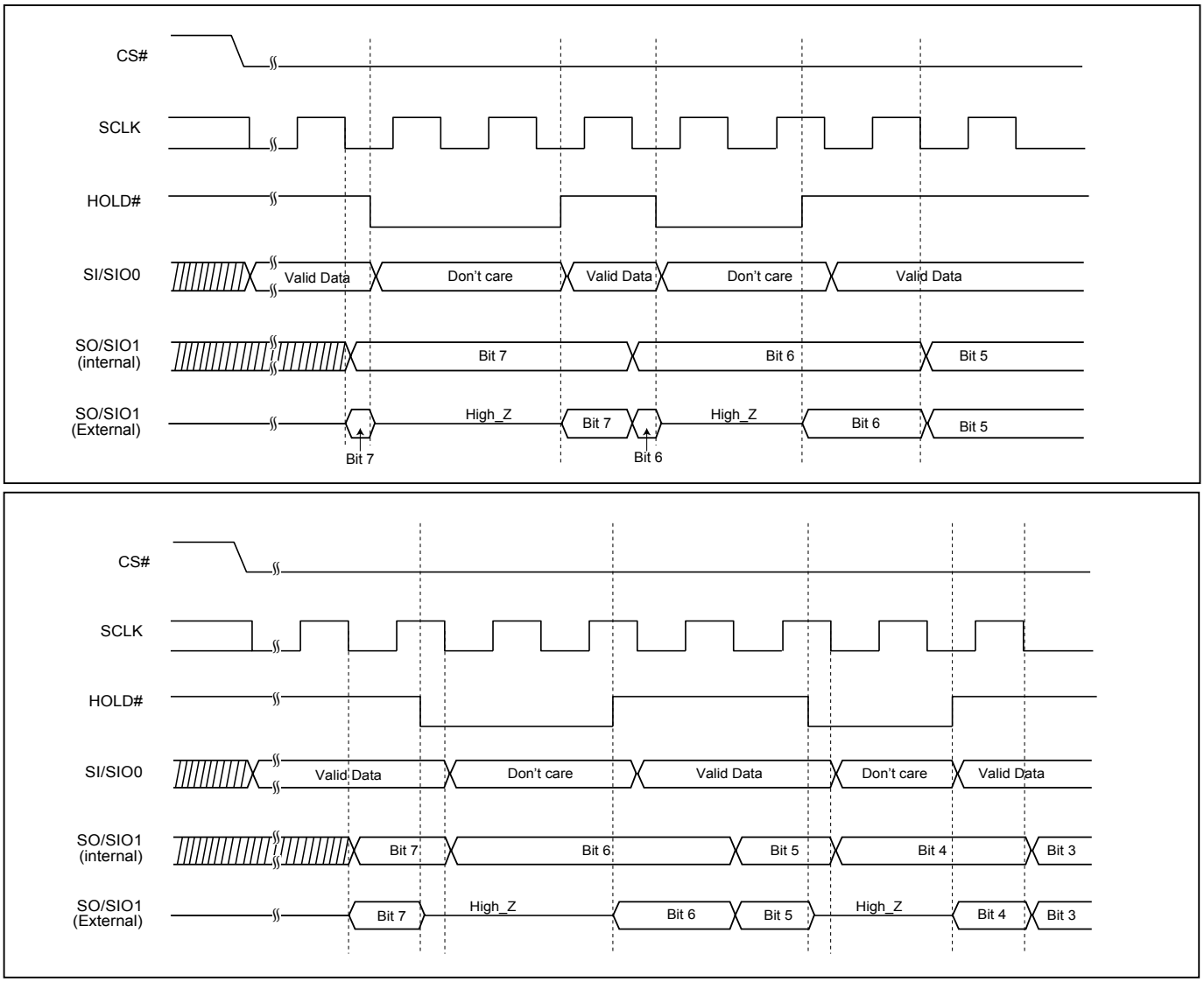


9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 4. Hold Condition Operation



During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

10. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

I/O	1	1	2	2	4	4
Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	4READ (4 x I/O read)	QREAD (1I/4O read)
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy	Dummy	Dummy	Dummy	Dummy
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual Output until CS# goes high	Quad I/O read with 6 dummy cycles	n bytes read out by Quad output until CS# goes high

I/O	1	4	1	1	1	1	1
Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)	RDSFDP (Read SFDP)
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)	5A (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1		ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2		ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3		ADD3
5th byte							Dummy
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32KB block	to erase the selected block	to erase whole chip	Read SFDP mode

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status register)	PGM/ERS Suspend (Suspends Program/Erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	75 or B0 (hex)
2nd byte					Values	
3rd byte					Values	
4th byte					Values	
5th byte						
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register -1 & configuration register -2	to write new values of the configuration/ status register	program/erase operation is interrupted by suspend command

Command (byte)	PGM/ERS Resume (Resumes Program/Erase)	DP (Deep power down)	SBL (Set Burst Length)
1st byte	7A or 30 (hex)	B9 (hex)	C0 (hex)
2nd byte			Value
3rd byte			
4th byte			
5th byte			
Action	to continue performing the suspended program/erase sequence	enters deep power down mode	to set Burst length

ID/Reset Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)
1st byte	9F (hex)	AB (hex)	90 (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte		x	x				
3rd byte		x	x				
4th byte		x	ADD *(Note 1)*				
5th byte							
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 8K-bit secured OTP mode	to exit the 8K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

COMMAND (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			*(Note 3)*

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

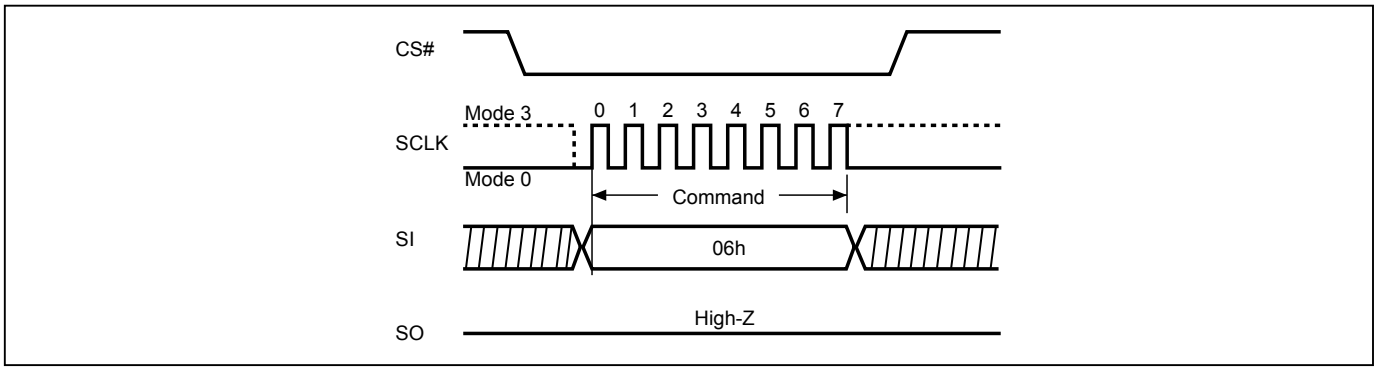
10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

The SIO[3:1] are "don't care" .

Figure 5. Write Enable (WREN) Sequence



10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

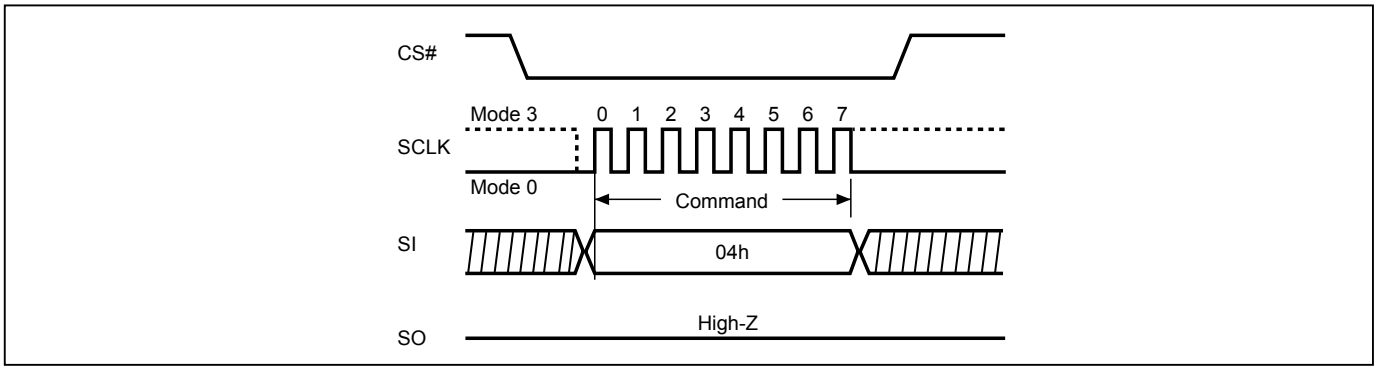
The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Program/Erase Suspend
- Completion of Softreset command
- Completion of Write Security Register (WRSCUR) command

Figure 6. Write Disable (WRDI) Sequence



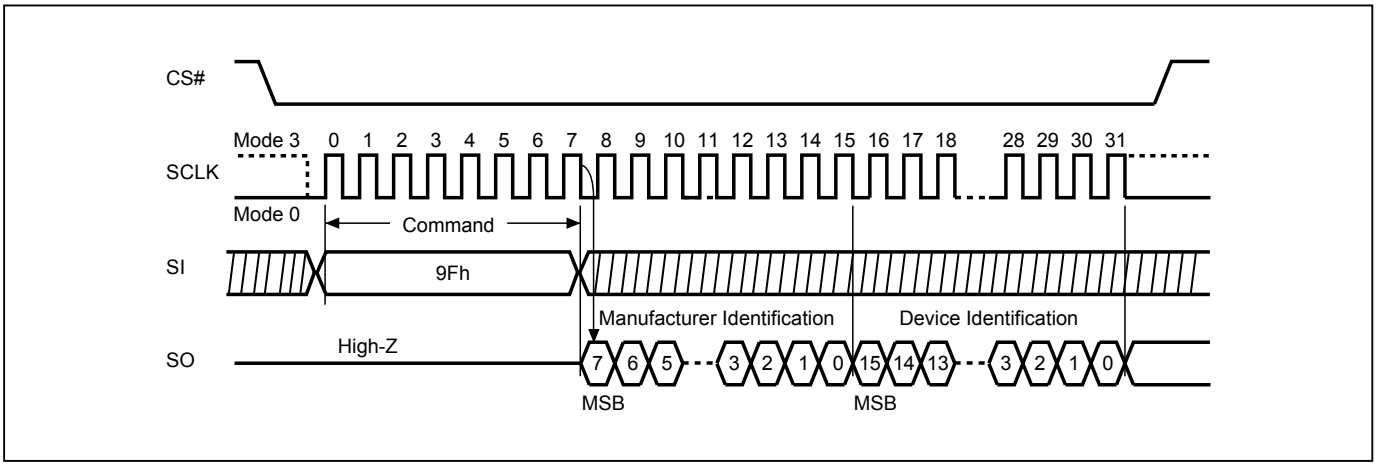
10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 6. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 7. Read Identification (RDID) Sequence



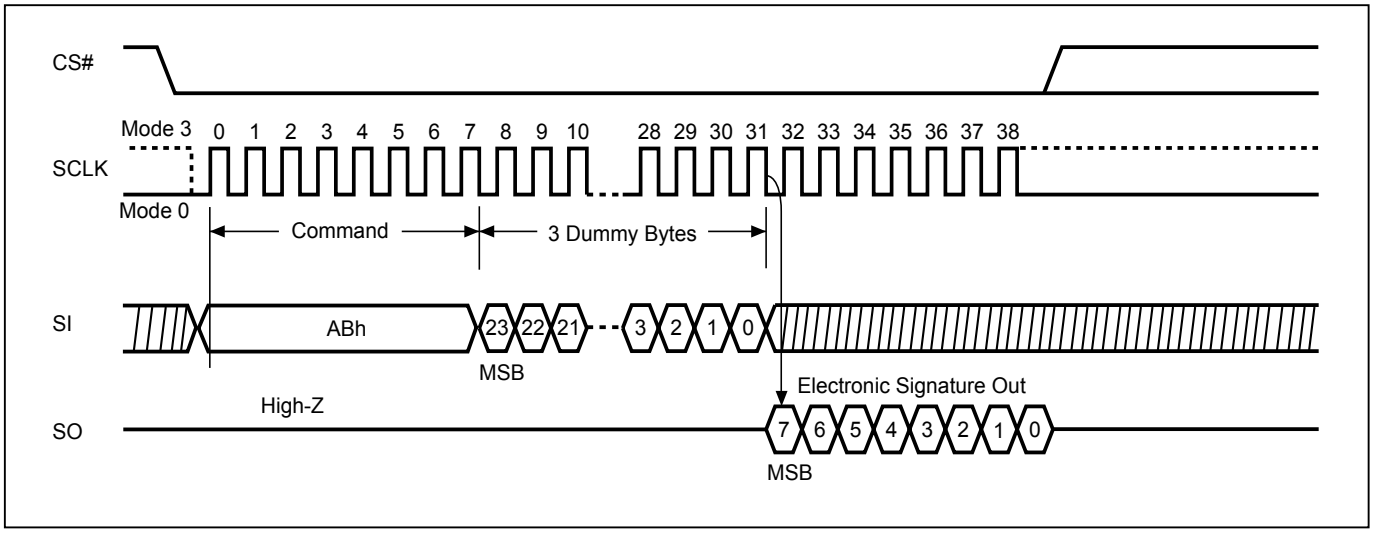
10-4. Read Electronic Signature (RES)

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The SIO[3:1] are "don't care".

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low.

Figure 8. Read Electronic Signature (RES) Sequence

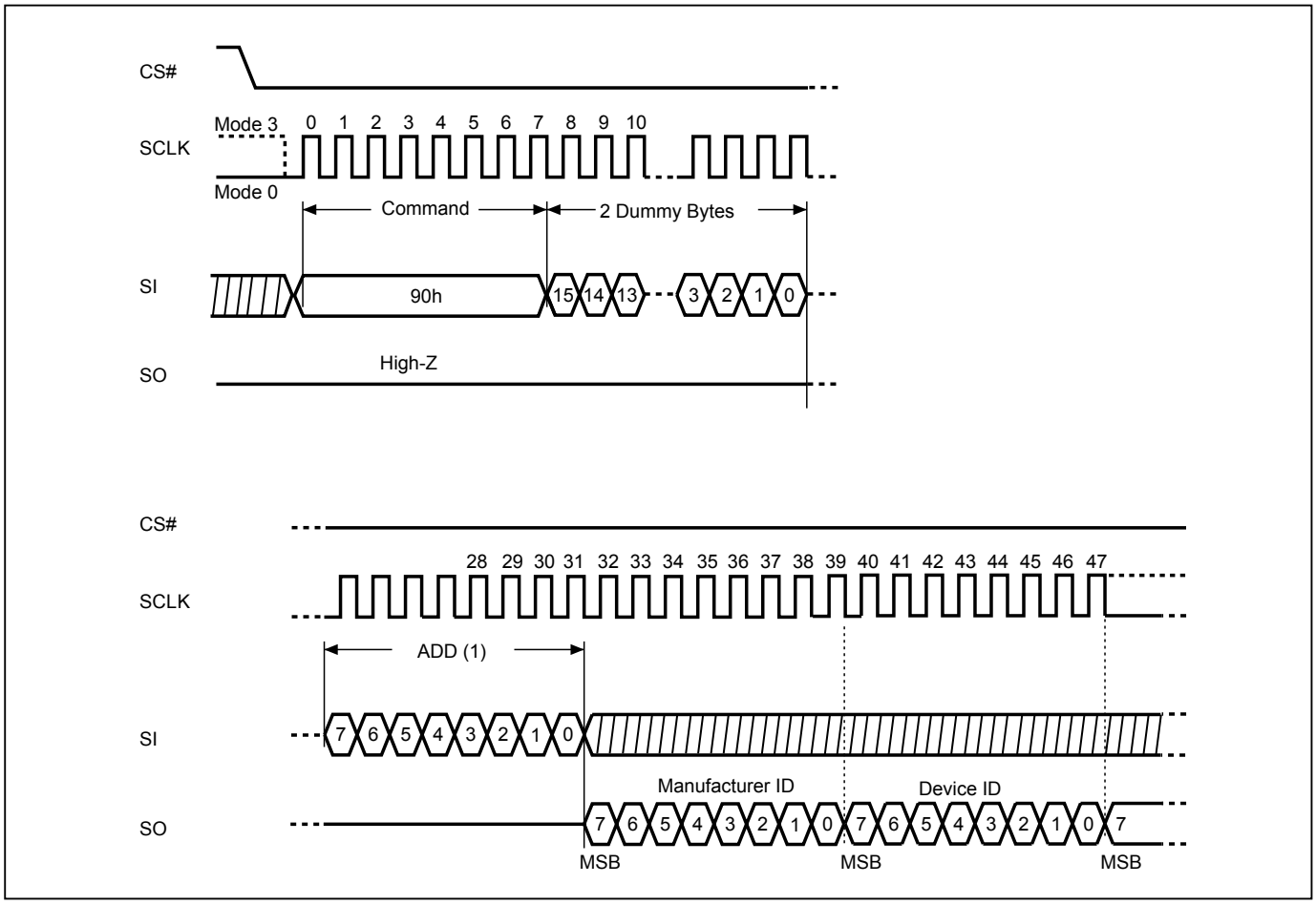


10-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 6. ID Definitions".*

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 9. Read Electronic Manufacturer & Device ID (REMS) Sequence



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

10-6. ID Read

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Table 6. ID Definitions

Command Type	Command	MX25R4035F		
RDID	9Fh	Manufacturer ID	Memory type	Memory density
		C2	28	13
RES	ABh	Electronic ID		
		13		
REMS	90h	Manufacturer ID	Device ID	
		C2	13	