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MX25U5121E, MX25U1001E

DATASHEET

Contents

512K-BIT [x 1/x 2/x 4] CMOS MXSMIO® SERIAL FLASH MEMORY
1M-BIT [x 1/x 2/x 4] CMOS MXSMIO® SERIAL FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 512Kb: 524,288 x 1 bit structure or 262,144 x 2 bit structure or 131,072 x 4 bit structure
  1Mb: 1,048,576 x 1 bit structure or 524,288 x 2 bit structure or 262,144 x 4 bit structure
- 16 Equal Sectors with 4K bytes each (512Kb)
  32 Equal Sectors with 4K bytes each (1Mb)
  - Any Sector can be erased individually
- 1 Equal Blocks with 64K bytes each (512Kb)
  2 Equal Blocks with 64K bytes each (1Mb)
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (32 bytes)
- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- Performance
  - Normal Read:
    - 30MHz
  - Fast Read:
    - 1 I/O: 70MHz with 8 dummy cycles
    - 2 I/O: 70MHz with 8 dummy cycles, equivalent to 140MHz
    - 4 I/O: 60MHz with 6 dummy cycles, equivalent to 240MHz
  - Fast program time: 140us(typ.) and 400us(max.)/page
  - Fast erase time: 55ms (typ.)/sector ; 400ms (typ.)/block
- Low Power Consumption
  - Low active read current: 4mA(max.) at 30MHz, 8mA(max.) at 70MHz
  - Low active programming current: 11mA (max.)
  - Low active erase current: 12mA (max.)
  - Low standby current: 8uA (typ.)
  - Deep power down current: 2uA (typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Block Lock protection
  - The BP0~BP1 status bits defines the size of the area to be software protected against Program and Erase instructions
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the

program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-bytes device ID

HARDWARE FEATURES
- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or Serial Data Input/Output for 4 x I/O read mode
- HOLD#/SIO3
  - Pause the chip without diselecting the chip or Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-pin TSSOP (173mil)
  - 8-USON (2x3mm)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

The device feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

The device provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector locations will be executed. Program command is executed on page (32 bytes) basis, and erase command is executes on sector, or block, or whole chip.

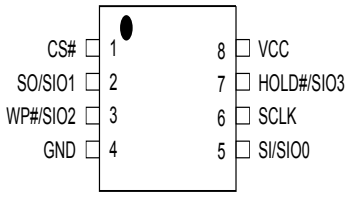
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in Standby Mode and draws less than 20uA (typical: 8uA) DC current.

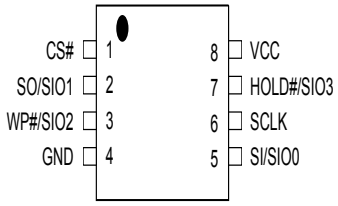
The device utilizes Macronix proprietary memory cell, which reliably stores memory contents even after typical 100,000 program and erase cycles.

3. PIN CONFIGURATIONS

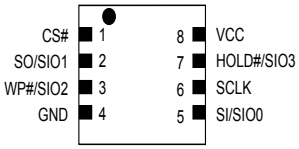
8-PIN SOP (150mil)



8-PIN TSSOP (173mil)



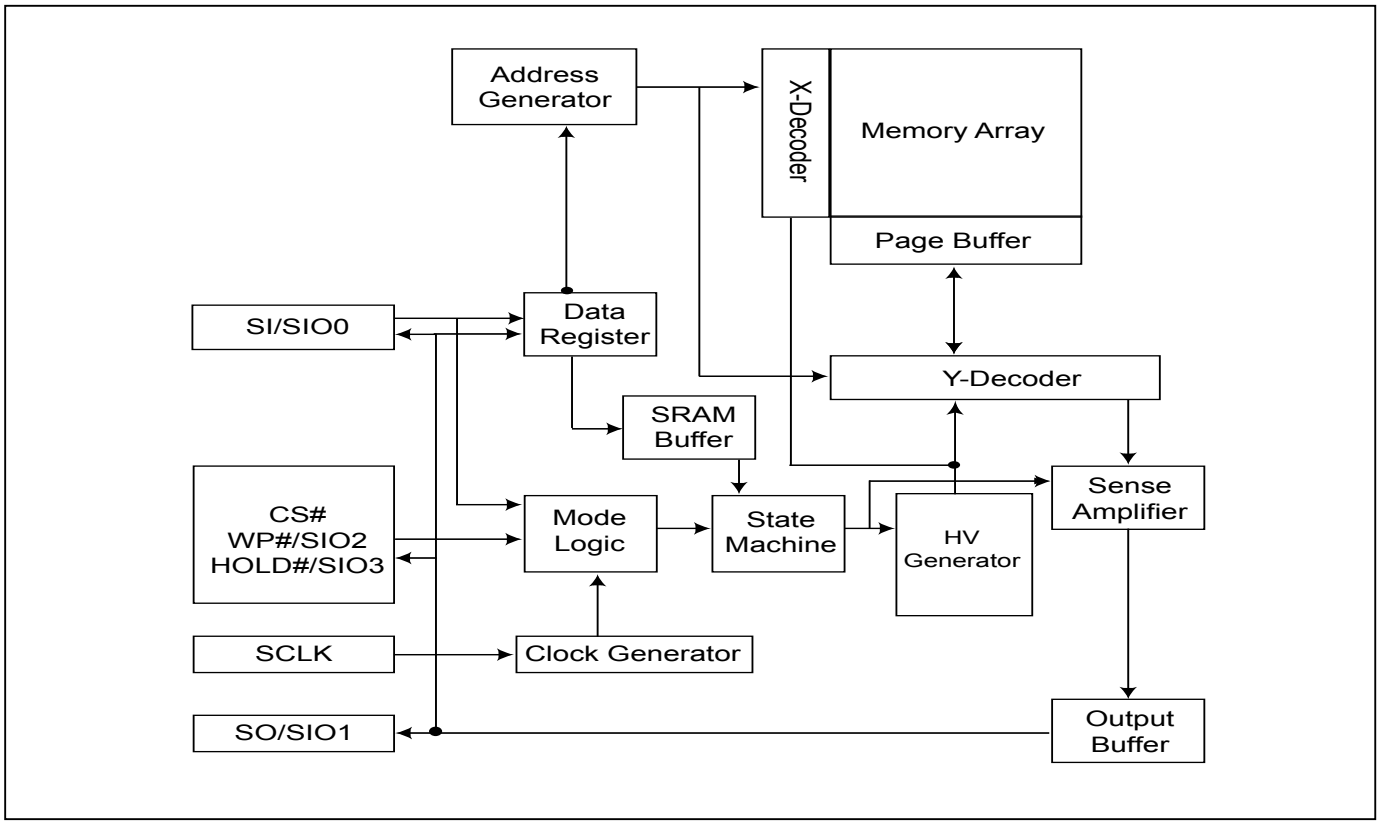
8-LAND USON (2x3mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
SO/SIO1	Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
SCLK	Clock Input
HOLD#/SIO3	Pause the chip without diselecting the chip or Serial Data Input/Output for 4 x I/O read mode
WP#/SIO2	Hardware write protection or Serial Data Input/Output for 4 x I/O read mode
VCC	+1.8V Power Supply
GND	Ground

5. BLOCK DIAGRAM



6. MEMORY ORGANIZATION

Table 1. Memory Organization (512Kb)

Block	Sector	Address Range	
0	15	00F000h	00FFFFh
	:	:	:
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Table 2. Memory Organization (1Mb)

Block	Sector	Address Range	
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

7. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes Standby Mode and keeps the Standby Mode until next CS# falling edge. In Standby Mode, all SO pins of this LSI should be High-Z.

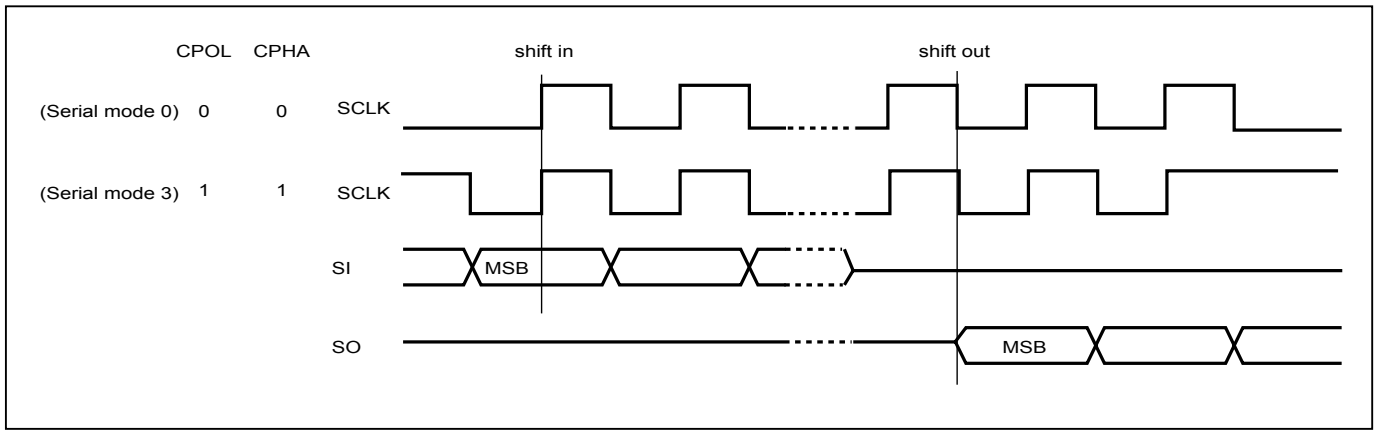
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, READ, FAST_READ and 4READ the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP, and DP the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Program, Erase operation, to access the memory array is neglected and not affect the current operation of Program and Erase.

Figure 1. Serial Modes Supported



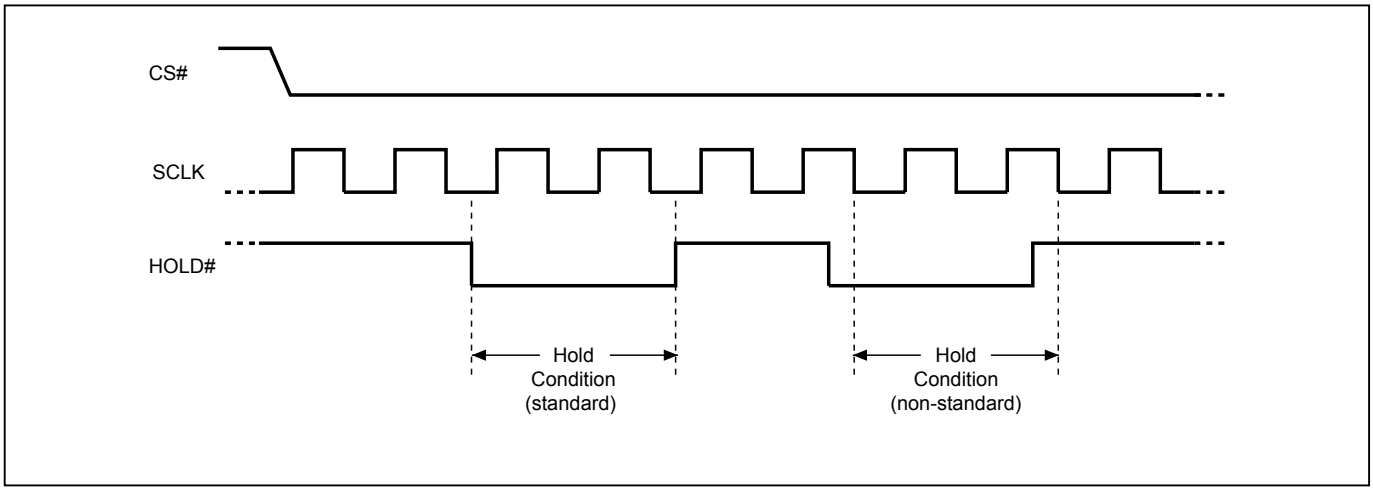
Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

8. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see*"Figure 2. Hold Condition Operation"*.

Figure 2. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

9. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC powerup and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Software Protection Mode (SPM): by using BP0-BP1 bits to set the part of Flash protected from data change.

- Hardware Protection Mode (HPM): by using WP# going low to protect the BP0-BP1 bits and SRWD bit from data change.

- Deep Power Down Mode: By entering Deep Power Down Mode, the flash device also is under protected from writing all commands except Release from Deep Power Down Mode command (RDP).

Table 3. Protected Area Sizes

Status bit		Protect level	
BP1	**BP0**	**MX25U5121E**	**MX25U1001E**
0	0	0 (none)	0 (none)
0	1	1 (All)	1 (1 block)
1	0	2 (All)	2 (All)
1	1	3 (All)	3 (All)

10. COMMAND DESCRIPTION

Table 4. Command Set

Command (byte)	WREN (write enable)	WRDI (write disable)	WRSR (write status register)	RDID (read identific-ation)	RDSR (read status register)	READ (read data)	FAST READ (fast read data)
1st byte	06 (hex)	04 (hex)	01 (hex)	9F (hex)	05 (hex)	03 (hex)	0B (hex)
2nd byte						AD1	AD1
3rd byte						AD2	AD2
4th byte						AD3	AD3
5th byte							Dummy
Data Cycles							
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to write new values of the status register	outputs JEDEC ID: 1-byte Manufacturer ID & 2-bytes Device ID	to read out the values of the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high

Command (byte)	DREAD (1I/2O read)	4READ (4 I/O read)	SE (sector erase)	BE (block erase)	CE (chip erase)	PP (page program)	DP (Deep power down)
1st byte	3B (hex)	EB (hex)	20 (hex)	52 or D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)
2nd byte	AD1	AD1	AD1	AD1		AD1	
3rd byte	AD2	AD2	AD2	AD2		AD2	
4th byte	AD3	AD3	AD3	AD3		AD3	
5th byte	Dummy	Dummy					
Data Cycles						1-32	
Action	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	to erase the selected sector	to erase the selected block	to erase whole chip	to program the selected page	enters Deep Power Down Mode

Command (byte)	RDP (Release from deep power down)
1st byte	AB (hex)
2nd byte	
3rd byte	
4th byte	
5th byte	
Data Cycles	
Action	release from Deep Power Down Mode

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 2: Value "0" should be input to the un-used significant bits of address bits by user (e.g. A17~A23(MSB) in MX25U1001E ; A16-A23(MSB) in MX25U5121E)

10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE, CE and WRSR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→CS# goes high. (Please refer to *"Figure 11. Write Enable (WREN) Sequence (Command 06)"*)

10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high. (Please refer to *"Figure 12. Write Disable (WRDI) Sequence (Command 04)"*)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-bytes.
The Macronix Manufacturer ID is C2(hex), the memory type ID is 25(hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as *"Table 5. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (Please refer to *"Figure 13. Read Identification (RDID) Sequence (Command 9F)"*)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at Standby Mode.

Table 5. ID Definitions

RDID Command	MX25U5121E			MX25U1001E		
	manufacturer ID	memory type	memory density	manufacturer ID	memory type	memory density
	C2	25	30	C2	25	31

10-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program or erase operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→sending RDSR instruction code→Status Register data out on SO (Please refer to *"Figure 14. Read Status Register (RDSR) Sequence (Command 05)"*)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase progress. When WIP bit sets to 1, which means the device is busy in program/erase progress. When WIP bit sets to 0, which means the device is not in progress of program/erase register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase instruction.

BP1, BP0 bits. The Block Protect (BP1, BP0) bits, volatile bits, indicate the protected area(as defined in *"Table 3. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed)

QE bit. The Quad Enable (QE) bit, volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the features of HPM and HOLD will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP1, BP0) are read only.

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	Reserved	Reserved	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	0	0	*(note 1)*	*(note 1)*	1=write enable 0=not write enable	1=write operation 0=not in write operation

Note: 1. See the *"Table 3. Protected Area Sizes"*. The default BP0-BP1 values are "1" (protected).
2. The SRWD default value is "0"

10-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP1, BP0) bits to define the protected area of memory (as shown in *"Table 3. Protected Area Sizes"*). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (see *"Figure 15. Write Status Register (WRSR) Sequence (Command 01)"*)

The WRSR instruction has no effect on b5, b4, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 7. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP1 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP1 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *"Table 3. Protected Area Sizes"*.

As the table above showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP1, BP0. The protected area, which is defined by BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP1, BP0. The protected area, which is defined by BP1, BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note:
- To exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP1, BP0.
- If the system had entered the Quad I/O (QE=1) mode, the feature of HPM will be disabled.

10-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fC. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction.

This product does not provide the function of read around. After reading through density 512Kb or 1Mb, CS# must go high. Otherwise, the data correctness will not be guaranteed. If the device needs to read data again, it must issue read command once more.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-bytes address on SI→data out on SO→to end READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 16. Read Data Bytes (READ) Sequence (Command 03)"*)

10-7. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→ 8 dummy cycles on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 17. Read at Higher Speed (FAST_READ) Sequence (Command 0B)"*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

10-8. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out. (Please refer to *"Figure 18. Dual Read Mode Sequence (Command 3B)"*)

10-9. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of Status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 x I/O pins) shift out on the falling edge of SCLK at a maximum frequency fC. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 19. 4 x I/O Read Mode Sequence (Command EB)"*)

10-10. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-bytes sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *"Table 1. Memory Organization (512Kb)"* and *"Table 2. Memory Organization (1Mb)"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the eighth bit of last address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→sending SE instruction code→3-bytes address on SI →CS# goes high. (Please refer to *"Figure 20. Sector Erase (SE) Sequence (Command 20)"*)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

10-11.Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte sector erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see *"Table 1. Memory Organization (512Kb)"* and *"Table 2. Memory Organization (1Mb)"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence is shown as *"Figure 21. Block Erase (BE) Sequence (Command D8 or 52)"*.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

10-12. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see *"Table 1. Memory Organization (512Kb)"* and *"Table 2. Memory Organization (1Mb)"*) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence is shown as *"Figure 22. Chip Erase (CE) Sequence (Command 60 or C7)"*.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

10-13. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). After the instruction and address input, data to be programmed is input sequentially. The internal sequence controller will sequentially program the data from the initial address. If the transmitted data goes beyond the page boundary, the internal sequence controller may not function properly and the content of the device will not be guaranteed. Therefore, If the initial A4-A0 (The five least significant address bits) are set to all 0, maximum 32 bytes of data can be input sequentially. If the initial address A4-A0 (The five least significant address bits) are not set to all 0, maximum bytes of data input will be the subtraction of the initial address A4-A0 from 32bytes. The data exceeding 32bytes data is not sent to device. In this case, data is not guaranteed.

The sequence of issuing PP instruction is: CS# goes low → sending PP instruction code → 3-bytes address on SI→ at least 1-byte on data on SI → CS# goes high. (Please refer to *"Figure 23. Page Program (PP) Sequence (Command 02)"*)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

10-14. Deep Power-Down (DP)

The Deep Power Down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power Down Mode), the standby current is reduced from ISB1 to ISB2. The Deep Power Down Mode requires the Deep Power Down (DP) instruction to enter, during the Deep Power Down Mode, the device is not active and all Read/Write/Program/Erase instruction are ignored.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→ CS# goes high. (Please refer to *"Figure 24. Deep Power Down (DP) Sequence (Command B9)"*)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power Down Mode (RDP) instruction. When Power-down, the Deep Power Down Mode automatically stops, and when power-up, the device automatically is in Standby Mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power Down Mode.

10-15. Release from Deep Power-Down (RDP)

The Release from Deep Power Down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Standby Mode. If the device was not previously in the Deep Power Down Mode, the transition to the Standby Mode is immediate. If the device was previously in the Deep Power Down Mode, though, the transition to the Standby Mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 9. AC CHARACTERISTICS"*. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

The sequence is shown as *"Figure 25. Release from Deep Power Down (RDP) Sequence (Command AB)"*. Even in Deep Power Down Mode, the RDP is also allowed to be executed, only except the device is in progress of program/erase cycle; there's no effect on the current program/erase cycle in progress.

11. POWER-ON STATE

The device is at below states when power-up:
- Standby Mode (please note it is not Deep Power Down Mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

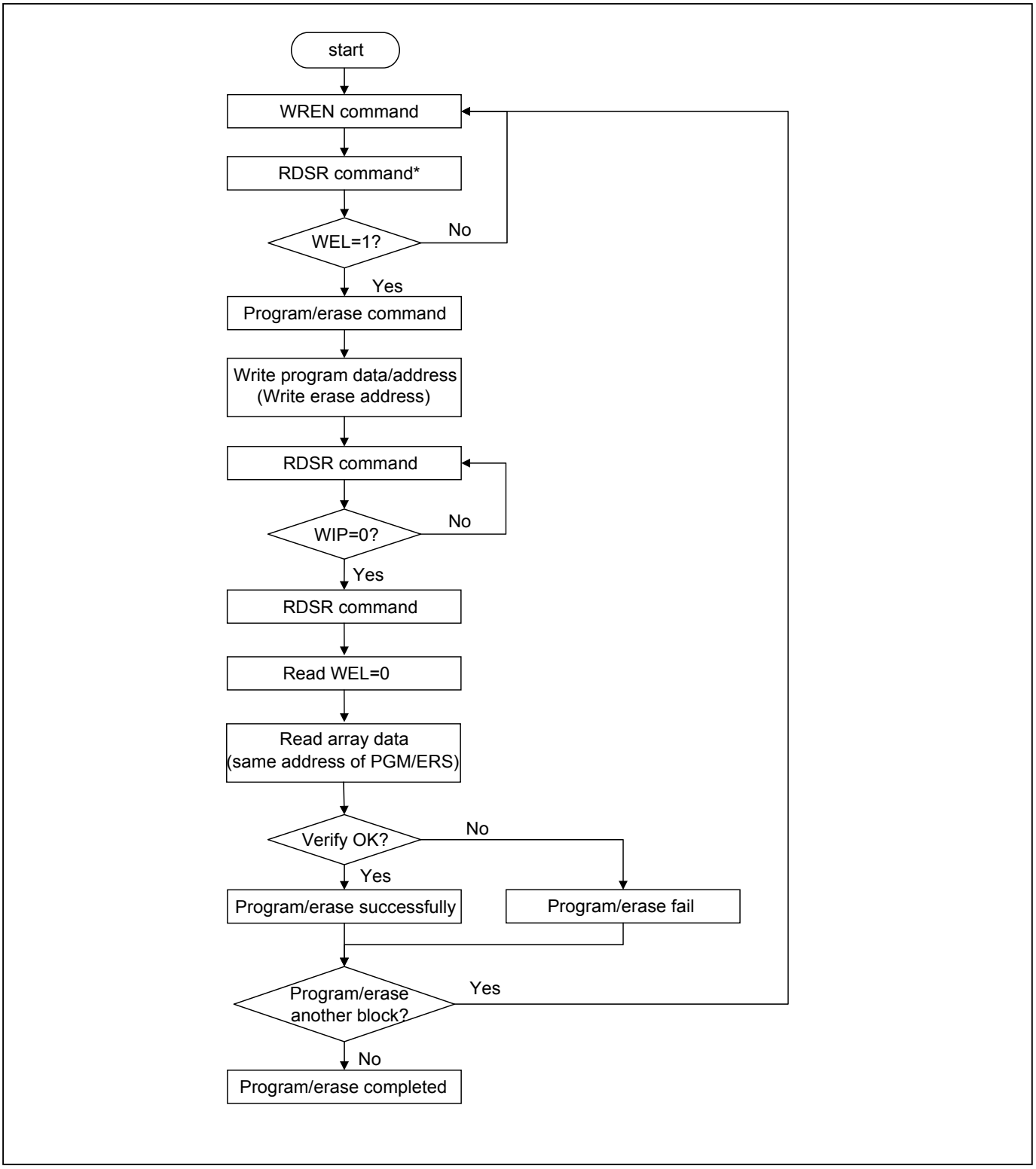
Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

Figure 3. Program/Erase flow with read array data



12. ELECTRICAL SPECIFICATIONS

12-1. ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 2.5V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 4. Maximum Negative Overshoot Waveform

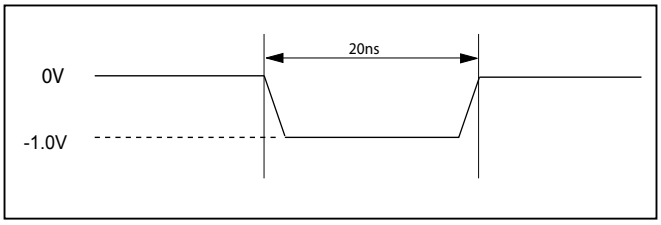
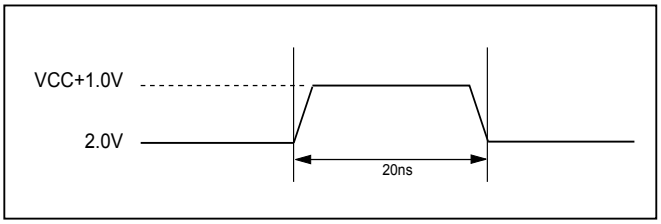


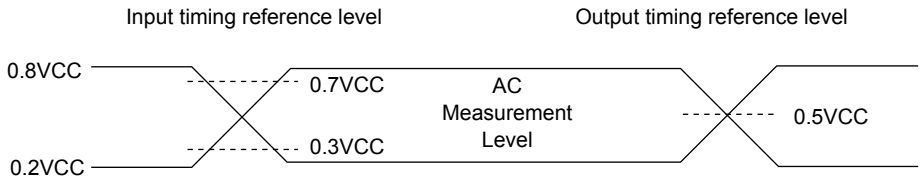
Figure 5. Maximum Positive Overshoot Waveform



12-2. CAPACITANCE TA = 25°C, f = 1.0 MHz

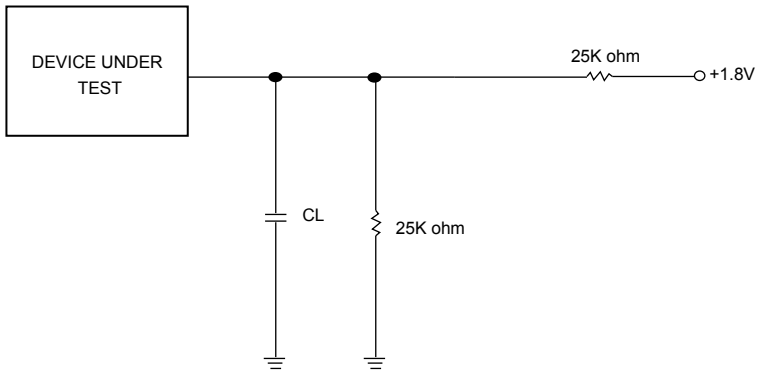
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 6. Input Test Waveforms and Measurement Level



Note: Input pulse rise and fall time are <5ns

Figure 7. Output Loading



CL=30pF Including jig capacitance

Table 8. DC CHARACTERISTICS

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		8	20	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power Down Current			2	10	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		4	8	mA	f=70MHz, (1 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				6	12	mA	f=60MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				2	4	mA	f=30MHz, (1 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		9	11	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Register (WRSR) Current	1		0.4	0.7	mA	Program Status Register in Progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		9	12	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.2VCC	V	
VIH	Input High Voltage		0.8VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA
VWI	Command Inhibit Voltage	3	1.0		1.4	V	

Notes :
1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. Not 100% tested.

Table 9. AC CHARACTERISTICS

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RDP, WREN, WRDI, RDID, RDSR, WRSR		DC		70	MHz
fRSCLK	fR	Clock Frequency for READ instruction		DC		30	MHz
fTSCLK	fT	Clock Frequency for DREAD instruction		DC		70	MHz
	fQ	Clock Frequency for 4READ instruction		DC		60	MHz
tCH(1)	tCLH	Clock High Time	Serial (fSCLK)	7			ns
			Normal Read (fRSCLK)	15			ns
tCL(1)	tCLL	Clock Low Time	Serial (fSCLK)	7			ns
			Normal Read (fRSCLK)	15			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		5			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		2			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5			ns
tSHSL(4)	tCSH	CS# Deselect Time	Read	10			ns
			Write/Erase/Program	20			ns
tSHQZ(2)	tDIS	Output Disable Time				8	ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)		5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)		5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)		5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)		5			ns
tHHQX	tLZ	HOLD# to Output Low-Z				8	ns
tHLQZ	tHZ	HOLD# to Output High-Z				8	ns
tCLQV	tV	Clock Low to Output Valid	@ 30pF			8	ns
			@ 15pF			6	ns
tCLQX	tHO	Output Hold Time		2			ns
tWHSL(4)		Write Protect Setup Time		20			ns
tSHWL(4)		Write Protect Hold Time		100			ns
tDP(2)		CS# High to Deep Power Down Mode				8	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				5	us
tW		Write Status Register Cycle Time			100	150	ns
tPP		Page Program Cycle Time (32 Bytes)			0.14	0.4	ms
tSE		Sector Erase Cycle Time (4K Bytes)			55	200	ms
tBE		Block Erase Cycle Time			0.4	1.2	s
tCE		Chip Erase Cycle Time	512Kb		0.4	1.2	s
			1Mb		0.8	2.4	s

Notes:
1. tCH + tCL must be greater than or equal to 1/ f (fC).
2. Value guaranteed by characterization, not 100% tested in production.
3. Test condition is shown as *"Figure 6. Input Test Waveforms and Measurement Level" & "Figure 7. Output Loading"*.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

13. Timing Analysis

Figure 8. Serial Input Timing

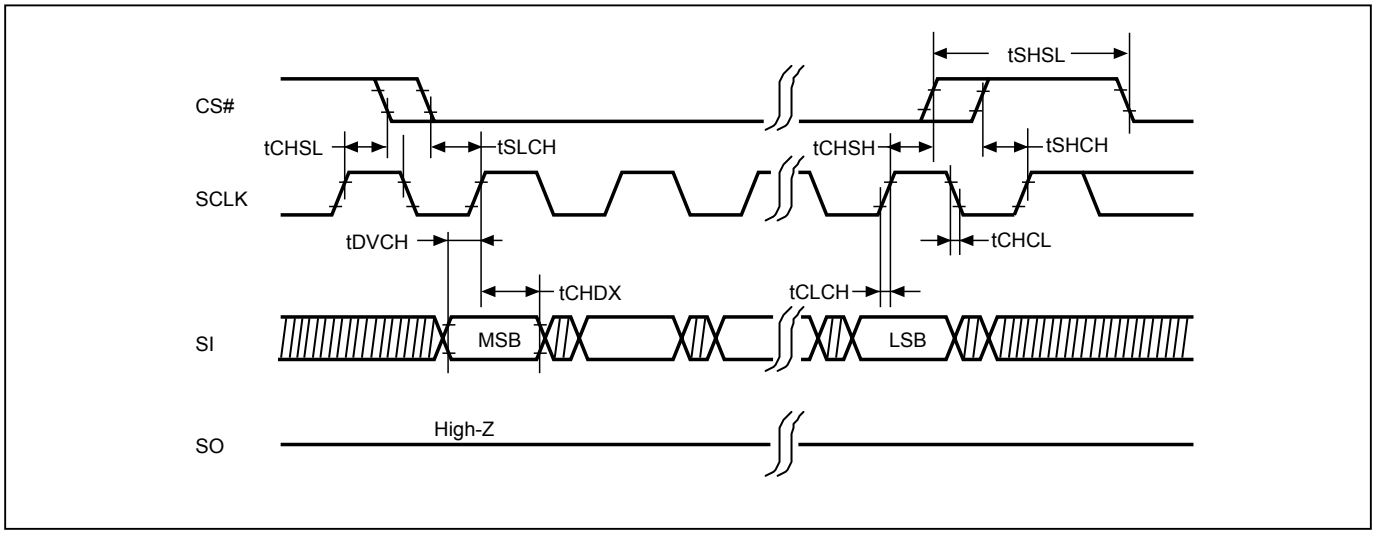


Figure 9. Output Timing