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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MACRONIX
INTERNATIONAL Co., LTD.

MX25U12835F

MX25U12835F

DATASHEET

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1.8V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO™ (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 134,217,728 x 1 bit structure or 67,108,864 x 2 bits (two I/O mode) structure or 33,554,432 x 4 bits (four I/O mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
 - Any Block can be erased individually
- Single Power Supply Operation
 - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V

PERFORMANCE

- High Performance
 - Fast read for SPI mode
 - 1 I/O: 104MHz with 8 dummy cycles
 - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
 - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
 - Fast read for QPI mode
 - 4 I/O: 84MHz with 2+2 dummy cycles, equivalent to 336MHz
 - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
 - Fast program time: 1.2ms(typ.) and 3ms(max.)/page (256-byte per page)
 - Byte program time: 12us (typical)
 - 8/16/32/64 byte Wrap-Around Burst Read Mode
 - Fast erase time: 60ms (typ.)/sector (4K-byte per sector); 250ms(typ.)/block (32K-byte per block), 500ms(typ.) / block (64K-byte per block)
- Low Power Consumption
 - Low active read current: 20mA(typ.) at 104MHz, 15mA(typ.) at 84MHz
 - Low active erase/programming current: 20mA (typ.)
 - Standby current: 30uA (typ.)
- Deep Power Down: 5uA(typ.)
- Typical 100,000 erase/program cycles
- 10 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
 - Additional 4k-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
 - Automatically erases and verifies data at selected sector or block
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)

- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID
 - RES command for 1-byte Device ID
 - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SIO0
 - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
 - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
 - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- RESET#/SIO3
 - Hardware Reset pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
 - 16-pin SOP (300mil)
 - 8-land WSON (6x5mm)
 - 8-land WSON (8x6mm)
 - **All devices are RoHS Compliant**

2. GENERAL DESCRIPTION

MX25U12835F is 128Mb bits serial Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108,864 bits x 2 or 33,554,432 bits x 4. MX25U12835F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and Reset# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U12835F MXSMIO™ (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 30uA DC current.

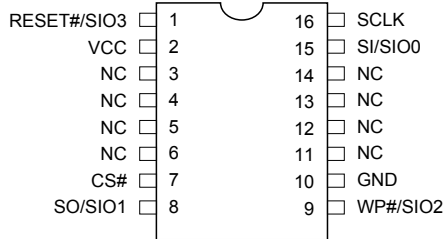
The MX25U12835F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

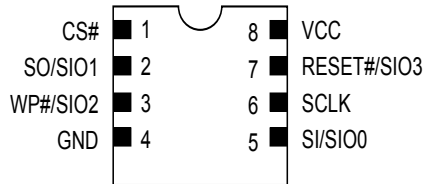
Part Name	Additional Features	Protection and Security		Read Performance			
				SPI			QPI
		Flexible Block Protection (BP0-BP3)	4K-bit security OTP	1 I/O	2 I/O	4 I/O	4 I/O
Dummy Cycle	-	-	8	4	6	4	6
MX25U12835F	V	V	104 MHz	84 MHz	104 MHz	84 MHz	104 MHz

3. PIN CONFIGURATIONS

16-PIN SOP (300mil)

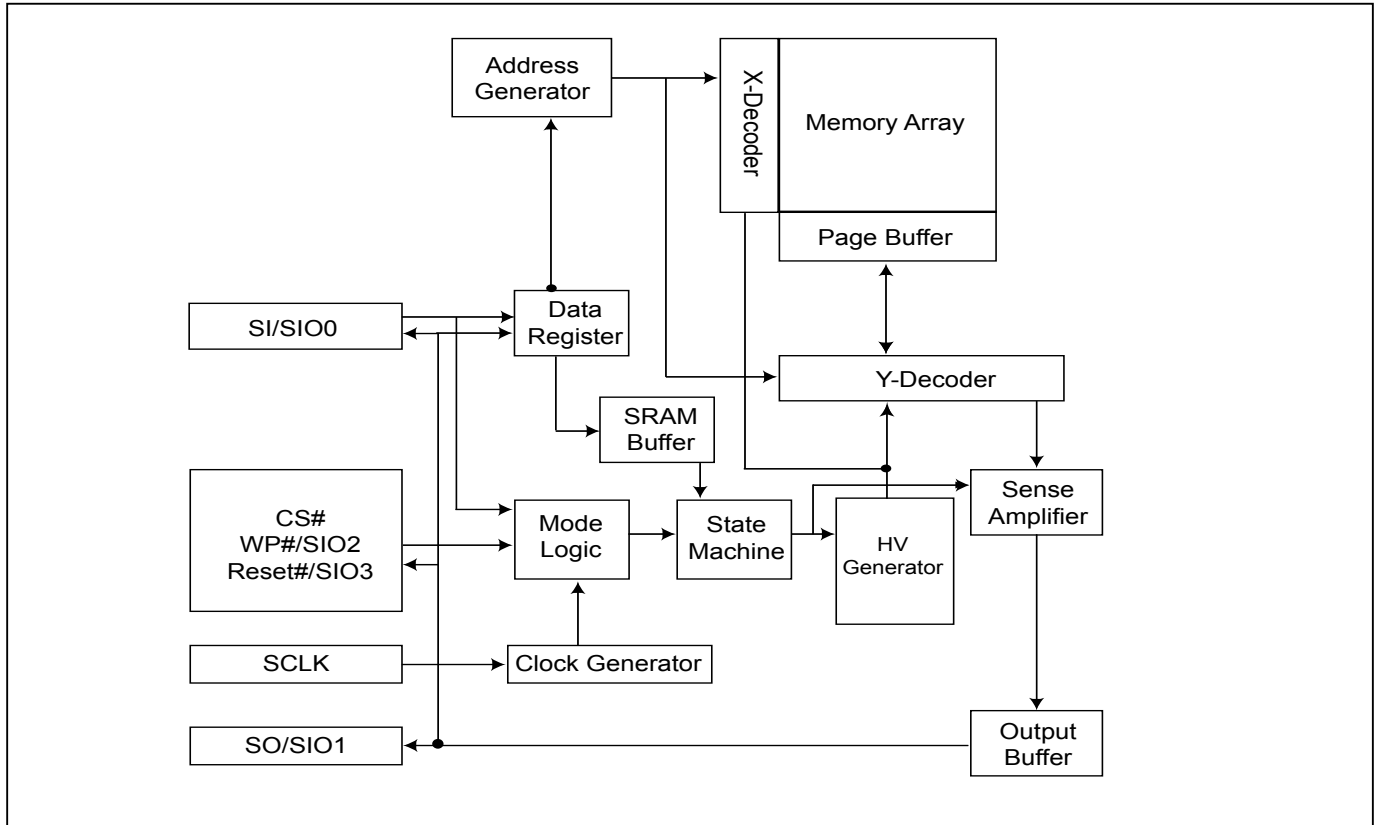


8-WSON (6x5mm, 8x6mm)



4. PIN DESCRIPTION

Symbol	Description
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
RESET#/SIO3	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground

5. BLOCK DIAGRAM

6. DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
 - Power-up
 - Reset# pin driven low
 - Write Disable (WRDI) command completion
 - Write Status Register (WRSR) command completion
 - Page Program (PP) command completion
 - Sector Erase (SE) command completion
 - Block Erase 32KB (BE32K) command completion
 - Block Erase (BE) command completion
 - Chip Erase (CE) command completion
 - Program/Erase Suspend
 - Softreset command completion
 - Write Security Register (WRSCUR) command completion
 - Write Protection Selection (WPSEL) command completion
- Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as [Table 2](#) Protected Area Sizes, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 255th)
0	0	1	0	2 (2 blocks, protected block 254th~255th)
0	0	1	1	3 (4 blocks, protected block 252nd~255th)
0	1	0	0	4 (8 blocks, protected block 248th~255th)
0	1	0	1	5 (16 blocks, protected block 240th~255th)
0	1	1	0	6 (32 blocks, protected block 224th~255th)
0	1	1	1	7 (64 blocks, protected block 192nd~255th)
1	0	0	0	8 (128 blocks, protected block 128th~255th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th~1th)
0	0	1	1	3 (4 blocks, protected block 0th~3rd)
0	1	0	0	4 (8 blocks, protected block 0th~7th)
0	1	0	1	5 (16 blocks, protected block 0th~15th)
0	1	1	0	6 (32 blocks, protected block 0th~31st)
0	1	1	1	7 (64 blocks, protected block 0th~63rd)
1	0	0	0	8 (128 blocks, protected block 0th~127th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to [Table 8](#) of "security register definition" for security register bit definition and [Table 3](#) of "4K-bit secured OTP definition" for address range definition.

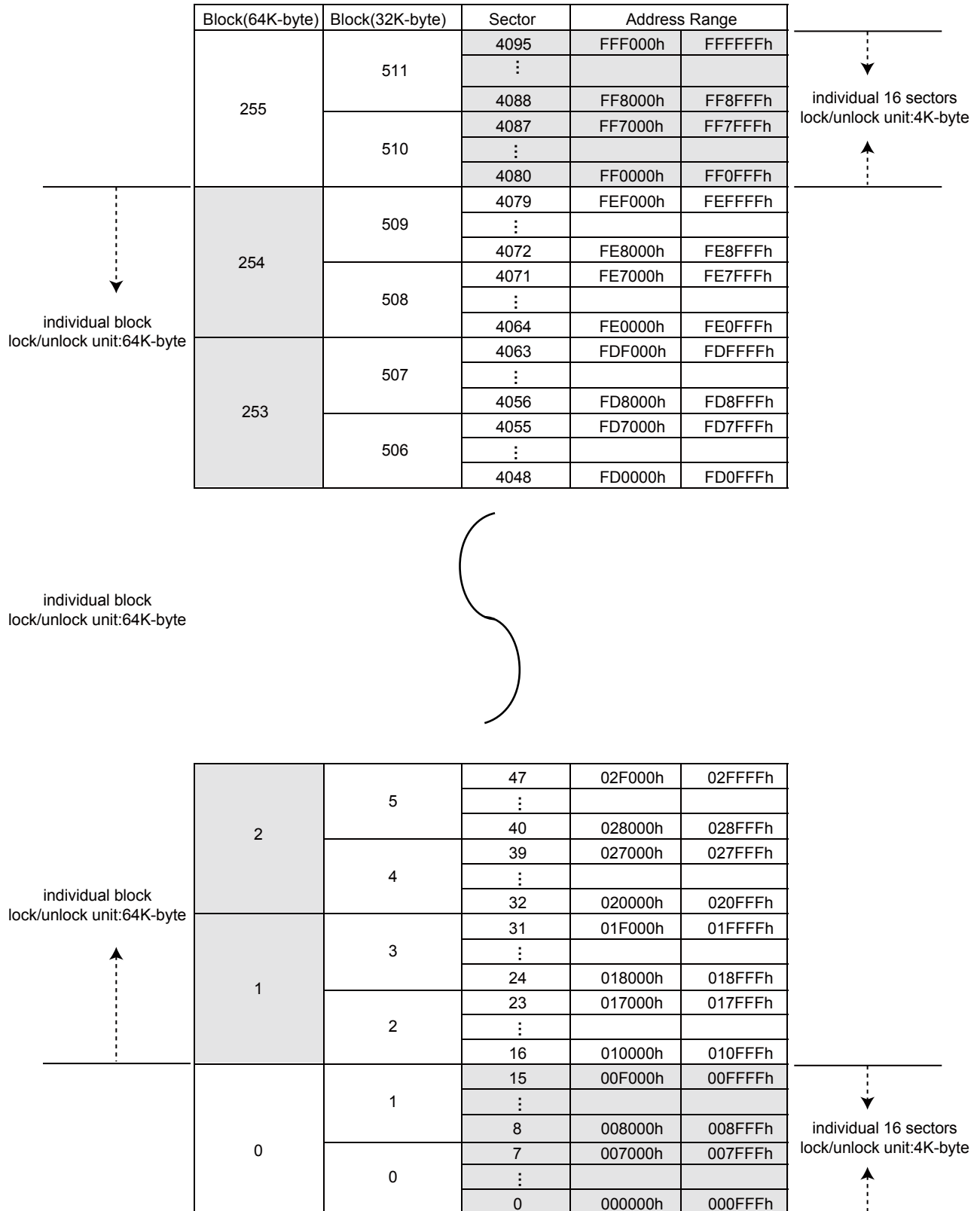
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7. Memory Organization

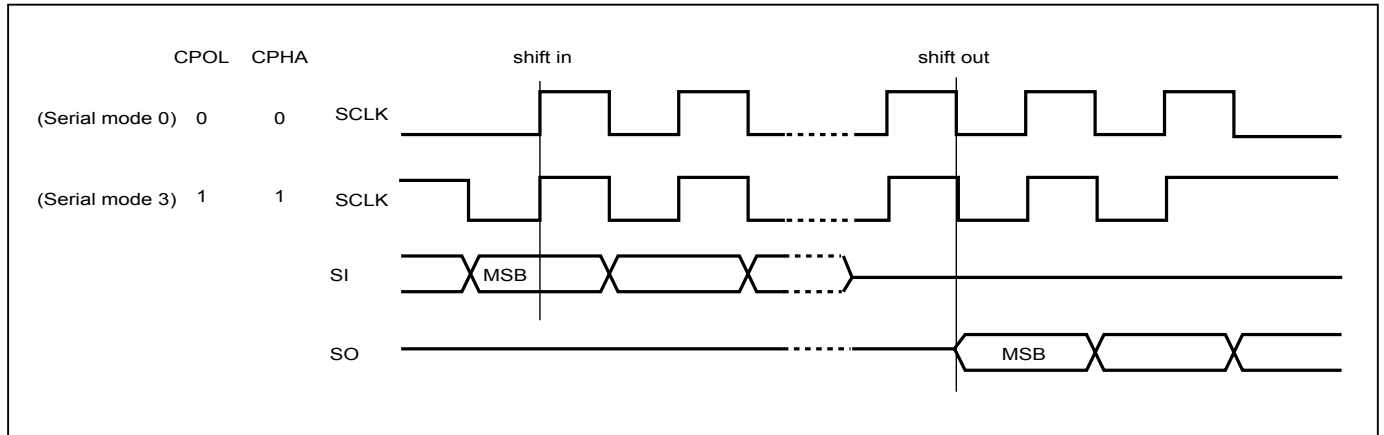
Table 4. Memory Organization



8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Serial Modes Supported".
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, 4READ, W4READ, RDS-FDP, RES, REMS, QPIID, RDBLOCK, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

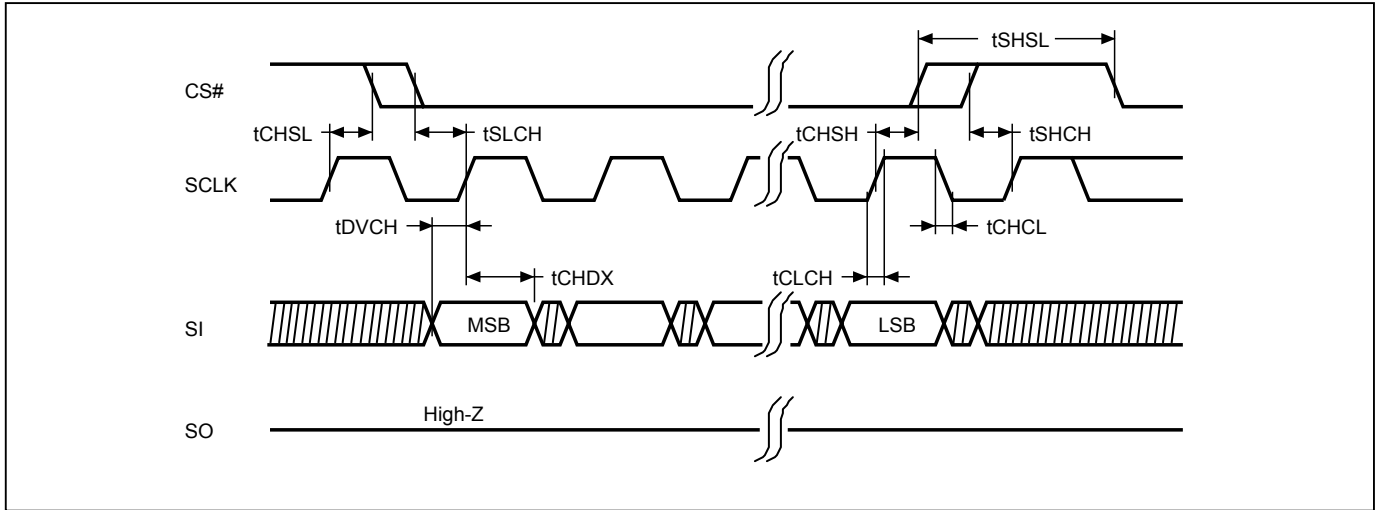
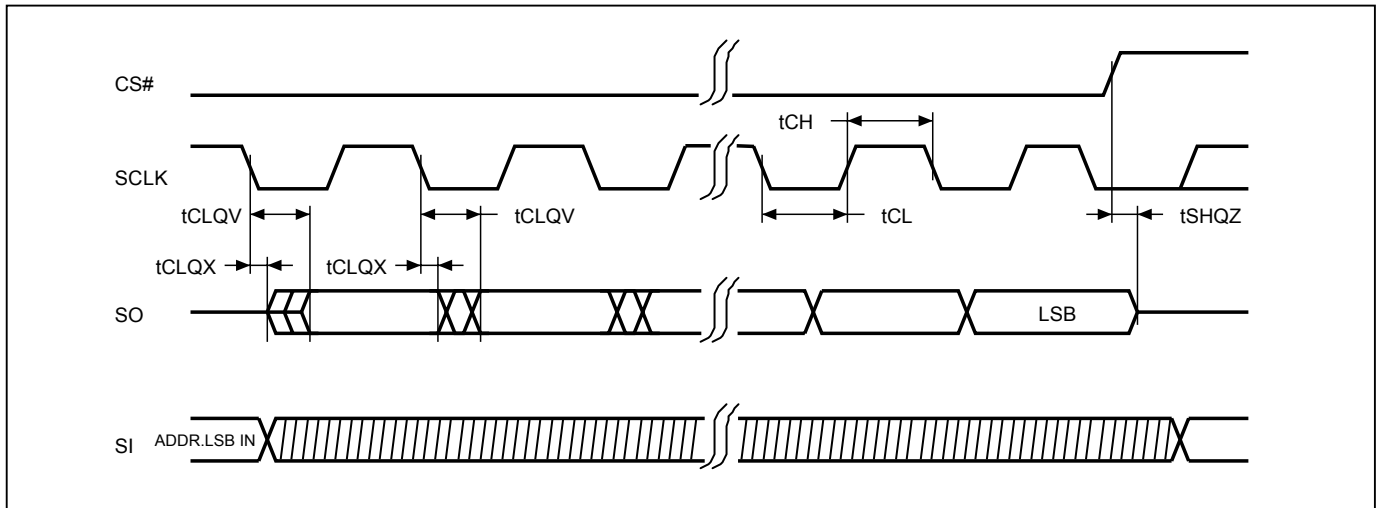


Figure 3. Output Timing



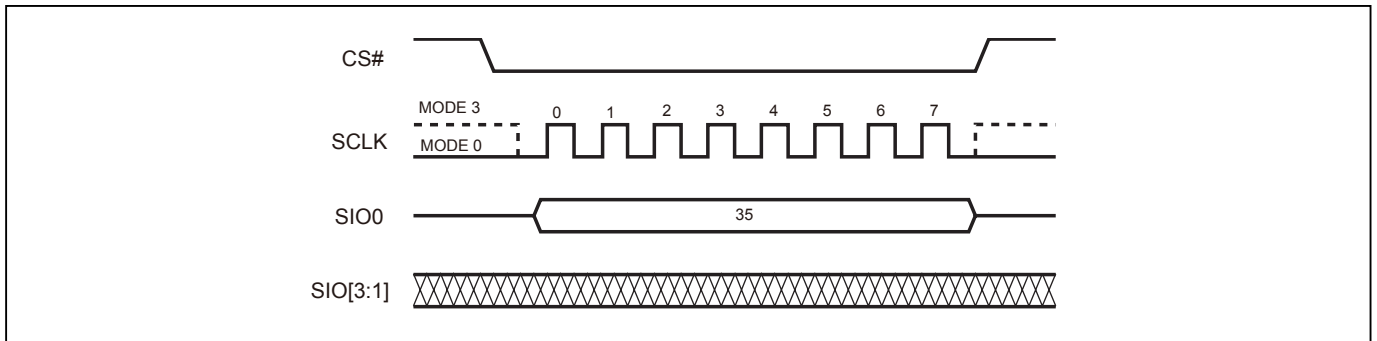
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enable.

Figure 4. Enable QPI Sequence (Command 35H)



Reset QPI (RSTQIO)

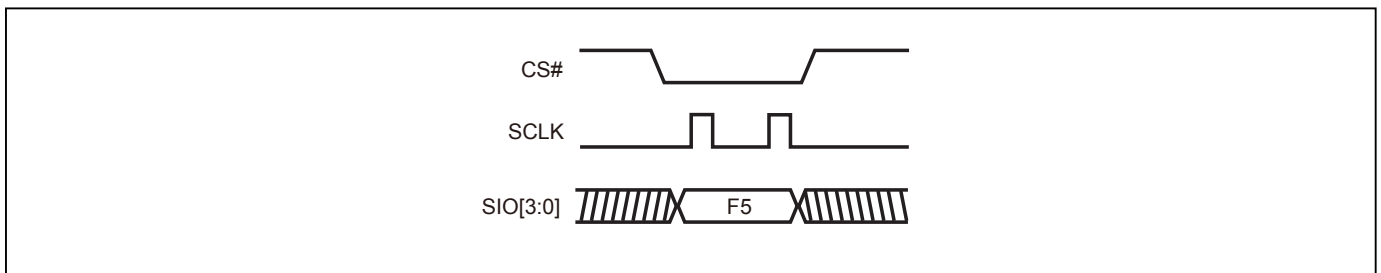
The Reset QPI instruction, F5H, resets the device to SPI protocol operation. To execute a Reset QPI operation, the host drives CS# low, sends the Reset QPI command cycle (F5h) then, drives CS# high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Note:

For EQIO/RSTQIO/SBL CS# high width has to follow "write spec" tSHSL as 30ns for next instruction.

Figure 5. Reset QPI Mode (Command F5H)



9. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

Mode	SPI	SPI/QPI	SPI	SPI/QPI	SPI
Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command) Note1	4READ (4 x I/O read)	W4READ
1st byte	03 (hex)	0B (hex)	BB (hex)	EB (hex)	E7 (hex)
2nd byte	ADD1(8)	ADD1(8)	ADD1(4)	ADD1(2)	ADD1
3rd byte	ADD2(8)	ADD2(8)	ADD2(4)	ADD2(2)	ADD2
4th byte	ADD3(8)	ADD3(8)	ADD3(4)	ADD3(2)	ADD3
5th byte		Dummy(8)/(4)*	Dummy(4)	Dummy(6)	Dummy(4)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	Quad I/O read with 6 dummy cycles	Quad I/O read for with 4 dummy cycles

Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	
5th byte						
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

* The fast read command (0Bh) when under QPI mode, the dummy cycle is 4 clocks.

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/configuration register)	WPSEL (Write Protect Selection)	EQIO (Enable QPI)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	68 (hex)	35 (hex)
2nd byte					Values		
3rd byte					Values		
4th byte							
5th byte							
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/configuration register	to enter and enable individual block protect mode	Entering the QPI mode

Command (byte)	RSTQIO (Reset QPI)	PGM/ERS Suspend (Suspends Program/Erase)	PGM/ERS Resume (Resumes Program/Erase)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)
Mode	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	F5 (hex)	B0 (hex)	30 (hex)	B9 (hex)	AB (hex)	C0 (hex)
2nd byte						Value
3rd byte						
4th byte						
5th byte						
Action	Exiting the QPI mode			enters deep power down mode	release from deep power down mode	to set Burst length

ID/Security Commands

Command (byte)	RDID (read identification)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1(8)		
3rd byte		x	x		ADD2(8)		
4th byte		x	ADD (Note 2)		ADD3(8)		
5th byte					Dummy(8)		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	ID in QPI interface	n bytes read out until CS# goes high	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode

COMMAND (byte)	RDSCUR (read security register)	WRSCUR (write security register)	SBLK (single block lock)	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	2B (hex)	2F (hex)	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)
2nd byte			ADD1	ADD1	ADD1		
3rd byte			ADD2	ADD2	ADD2		
4th byte			ADD3	ADD3	ADD3		
5th byte							
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect

Reset Commands

COMMAND (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)	Release Read Enhanced
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)	99 (hex)	FF (hex)
2nd byte				
3rd byte				
4th byte				
5th byte				
Action			(Note 4)	All these commands FFh, 00h, AAh or 55h will escape the performance mode

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1 which is different from 1 x I/O condition.

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 4: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

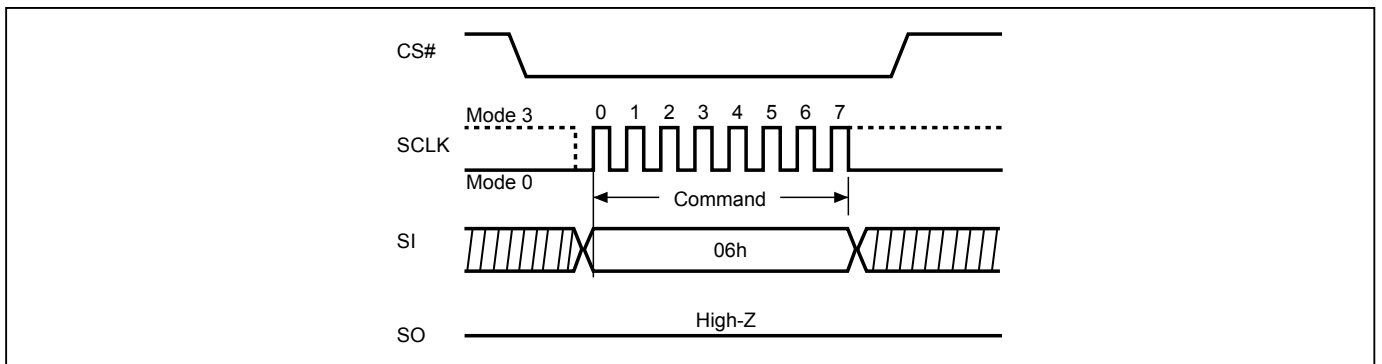
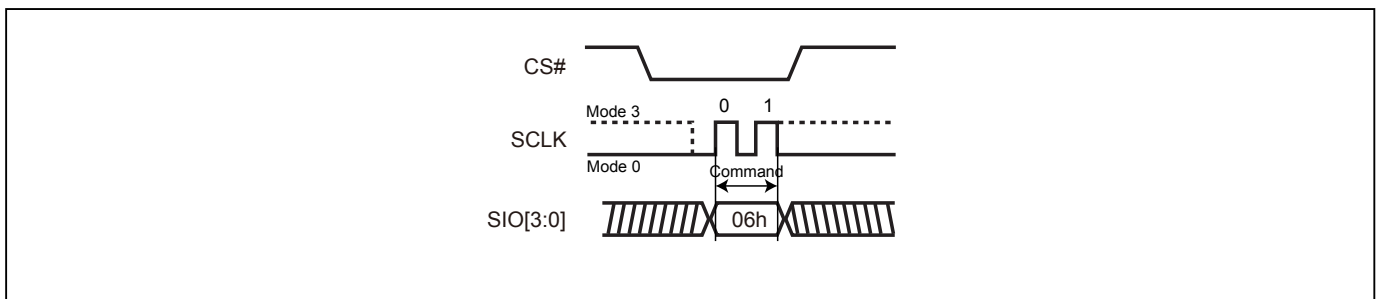
Note 5: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Figure 6. Write Enable (WREN) Sequence (SPI Mode)**Figure 7. Write Enable (WREN) Sequence (QPI Mode)**

9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Pgm/Ers Suspend

Figure 8. Write Disable (WRDI) Sequence (SPI Mode)

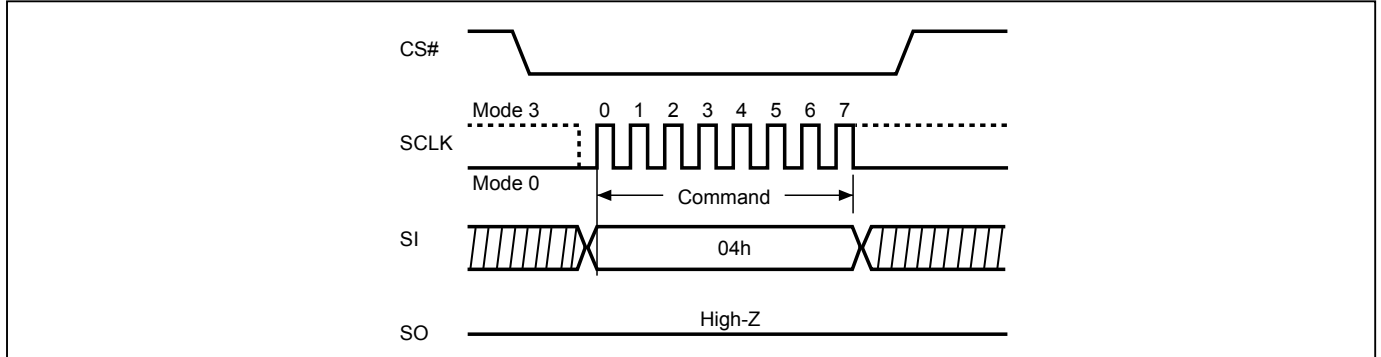
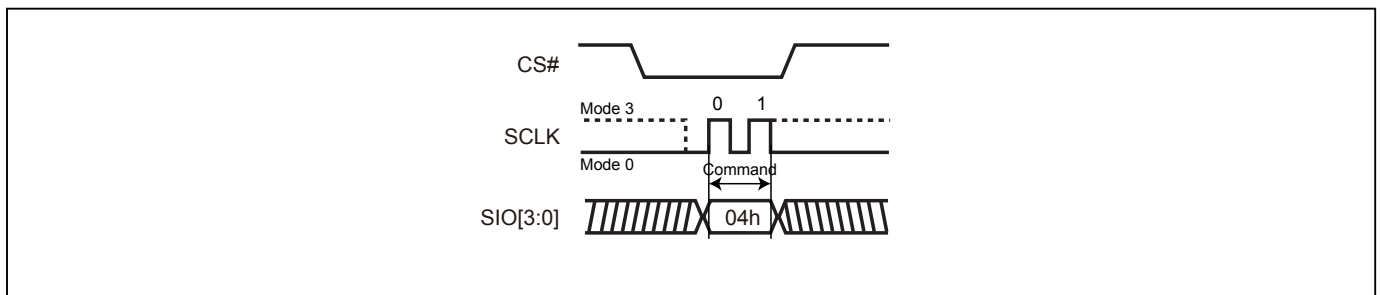


Figure 9. Write Disable (WRDI) Sequence (QPI Mode)



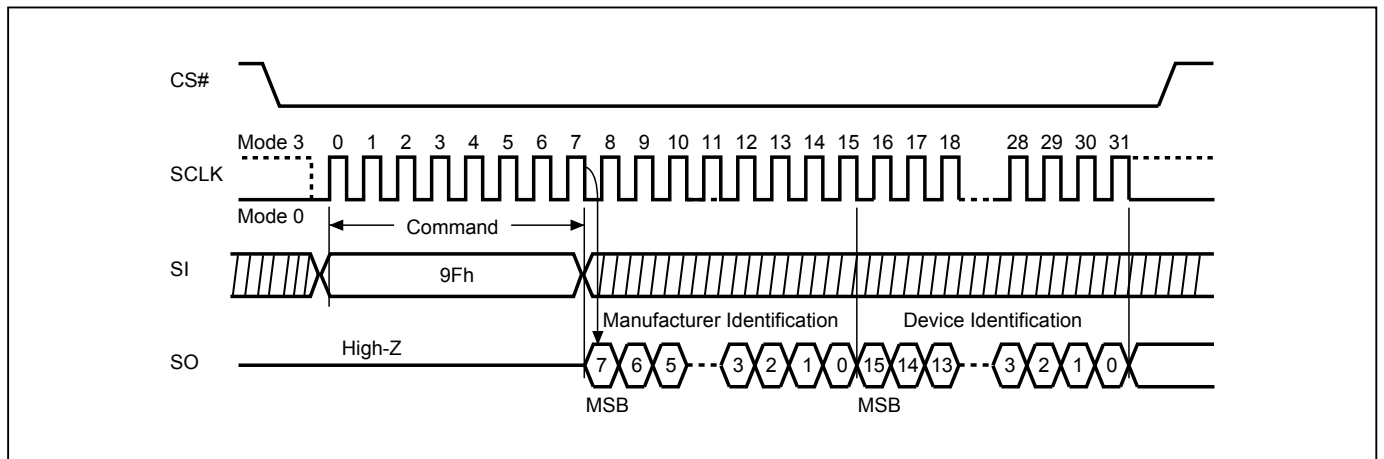
9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macro-nix Manufacturer ID and Device ID are listed as [Table 6 ID Definitions](#).

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 10. Read Identification (RDID) Sequence (SPI mode only)



9-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, the transition to the Stand-by Power mode is delayed by t_{RES2} , and Chip Select (CS#) must remain High for at least $t_{RES2(max)}$, as specified in [Table 16](#). AC Characteristics. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as [Table 6](#) ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of t_{RES2} to transit to standby mode, and CS# must remain to high at least $t_{RES2(max)}$. Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 11. Read Electronic Signature (RES) Sequence (SPI Mode)

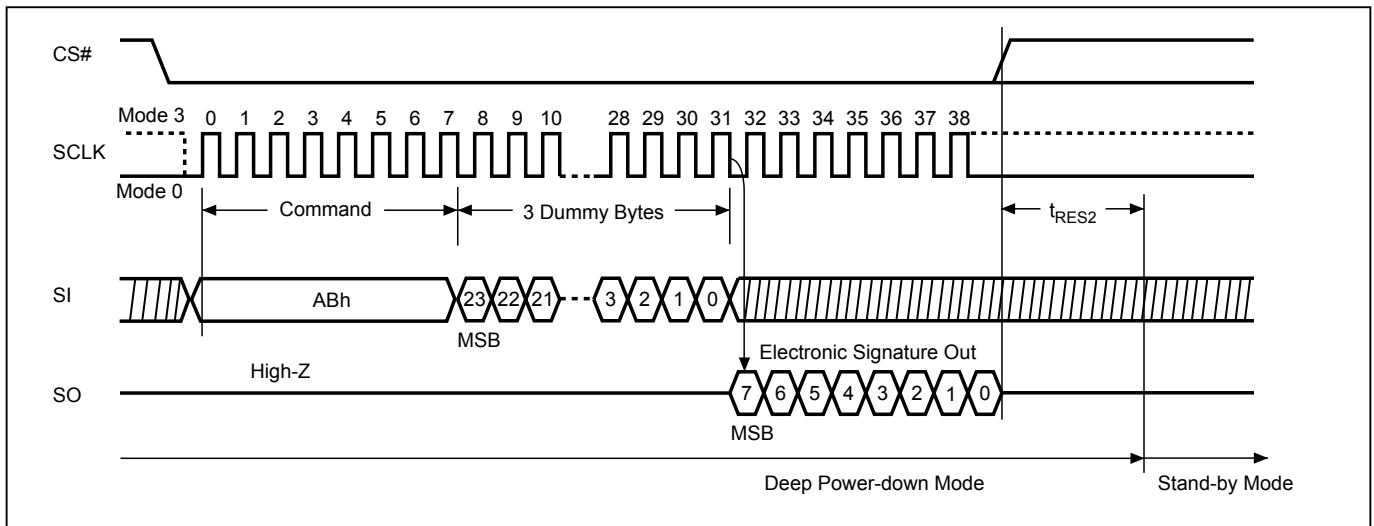


Figure 12. Read Electronic Signature (RES) Sequence (QPI Mode)

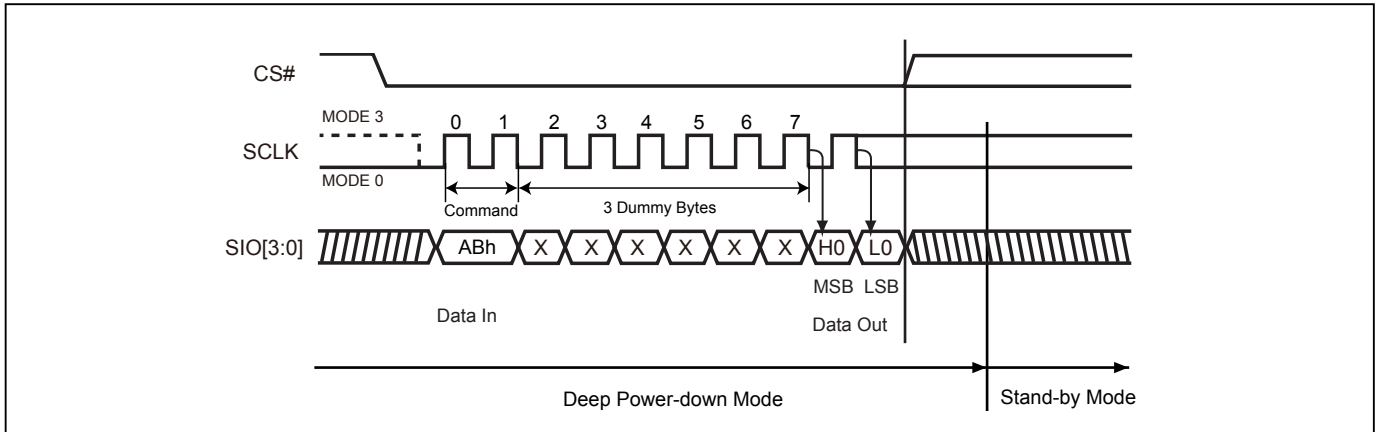


Figure 13. Release from Deep Power-down (RDP) Sequence (SPI Mode)

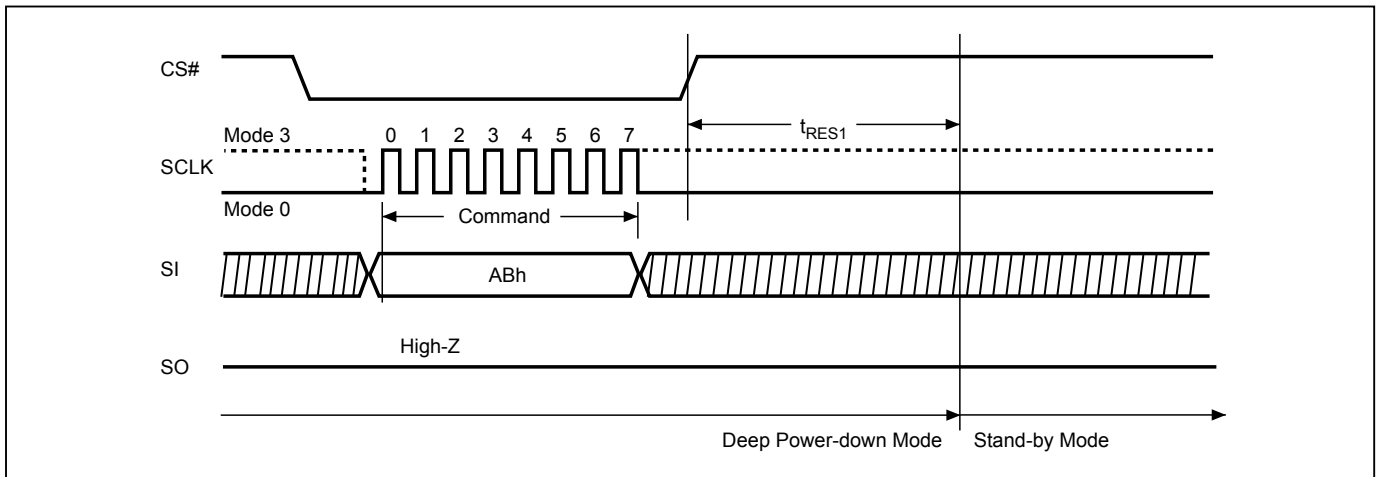
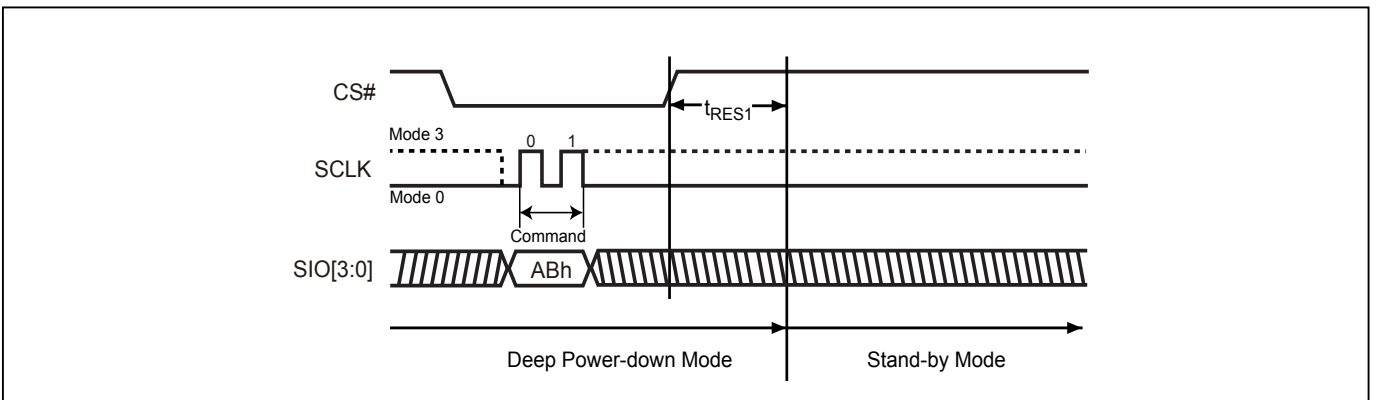


Figure 14. Release from Deep Power-down (RDP) Sequence (QPI Mode)

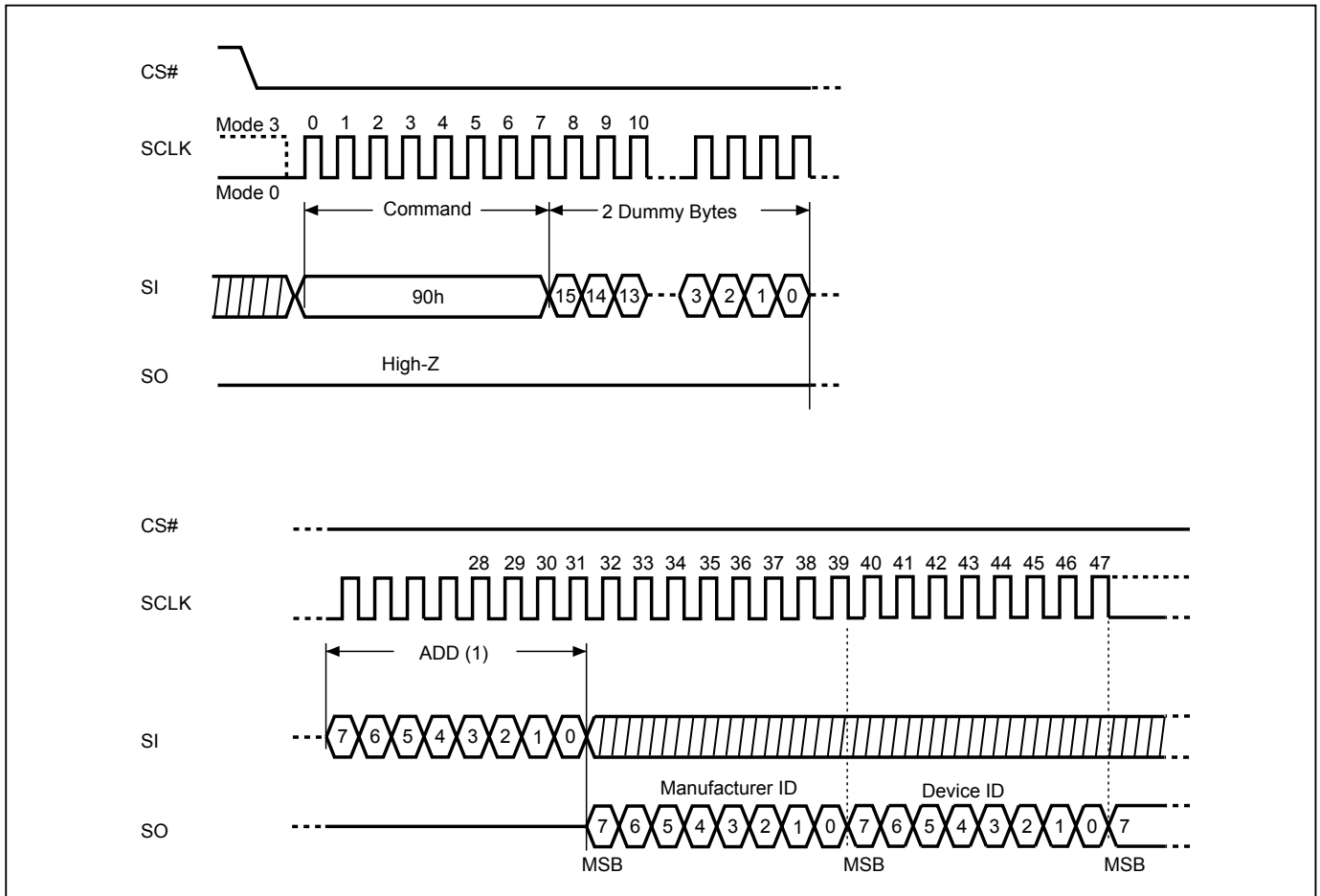


9-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID values are listed in [Table 6](#) of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 15. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)



Notes:

- (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.
- (2) Instruction is either 90(hex).