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MX25U2033E DATASHEET

Contents

1. FEATURES

GENERAL

- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 2,097,152 x 1 bits structure or 1,048,576 x 2 bits (Two I/O read mode) structure or 524,288 x 4 bits (Four I/O read mode) structure
- 64 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 8 Equal Blocks with 32K byte each
  - Any Block can be erased individually
- 4 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast read
    - 1 I/O: 80MHz with 8 dummy cycles
    - 2 I/O: 80MHz with 4 dummy cycles, equivalent to 160MHz
    - 4 I/O: 70MHz with 6 dummy cycles, equivalent to 280MHz;
  - Fast program time: 1.2ms (typ.) and 3ms (max.)/page (256-byte per page)
  - Byte program time: 10us (typ.)
  - Fast erase time
    - 30ms(typ.) and 200ms(max.)/sector (4K-byte per sector)
    - 200ms(typ.) and 1000ms(max.)/block (32K-byte per block)
    - 500ms(typ.) and 2000ms(max.)/block (64K-byte per block)
    - 1.25.s(typ.) and 2.5s(max.)/chip
- Low Power Consumption
  - Low active read current: 12mA(max.) at 80MHz, 7mA(max.) at 33MHz
  - Low active erase/programming current: 25mA (max.)
  - Low standby current: 8uA (typ.)/30uA (max.)
- Low Deep Power Down current: 8uA(max.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

  The BP0-BP2 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 4K-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first).

- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS, REMS2 and REMS4 commands for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- HOLD#/SIO3
  - HOLD feature, to pause the device without deselecting the device or serial data Input/Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-land USON (4x4mm)
  - 8-land WSON (6x5mm)
  - 8-WLCSP
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

The MX25U2033E is 2,097,152 bit serial Flash memory, which is configured as 1,048,576 x 2 internally. The MX25U2033E features a serial peripheral interface and software protocol allowing operation on a simple 4-wire bus while it is in single I/O mode. The four bus signals are a clock input (SCLK), a serial data input (SI), a serial data output (SO) and a chip select (CS#). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U2033E MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip

basis.
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via the WIP bit.
Advanced security features enhance the protection and security functions, please see security features section for more details.
When the device is not in operation and CS# is high, it is put in standby mode and typically draws 25uA DC current.

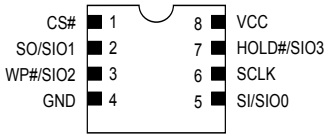
The MX25U2033E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

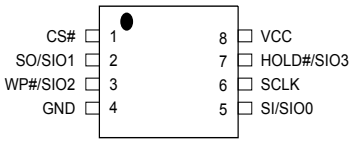
Part Name \ Additional Features	Protection and Security			Read Performance		Identifier		
	Flexible Block Protection (BP0-BP2)	Individual Protect	4K-bit secured OTP	2 I/O Read	4 I/O Read	RES (Command: AB hex)	REMS/ REMS2/ REMS4 (Command: 90/EF/DF hex)	RDID (Command: 9F hex)
MX25U2033E	V	V	V	V	V	32 (hex)	C2 32 (hex) (if ADD=0)	C2 25 32 (hex)

3. PIN CONFIGURATIONS

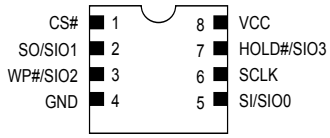
8-LAND USON (4x4mm)



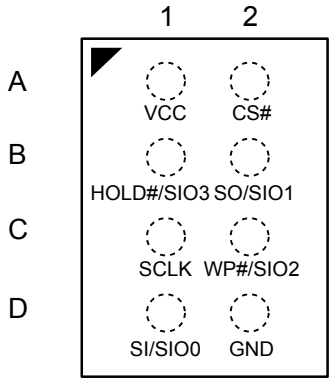
8-PIN SOP (150mil)



8-LAND WSON (6x5mm)



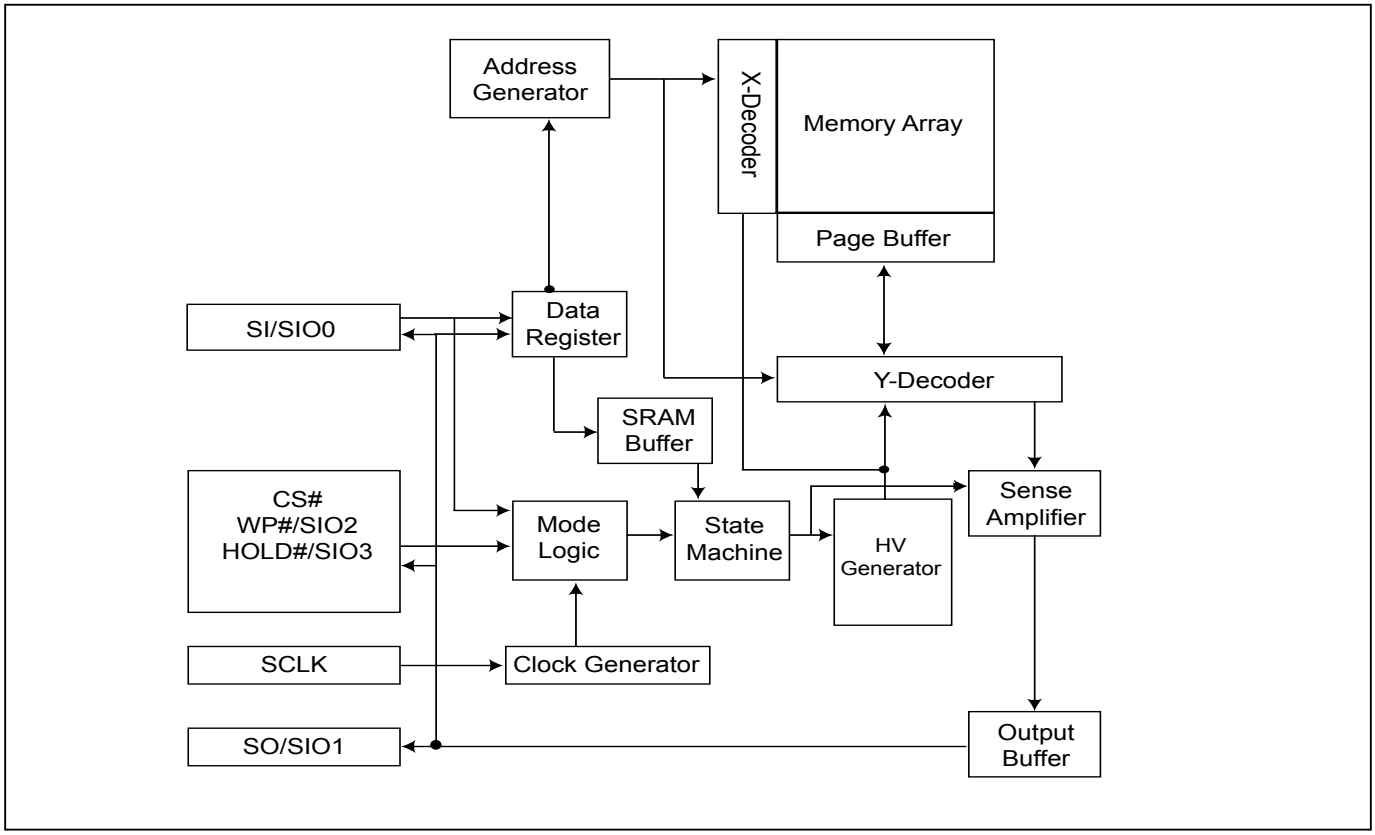
8-BALL BGA (WLCSP) TOP View



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4x I/O read mode)
HOLD#/SIO3	To pause the device without deselecting the device or Serial Data Input & Output (for 4x I/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC powerup and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data. The WEL bit will return to resetting stage while the following conditions occurred:
  - Power-up
  - Completion of Write Disable (WRDI) command
  - Completion of Write Status Register (WRSR) command
  - Completion of Page Program (PP) command
  - Completion of Quad page program (4PP) command
  - Completion of Sector Erase (SE) command
  - Completion of Block Erase 32KB (BE32K) command
  - Completion of Block Erase (BE) command
  - Completion of Chip Erase (CE) command
  - Completion of Write Protection Select (WPSEL) command
  - Completion of Write Security Register (WRSCUR) command
  - Completion of Single Block Lock/Unlock (SBLK/SBULK) command
  - Completion of Gang Block Lock/Unlock (GBLK/GBULK) command

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP2 bits.
Please refer to table of *"Table 2. Protected Area Sizes"*.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O read mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status Bit			Protect Level
BP2	BP1	BP0	
0	0	0	0 (none, not protected)
0	0	1	1 (1 block, protected block 3)
0	1	0	2 (2 blocks, protected blocks 2~3)
0	1	1	3 (4 blocks, protected all blocks)
1	0	0	4 (4 blocks, protected all blocks)
1	0	1	5 (2 blocks, protected blocks 0~1)
1	1	0	6 (3 blocks, protected blocks 0~2)
1	1	1	7 (4 blocks, protected all blocks)

II. **Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker. Please refer to *"Table 3. 4K-bit Secured OTP Definition"*.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 9. Security Register Definition"* for security register bit definition and *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

Note:
Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7. MEMORY ORGANIZATION

Table 4. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range		
3	7 | 6	63	03F000h	03FFFFh	▲ Individual Sector Lock/Unlock ▼
		:	:	:	
		48	030000h	030FFFh	
2	5 | 4	47	02F000h	02FFFFh	▲ Individual Block Lock/Unlock ▼
		:	:	:	
		32	020000h	020FFFh	
1	3 | 2	31	01F000h	01FFFFh	
		:	:	:	
		16	010000h	010FFFh	
0	1 | 0	15	00F000h	00FFFFh	▲ Individual Sector Lock/Unlock ▼
		:	:	:	
		2	002000h	002FFFh	
		1	001000h	001FFFh	
		0	000000h	000FFFh	

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

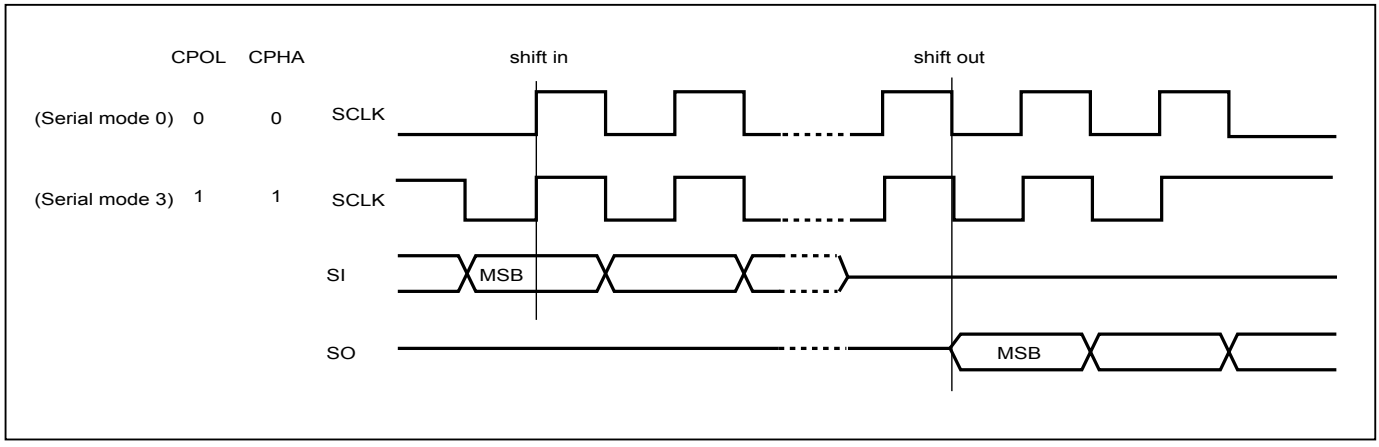
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"* .

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, 4READ, RES, REMS, REMS2, and REMS4, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK,ENSO, EXSO, and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of WRSCUR, WPSEL Write Status Register, Program and Erase.

Figure 1. Serial Modes Supported



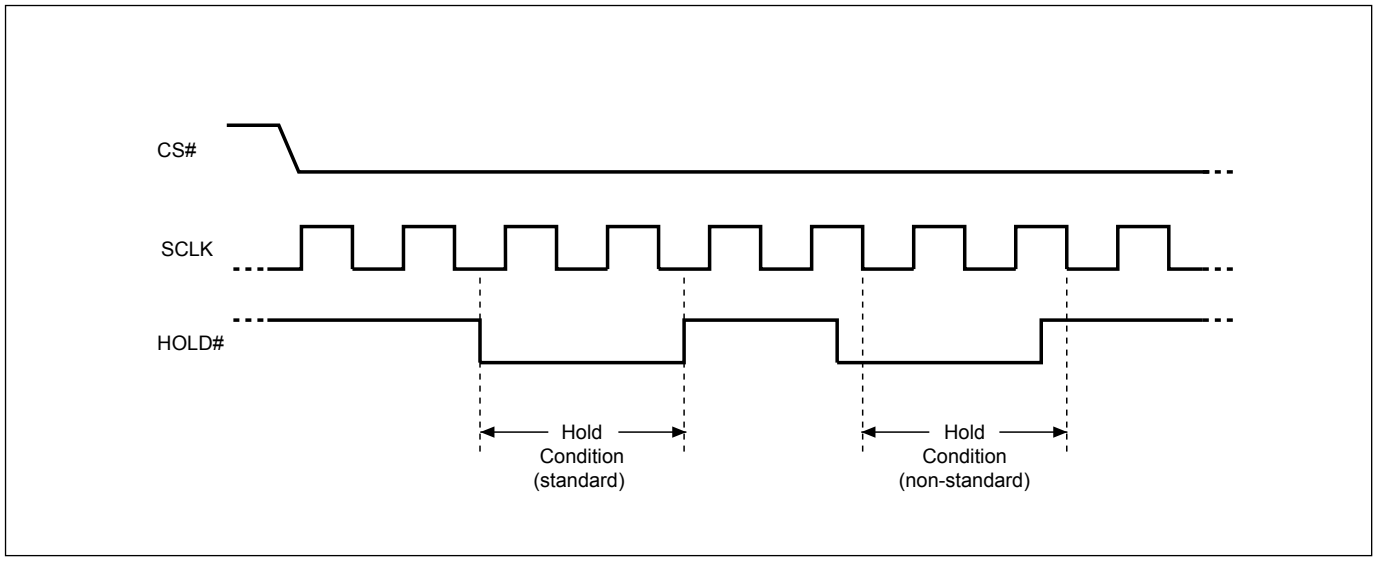
Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see *"Figure 2. Hold Condition Operation"*.

Figure 2. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

10. COMMAND DESCRIPTION

Table 5. Command Set

Read Commands

I/O	1	1	1	2	4
Command (byte)	READ (normal read)	FAST READ (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command)	4READ (4 x I/O read command)
Clock rate (MHz)	50	80	80	80	70
1st byte	03 (hex)	0B (hex)	5A (hex)	BB (hex)	EB (hex)
2nd byte	AD1	AD1	AD1	AD1	AD1
3rd byte	AD2	AD2	AD2	AD2	AD2
4th byte	AD3	AD3	AD3	AD3	AD3
5th byte		Dummy	Dummy	Dummy	Dummy
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by 4 x I/O until CS# goes high

Program/Erase Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	WRSR (write status register)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)
1st byte	06 (hex)	04 (hex)	05 (hex)	01 (hex)	20 (hex)	52 (hex)	D8 (hex)
2nd byte				Values	AD1	AD1	AD1
3rd byte					AD2	AD2	AD2
4th byte					AD3	AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to write new values of the status register	to erase the selected sector	to erase the selected 32KB block	to erase the selected block

Command (byte)	CE (chip erase)	PP (page program)	4PP (Quad page program)	DP (Deep power down)	RDP (Release from deep power down)
1st byte	60 or C7 (hex)	02 (hex)	38 (hex)	B9 (hex)	AB (hex)
2nd byte		AD1	AD1		
3rd byte		AD2	AD2		
4th byte		AD3	AD3		
Action	to erase whole chip	to program the selected page	quad input to program the selected page	enters deep power down mode	release from deep power down mode

Security/ID/Mode Setting/Reset Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)
1st byte	9F (hex)	AB (hex)	90 (hex)	EF (hex)	DF (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x	X	x		
3rd byte		x	x	X	x		
4th byte		x	ADD	ADD	ADD		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	SBLK (single block lock	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)
1st byte	2B (hex)	2F (hex)	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)
2nd byte			AD1	AD1	AD1		
3rd byte			AD2	AD2	AD2		
4th byte			AD3	AD3	AD3		
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect

Command (byte)	WPSEL (Write Protect Selection)
1st byte	68 (hex)
2nd byte	
3rd byte	
4th byte	
Action	to enter and enable individal block protect mode

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, WPSEL, WRSCUR, SBLK, SBULK, GBLK, GBULK and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high. (Please refer to *"Figure 14. Write Enable (WREN) Sequence (Command 06)"*)

10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high. (Please refer to *"Figure 15. Write Disable (WRDI) Sequence (Command 04)"*)

The WEL bit is reset by following situations:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Completion of Write Protection Select (WPSEL) instruction
- Completion of Write Security Register (WRSCUR) instruction
- Completion of Single Block Lock/Unlock (SBLK/SBULK) instruction
- Completion of Gang Block Lock/Unlock (GBLK/GBULK) instruction

10-3. Read Identification (RDID)

The RDID instruction is to read the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 25(hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as table of "ID Definitions". (Please refer to *"Table 8. ID Definitions"*)

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out. (Please refer to *"Figure 16. Read Identification (RDID) Sequence (Command 9F)"*)

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

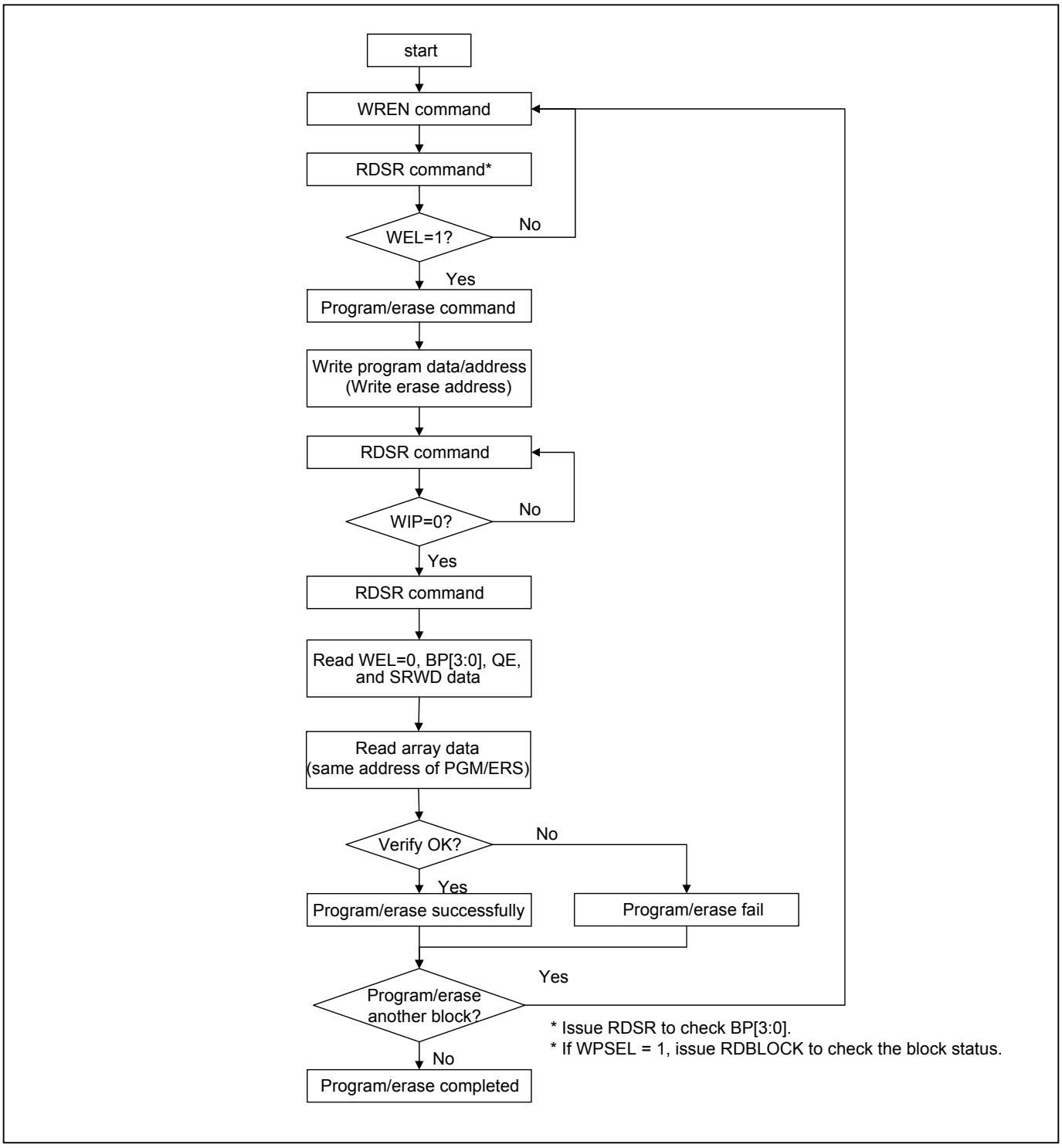
10-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/WPSEL/WRSCUR/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

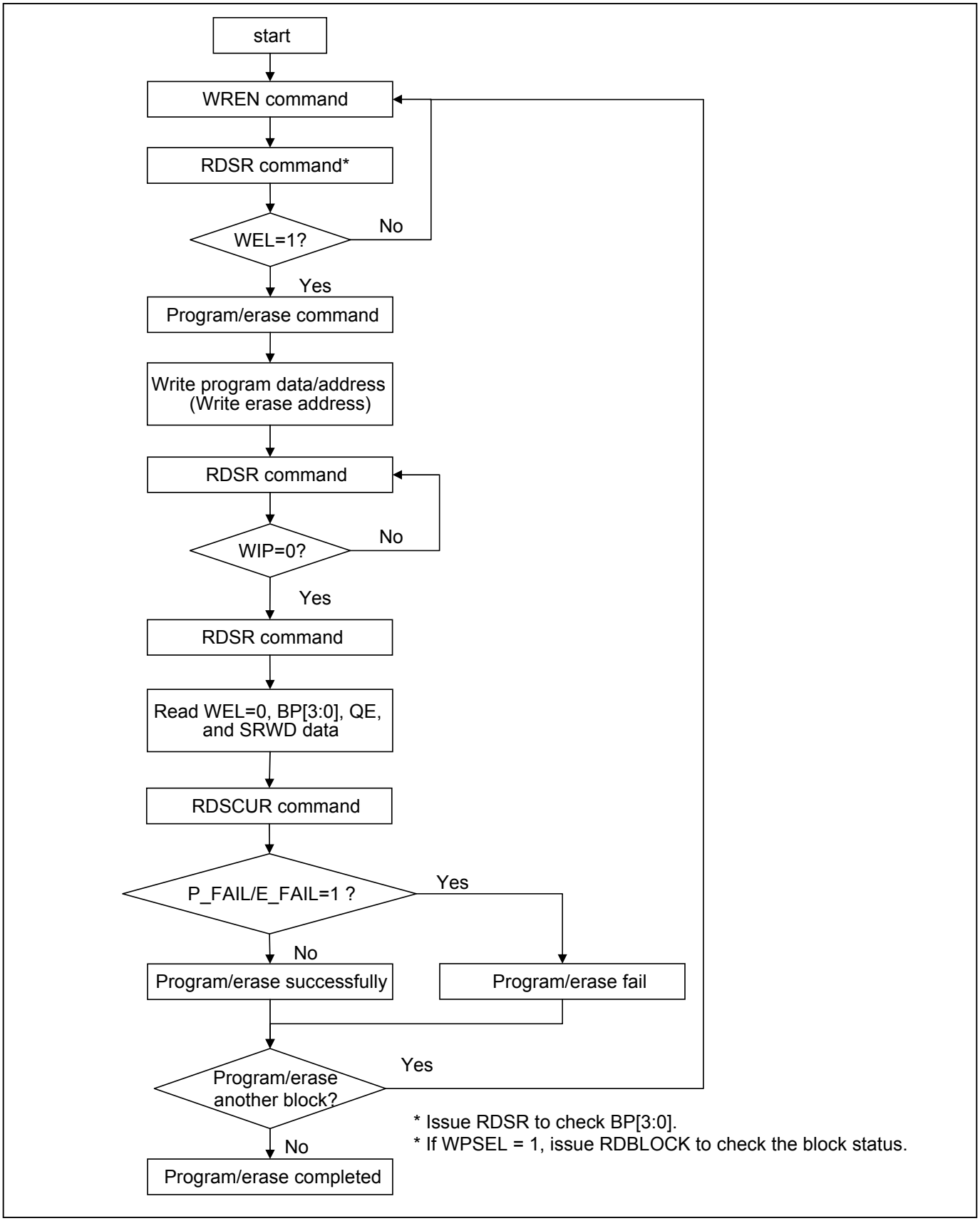
The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO. (Please refer to *"Figure 17. Read Status Register (RDSR) Sequence (Command 05)"*)

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

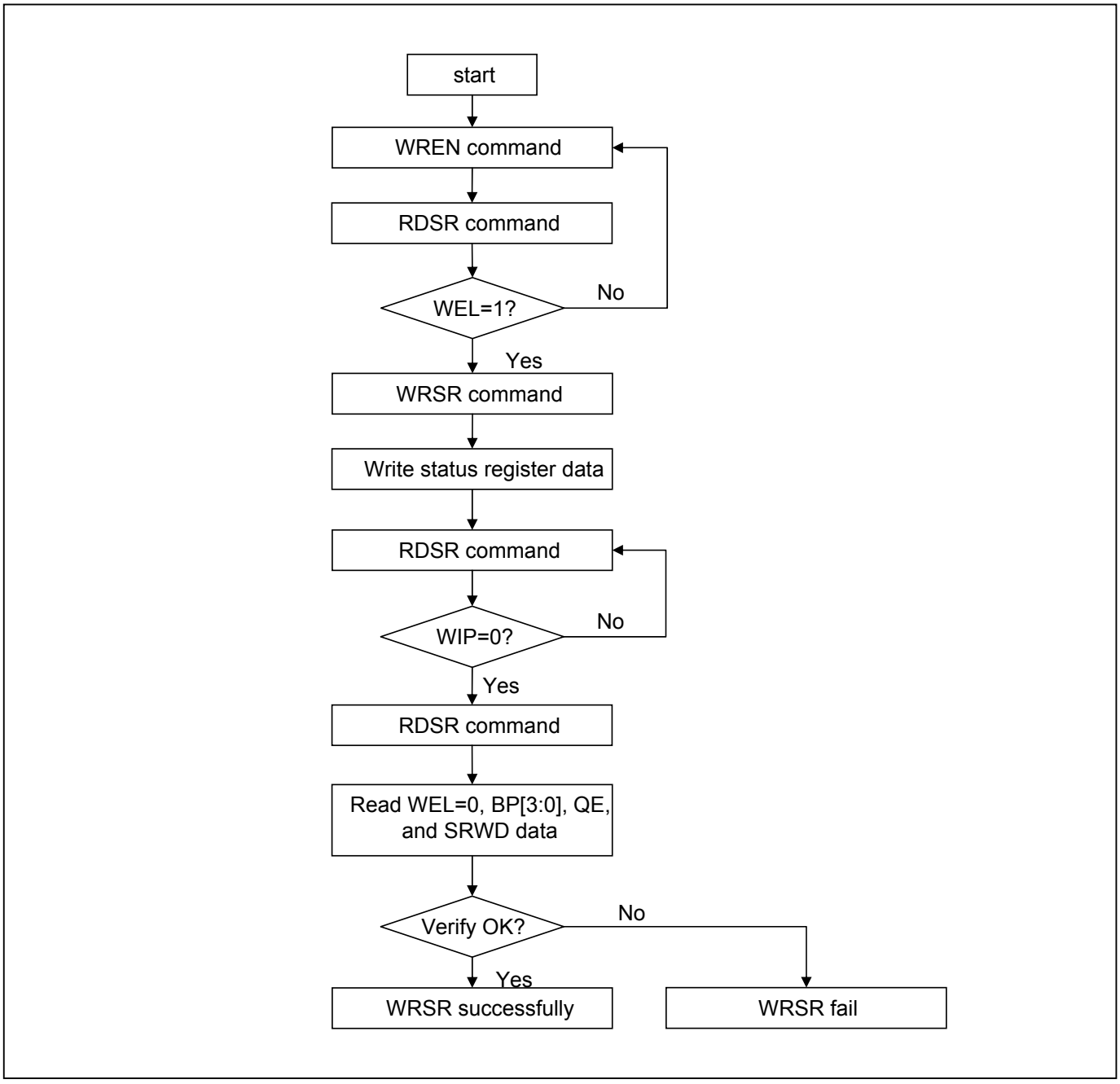
Program/Erase Flow with Read Array Data



Program/ Erase Flow without Read Array Data (read P_FAIL/E_FAIL flag)



WRSR Flow


start
WREN command
RDSR command
WEL=1?
No
Yes
WRSR command
Write status register data
RDSR command
WIP=0?
No
Yes
RDSR command
Read WEL=0, BP[3:0], QE, and SRWD data
Verify OK?
No
Yes
WRSR successfully
WRSR fail

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP2:BP0) set to 0, the CE instruction can be executed). The BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the features of HPM and HOLD will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	0	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	0	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the *"Table 2. Protected Area Sizes"*.

10-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high. (Please refer to *"Figure 18. Write Status Register (WRSR) Sequence (Command 01)"*)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 7. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP2 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP2 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is at software protected mode (SPM)

Note:
If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP2, BP1, BP0.
If the system enter Quad I/O QE=1, the feature of HPM will be disabled.

10-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 19. Read Data Bytes (READ) Sequence (Command 03) (50MHz)"*)

10-7. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 20. Read at Higher Speed (FAST_READ) Sequence (Command 0B)"*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

10-8. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4 dummy cycles on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (Please refer to *"Figure 21. 2 x I/O Read Mode Sequence (Command BB)"*).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

10-9. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 22. 4 x I/O Read Mode Sequence (Command EB)"*)

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

10-10. Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please note *Figure 22. 4 x I/O Read Enhance Performance Mode Sequence (Command EB)"*)

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still CS# goes high → CS# goes low (reduce 4Read instruction) →24-bit random access address (Please refer to *"Figure 23. 4 x I/O Read Enhance Performance Mode Sequence (Command EB)"*).

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

10-11. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high. (Please refer to *"Figure 26. Sector Erase (SE) Sequence (Command 20)")*

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP2 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Sector Erase (SE) instruction will not be executed on the sector.