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MX25U3235E

DATASHEET

Contents

32M-BIT [x 1/x 2/x 4] 1.8V CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 32,554,432 x 1 bit structure or 16,777,216 x 2 bits (two I/O read mode) structure or 8,388,608 x 4 bits (four I/O read mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V

PERFORMANCE

- High Performance
  - Fast read for SPI mode
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
    - 4 I/O: 104MHz with 6 dummy cycles, equivalent to 416MHz
  - Fast read for QPI mode
    - 4 I/O: 84MHz with 4 dummy cycles, equivalent to 336MHz
    - 4 I/O: 104MHz with 6 dummy cycles, equivalent to 416MHz
  - Fast program time: 1.2ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 10us (typical)
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
  - Fast erase time: 45ms (typ.)/sector (4K-byte per sector); 250ms(typ.) /block (32K-byte per block); 500ms(typ.) / block (64K-byte per block); 18s(typ.) /chip
- Low Power Consumption
  - Low active read current: 20mA(max.) at 104MHz, 15mA(max.) at 84MHz
  - Low active erase/programming current: 20mA (typ.)
  - Standby current: 25uA (typ.)
- Deep Power Down: 2uA(typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 4k-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block

- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES
- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- NC/SIO3
  - NC pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (200mil)
  - 8-land WSON (6x5mm)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

The MX25U3235E are 32,554,432 bit serial Flash memory, which is configured as 4,194,304 x 8 internally. When it is in two or four I/O read mode, the structure becomes 16,777,216 bits x 2 or 8,388,608 bits x 4. MX25U3235E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin and WP# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U3235E MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode and typically draws 30uA DC current.

The MX25U3235E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

Part Name \ Additional Features	Protection and Security		Read Performance					
			SPI				QPI	
	Flexible Block Protection (BP0-BP3)	4K-bit security OTP	1 I/O (104 MHz)	2 I/O (84 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)
MX25U3235E	V	V	V	V	V	V	V	V

Part Name \ Additional Features	Identifier			
	RES (command: AB hex)	REMS (command: 90 hex)	RDID (command: 9F hex)	QPIID (Command: AF hex)
MX25U3235E	36 (hex)	C2 36 (hex) (if ADD=0)	C2 25 36	C2 25 36

3. PIN CONFIGURATIONS

8-LAND WSON (6x5mm)

```
        CS#  ■ 1      8 ■  VCC
     SO/SIO1 ■ 2      7 ■  NC/SIO3
    WP#/SIO2 ■ 3      6 ■  SCLK
         GND ■ 4      5 ■  SI/SIO0
```

8-PIN SOP (200mil)

```
        CS#  □ 1      8 □  VCC
     SO/SIO1 □ 2      7 □  NC/SIO3
    WP#/SIO2 □ 3      6 □  SCLK
         GND □ 4      5 □  SI/SIO0
```
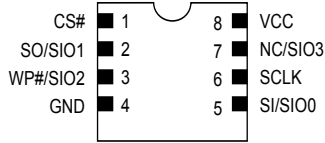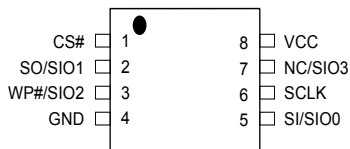
4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC pin (Not connected) or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground

5. BLOCK DIAGRAM
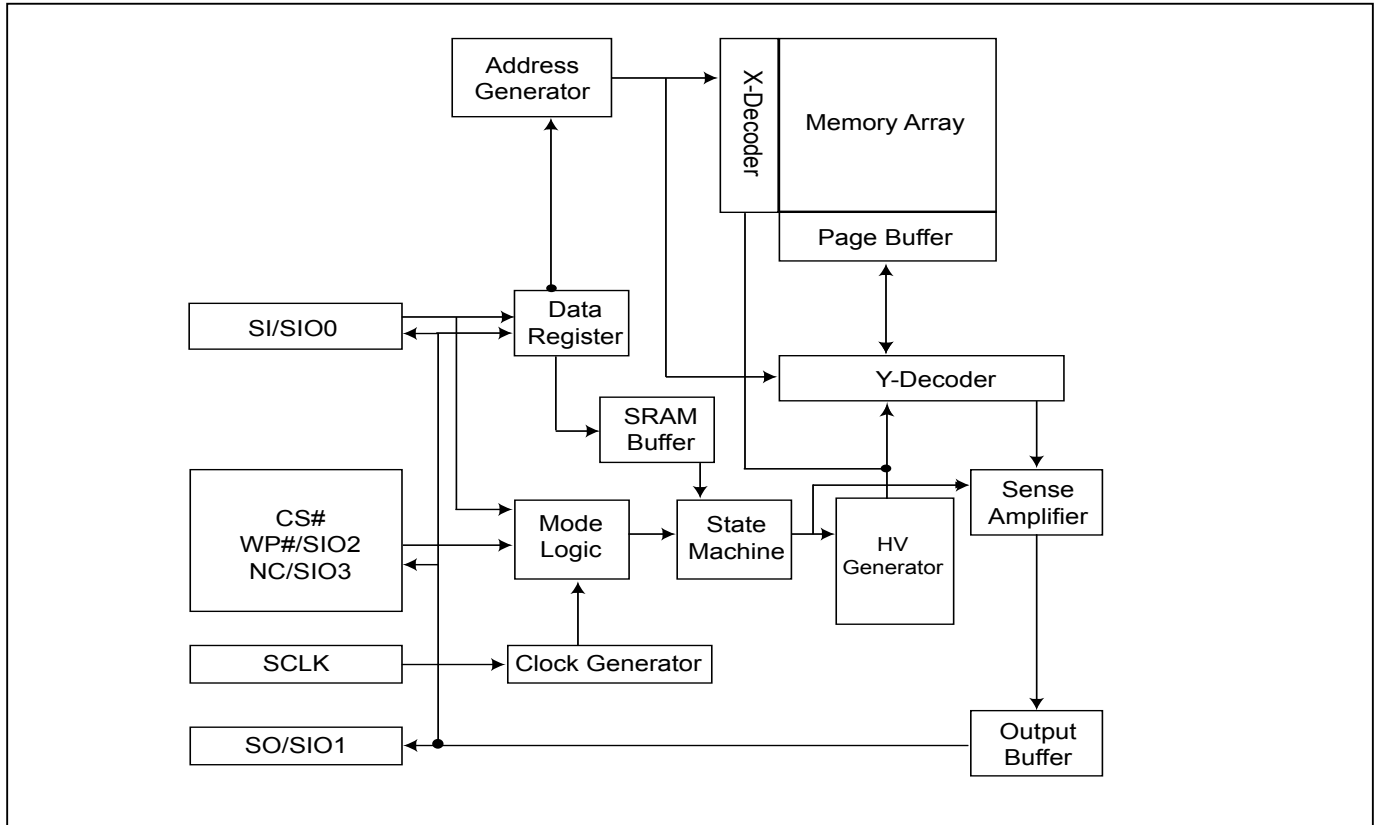
6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issung other commands to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Quad I/O Page Program (4PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase 32KB (BE32K) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
  - Program/Erase Suspend
  - Softreset command completion
  - Write Security Register (WRSCUR) command completion
  - Write Protection Selection (WPSEL) command completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.

- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection
- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Proteced Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, protected block 63rd)
0	0	1	0	2 (2blocks, protected block 62nd~63rd)
0	0	1	1	3 (4blocks, protected block 60th~63rd)
0	1	0	0	4 (8blocks, protected block 56th-63rd)
0	1	0	1	5 (16blocks, protected block 48th~63rd)
0	1	1	0	6 (32blocks, protected block 32nd~63rd)
0	1	1	1	7 (64blocks, protected all)
1	0	0	0	8 (64blocks, protected all)
1	0	0	1	9 (32blocks, protected block 0th~31st)
1	0	1	0	10 (48blocks, protected block 0th~47th)
1	0	1	1	11 (56blocks, protected block 0th~55th)
1	1	0	0	12 (60blocks, protected block 0th~59th)
1	1	0	1	13 (62blocks, protected block 0th~61st)
1	1	1	0	14 (63blocks, protected block 0th~62nd)
1	1	1	1	15 (64blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to *"Table 3. 4K-bit Secured OTP Definition"*.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP (ENSO) command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP (EXSO) command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 10. Security Register Definition"* for security register bit definition and *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7. Memory Organization

Table 4. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
63	127	1023	3FF000h	3FFFFFh
	|	:	:	:
	126	1008	3F0000h	3F0FFFh
62	125	1007	3EF000h	3EFFFFh
	|	:	:	:
	124	992	3E0000h	3E0FFFh
61	123	991	3DF000h	3DFFFFh
	|	:	:	:
	122	976	3D0000h	3D0FFFh
60	121	975	3CF000h	3CFFFFh
	|	:	:	:
	120	960	3C0000h	3C0FFFh
59	119	959	3BF000h	3BFFFFh
	|	:	:	:
	118	944	3B0000h	3B0FFFh
58	117	943	3AF000h	3AFFFFh
	|	:	:	:
	116	928	3A0000h	3A0FFFh
57	115	927	39F000h	39FFFFh
	|	:	:	:
	114	912	390000h	390FFFh
56	113	911	38F000h	38FFFFh
	|	:	:	:
	112	896	380000h	380FFFh
55	111	895	37F000h	37FFFFh
	|	:	:	:
	110	880	370000h	370FFFh
54	109	879	36F000h	36FFFFh
	|	:	:	:
	108	864	360000h	360FFFh
53	107	863	35F000h	35FFFFh
	|	:	:	:
	106	848	350000h	350FFFh
52	105	847	34F000h	34FFFFh
	|	:	:	:
	104	832	340000h	340FFFh
51	103	831	33F000h	33FFFFh
	|	:	:	:
	102	816	330000h	330FFFh
50	101	815	32F000h	32FFFFh
	|	:	:	:
	100	800	320000h	320FFFh
49	99	799	31F000h	31FFFFh
	|	:	:	:
	98	784	310000h	310FFFh
48	97	783	30F000h	30FFFFh
	|	:	:	:
	96	768	300000h	300FFFh

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
47	95	767	2FF000h	2FFFFFh
	|	:	:	:
	94	752	2F0000h	2F0FFFh
46	93	751	2EF000h	2EFFFFh
	|	:	:	:
	92	736	2E0000h	2E0FFFh
45	91	735	2DF000h	2DFFFFh
	|	:	:	:
	90	720	2D0000h	2D0FFFh
44	89	719	2CF000h	2CFFFFh
	|	:	:	:
	88	704	2C0000h	2C0FFFh
43	87	703	2BF000h	2BFFFFh
	|	:	:	:
	86	688	2B0000h	2B0FFFh
42	85	687	2AF000h	2AFFFFh
	|	:	:	:
	84	672	2A0000h	2A0FFFh
41	83	671	29F000h	29FFFFh
	|	:	:	:
	82	656	290000h	290FFFh
40	81	655	28F000h	28FFFFh
	|	:	:	:
	80	640	280000h	280FFFh
39	79	639	27F000h	27FFFFh
	|	:	:	:
	78	624	270000h	270FFFh
38	77	623	26F000h	26FFFFh
	|	:	:	:
	76	608	260000h	260FFFh
37	75	607	25F000h	25FFFFh
	|	:	:	:
	74	592	250000h	250FFFh
36	73	591	24F000h	24FFFFh
	|	:	:	:
	72	576	240000h	240FFFh
35	71	575	23F000h	23FFFFh
	|	:	:	:
	70	560	230000h	230FFFh
34	69	559	22F000h	22FFFFh
	|	:	:	:
	68	544	220000h	220FFFh
33	67	543	21F000h	21FFFFh
	|	:	:	:
	66	528	210000h	210FFFh
32	65	527	20F000h	20FFFFh
	|	:	:	:
	64	512	200000h	200FFFh

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
31	63	511	1FF000h	1FFFFFh
	|	:	:	:
	62	496	1F0000h	1F0FFFh
30	61	495	1EF000h	1EFFFFh
	|	:	:	:
	60	480	1E0000h	1E0FFFh
29	59	479	1DF000h	1DFFFFh
	|	:	:	:
	58	464	1D0000h	1D0FFFh
28	57	463	1CF000h	1CFFFFh
	|	:	:	:
	56	448	1C0000h	1C0FFFh
27	55	447	1BF000h	1BFFFFh
	|	:	:	:
	54	432	1B0000h	1B0FFFh
26	53	431	1AF000h	1AFFFFh
	|	:	:	:
	52	416	1A0000h	1A0FFFh
25	51	415	19F000h	19FFFFh
	|	:	:	:
	50	400	190000h	190FFFh
24	49	399	18F000h	18FFFFh
	|	:	:	:
	48	384	180000h	180FFFh
23	47	383	17F000h	17FFFFh
	|	:	:	:
	46	368	170000h	170FFFh
22	45	367	16F000h	16FFFFh
	|	:	:	:
	44	352	160000h	160FFFh
21	43	351	15F000h	15FFFFh
	|	:	:	:
	42	336	150000h	150FFFh
20	41	335	14F000h	14FFFFh
	|	:	:	:
	40	320	140000h	140FFFh
19	39	319	13F000h	13FFFFh
	|	:	:	:
	38	304	130000h	130FFFh
18	37	303	12F000h	12FFFFh
	|	:	:	:
	36	288	120000h	120FFFh
17	35	287	11F000h	11FFFFh
	|	:	:	:
	34	272	110000h	110FFFh
16	33	271	10F000h	10FFFFh
	|	:	:	:
	32	256	100000h	100FFFh

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
15	31	255	0FF000h	0FFFFFh
	|	:	:	:
	30	240	0F0000h	0F0FFFh
14	29	239	0EF000h	0EFFFFh
	|	:	:	:
	28	224	0E0000h	0E0FFFh
13	27	223	0DF000h	0DFFFFh
	|	:	:	:
	26	208	0D0000h	0D0FFFh
12	25	207	0CF000h	0CFFFFh
	|	:	:	:
	24	192	0C0000h	0C0FFFh
11	23	191	0BF000h	0BFFFFh
	|	:	:	:
	22	176	0B0000h	0B0FFFh
10	21	175	0AF000h	0AFFFFh
	|	:	:	:
	20	160	0A0000h	0A0FFFh
9	19	159	09F000h	09FFFFh
	|	:	:	:
	18	144	090000h	090FFFh
8	17	143	08F000h	08FFFFh
	|	:	:	:
	16	128	080000h	080FFFh
7	15	127	07F000h	07FFFFh
	|	:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
	|	:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
	|	:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
	|	:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
	|	:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
	|	:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
	|	:	:	:
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
	|	:	:	:
	|	2	002000h	002FFFh
	0	1	001000h	001FFFh
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, 4READ, RES, REMS, SQIID, RDBLOCK, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported
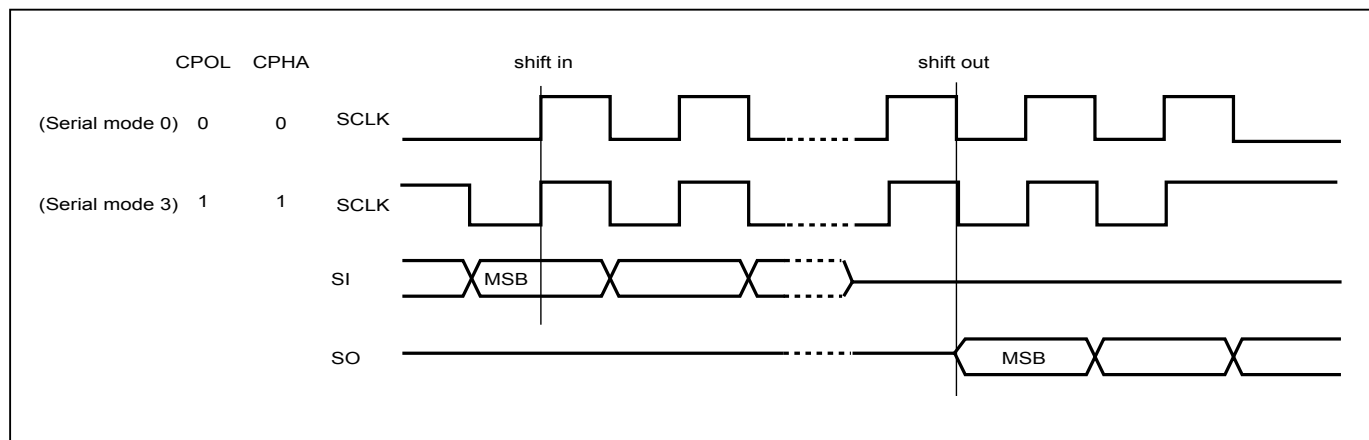
Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enabled.

Figure 2. Enable QPI Sequence (Command 35H)
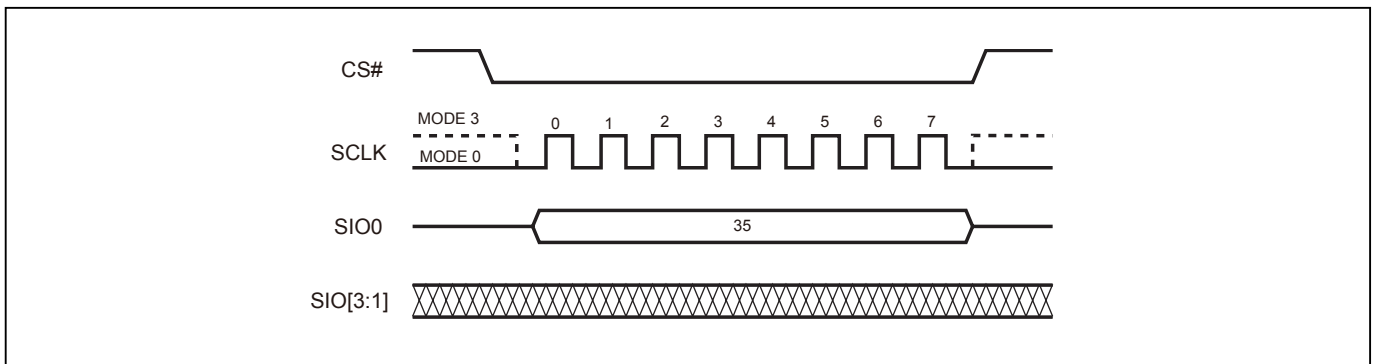
Reset QPI mode

By issuing F5H command, the device is reset to 1-I/O SPI mode.

Figure 3. Reset QPI Mode (Command F5H)
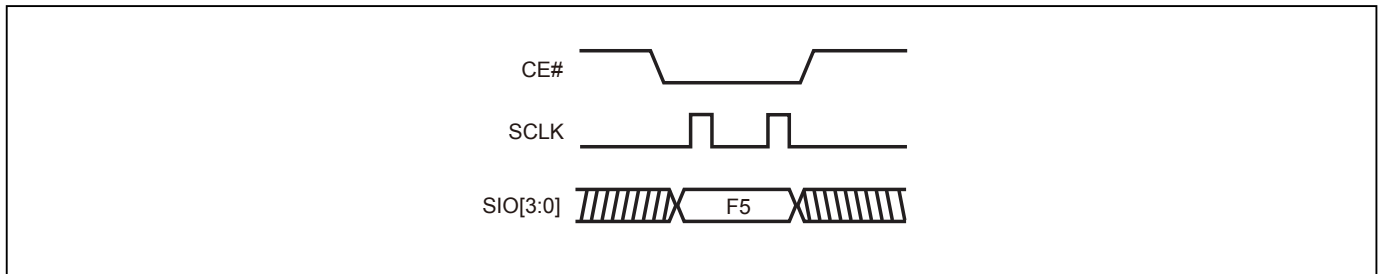
Fast QPI Read mode (FASTRDQ)

To increase the code transmission speed, the device provides a "Fast QPI Read Mode" (FASTRDQ). By issuing command code EBH, the FASTRDQ mode is enabled. The number of dummy cycle increase from 4 to 6 cycles. The read cycle frequency will increase from 84MHz to 104MHz.

Figure 4. Fast QPI Read Mode (FASTRDQ) (Command EBH)
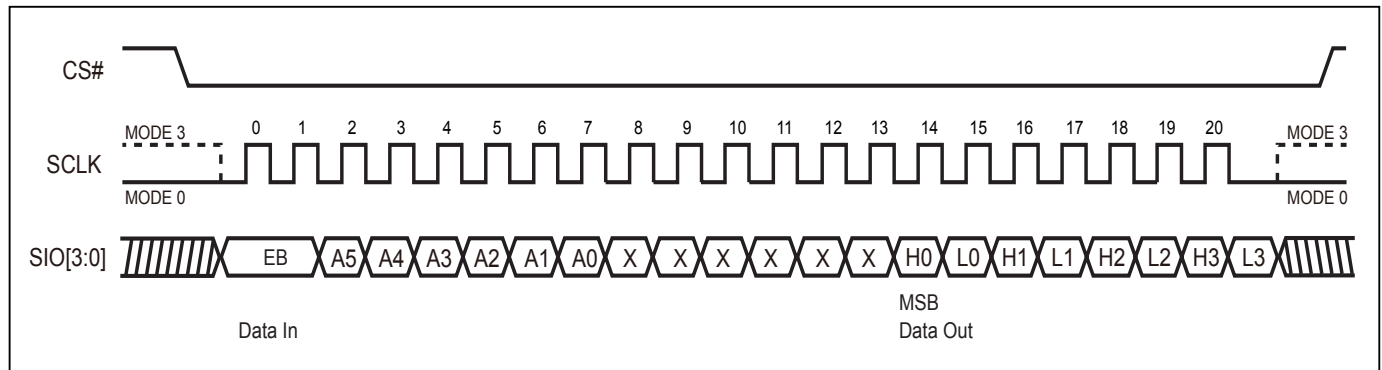
9. COMMAND DESCRIPTION

Table 5. Command Set

Read Commands

I/O	1	1	1	2	4	4	4	4
Read Mode	SPI	SPI	SPI	SPI	SPI	SPI	QPI	QPI
Command (byte)	READ (normal read)	FAST READ * (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command) Note1	W4READ	4READ * (4 x I/O read command) Note1	FAST READ * (fast read data)	4READ * (4 x I/O read command) Note1
Clock rate (MHz)	33	104	104	84	84	104	84	104
1st byte	03 (hex)	0B (hex)	5A (hex)	BB (hex)	E7 (hex)	EB (hex)	0B (hex)	EB (hex)
2nd byte	AD1(8)	AD1(8)	AD1(8)	AD1(4)	AD1(2)	AD1(2)	AD1(2)	AD1(2)
3rd byte	AD2(8)	AD2(8)	AD2(8)	AD2(4)	AD2(2)	AD2(2)	AD2(2)	AD2(2)
4th byte	AD3(8)	AD3(8)	AD3(8)	AD3(4)	AD3(2)	AD3(2)	AD3(2)	AD3(2)
5th byte		Dummy(8)	Dummy(8)	Dummy(4)	Dummy(4)	Dummy(6)	Dummy(4)	Dummy(6)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high	Quad I/O read with 4 dummy cycles in 84MHz	Quad I/O read with 6 dummy cycles in 104MHz	n bytes read out until CS# goes high	Quad I/O read with 6 dummy cycles in 104MHz

Program/Erase Commands

Command (byte)	WREN* (write enable)	WRDI * (write disable)	RDSR * (read status register)	WRSR * (write status register)	4PP (quad page program)	SE * (sector erase)	BE 32K * (block erase 32KB)
1st byte	06 (hex)	04 (hex)	05 (hex)	01 (hex)	38 (hex)	20 (hex)	52 (hex)
2nd byte				Values	AD1	AD1	AD1
3rd byte					AD2	AD2	AD2
4th byte					AD3	AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to write new values of the status register	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block

Command (byte)	BE * (block erase 64KB)	CE * (chip erase)	PP * (page program)	DP * (Deep power down)	RDP * (Release from deep power down)	PGM/ERS Suspend * (Suspends Program/ Erase)	PGM/ERS Resume * (Resumes Program/ Erase)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	B0 (hex)	30 (hex)
2nd byte	AD1		AD1				
3rd byte	AD2		AD2				
4th byte	AD3		AD3				
Action	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode		

Security/ID/Mode Setting/Reset Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO * (enter secured OTP)	EXSO * (exit secured OTP)	RDSCUR * (read security register)	WRSCUR * (write security register)
1st byte	9F (hex)	AB (hex)	90 (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte		x	x				
3rd byte		x	x				
4th byte		x	ADD (Note 2)				
5th byte							
Action	outputs JEDEC ID: 1-byte Manufact-urer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

COMMAND (byte)	SBLK * (single block lock)	SBULK * (single block unlock)	RDBLOCK * (block protect read)	GBLK * (gang block lock)	GBULK * (gang block unlock)	NOP * (No Operation)	RSTEN * (Reset Enable)
1st byte	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)	00 (hex)	66 (hex)
2nd byte	AD1	AD1	AD1				
3rd byte	AD2	AD2	AD2				
4th byte	AD3	AD3	AD3				
Action	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect		

COMMAND (byte)	RST * (Reset Memory)	EQIO (Enable Quad I/O)	RSTQIO (Reset Quad I/O)	QPIID (QPI ID Read)	SBL * (Set Burst Length)	WPSEL * (Write Protect Selection)
1st byte	99 (hex)	35 (hex)	F5 (hex)	AF (hex)	C0 (hex)	68 (hex)
2nd byte					Value	
3rd byte						
4th byte						
Action		Entering the QPI mode	Exiting the QPI mode	ID in QPI interface	to set Burst length	to enter and enable individal block protect mode

Note 1: Command set highlighted with (*) are supported both in SPI and QPI mode.

Note 2: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO1 which is different from 1 x I/O condition.

Note 3: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 4: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 5: *Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.*

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode. (Please refer to *"Figure 23. Write Enable (WREN) Sequence (Command 06) (SPI Mode)"* and *"Figure 24. Write Enable (WREN) Sequence (Command 06) (QPI Mode)"*)

9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode. (Please refer to *"Figure 26. Write Disable (WRDI) Sequence (Command 04) (QPI Mode)"* and *"Figure 25. Write Disable (WRDI) Sequence (Command 04) (SPI Mode)"*)

The WEL bit is reset by following situations:
- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Pgm/Ers Suspend

9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 9. ID Definitions"* ID Definitions.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

9-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to *"Figure 28. Read Status Register (RDSR) Sequence (Command 05) (SPI Mode)"* and *"Figure 29. Read Status Register (RDSR) Sequence (Command 05) (QPI Mode)"*)

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

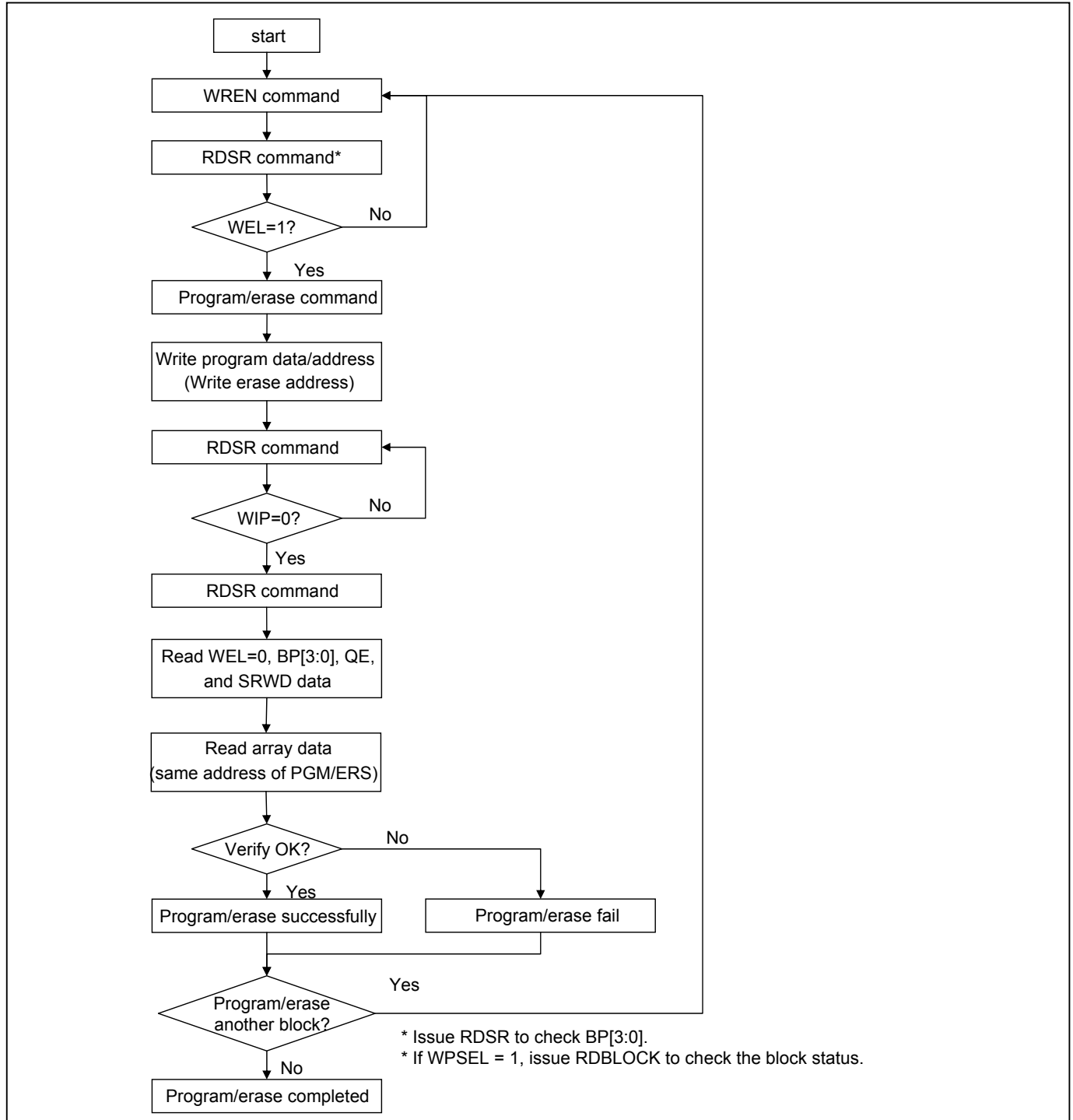**Figure 5. Program/ Erase flow with read array data**

Figure 6. Program/ Erase flow without read array data (read P_FAIL/E_FAIL flag)

```
                    ┌──────────────┐
                    │    start     │
                    └──────┬───────┘
                           ↓
                ┌─────────────────────┐ ◄──────────────────────┐
                │    WREN command     │                        │
                └──────────┬──────────┘                        │
                           ↓                                   │
                ┌─────────────────────┐                        │
                │   RDSR command*     │                        │
                └──────────┬──────────┘                        │
                           ↓                    No             │
                       ◇ WEL=1? ◇ ─────────────────────────────┘
                           │ Yes
                           ↓
                ┌─────────────────────┐
                │ Program/erase command │
                └──────────┬──────────┘
                           ↓
                ┌──────────────────────────┐
                │ Write program data/address │
                │  (Write erase address)     │
                └──────────┬───────────────┘
                           ↓
                ┌─────────────────────┐ ◄────────┐
                │    RDSR command     │           │
                └──────────┬──────────┘           │
                           ↓              No       │
                       ◇ WIP=0? ◇ ────────────────┘
                           │ Yes
                           ↓
                ┌─────────────────────┐
                │    RDSR command     │
                └──────────┬──────────┘
                           ↓
                ┌──────────────────────────┐
                │ Read WEL=0, BP[3:0], QE,   │
                │   and SRWD data            │
                └──────────┬───────────────┘
                           ↓
                ┌─────────────────────┐
                │   RDSCUR command    │
                └──────────┬──────────┘
                           ↓
                  ◇ P_FAIL/E_FAIL =1 ? ◇ ──────────Yes──────────┐
                           │ No                                  ↓
              ┌────────────────────────┐          ┌────────────────────────┐
              │ Program/erase successfully │       │   Program/erase fail    │
              └───────────┬────────────┘          └────────────────────────┘
                          ↓
                  ◇ Program/erase  ◇ ──────────Yes──────────────────────────┐
                  ◇ another block? ◇                                        (to WREN)
                          │ No
                          ↓
              ┌────────────────────────┐
              │ Program/erase completed │
              └────────────────────────┘
```

* Issue RDSR to check BP[3:0].
* If WPSEL = 1, issue RDBLOCK to check the block status.

Figure 7. WRSR flow

The definitions of the status register bits are as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in "Table 2. Protected Area Sizes") of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, performs SPI Quad modes when it is reset to "0" (factory default) to enable WP# or is set to "1" to enable Quad SIO2 and SIO3. QE bit is only valid for SPI mode. When operate in SPI mode, and quad IO read is desired (for command EBh/E7h, or quad IO program, 38h). WRSR command has to be set the through Status Register bit 6, the QE bit. Then the SPI Quad I/O commands (EBh/E7h/38h) will be accepted by flash. If QE bit is not set, SPI Quad I/O commands (EBh/E7h/38h) will be invalid commands, the device will not respond to them. Once QE bit is set, all SPI commands are valid. 1I/O commands and 2 I/O commands can be issued no matter QE bit is "0" or "1". When in QPI mode, QE bit will not affect the operation of QPI mode at all. Therefore either "0" or "1" value of QE bit does not affect the QPI mode operation.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: See the "Table 2. Protected Area Sizes".