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MX25U3235F

1.8V, 32M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Fast Program and Erase time*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Quad Peripheral Interface (QPI) Read / Program Mode*
- *Program Suspend/Resume & Erase Suspend/Resume*

Contents

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1.8V 32M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 33,554,432 x 1 bit structure
  or 16,777,216 x 2 bits (two I/O mode) structure
  or 8,388,608 x 4 bits (four I/O mode) structure
- Equal Sectors with 4K byte each,
  or Equal Blocks with 32K byte each
  or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V

PERFORMANCE

- High Performance
  - Fast read for SPI mode
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast read for QPI mode
    - 4 I/O: 84MHz with 2+2 dummy cycles, equivalent to 336MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast program time:
    0.5ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 12us (typical)
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
  - Fast erase time:
    - 35ms (typ.)/sector (4K-byte per sector);
    - 200ms(typ.)/block (32K-byte per block),
    - 350ms(typ.)/block (64K-byte per block)
- Low Power Consumption
  - Low active read current:
    - 20mA(typ.) at 104MHz,
      15mA(typ.) at 84MHz
  - Low active erase current:
    - 18mA(typ.) at Sector Erase, Block Erase (32KB/64KB);
      20mA at Chip Erase
  - Low active programming current: 20mA (typ.)
  - Standby current: 10uA (typ.)
- Deep Power Down: 1.5uA(typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 4k-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or Serial Data Input/Output for 4 x I/O read mode
- RESET#/SIO3
  - Hardware Reset pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
  -8-pin SOP (200mil)
  -8-land WSON (6x5mm)
  -8-land USON (4x3mm)
  -8-land XSON(4x4mm)
  -12-ball WLCSP
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25U3235F is 32Mb bits Serial NOR Flash memory, which is configured as 4,194,304 x 8 internally. When it is in two or four I/O mode, the structure becomes 16,777,216 bits x 2 or 8,388,608 bits x 4.

MX25U3235F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and RESET# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U3235F MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please refer to the security features section for more details.

The MX25U3235F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

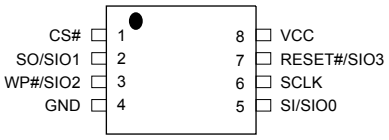
Table 1. Additional Feature

Protection and Security	MX25U3235F
Flexible Block Protection (BP0-BP3)	V
4K-bit security OTP	V

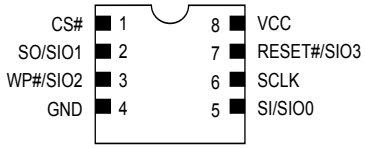
Read Performance	MX25U3235F							
I/O mode	SPI						QPI	
I/O	1 I/O	1I /2O	2 I/O	1I/4O	4 I/O	4 I/O	4 I/O	4 I/O
Dummy Cycle	8	8	4	8	4	6	4	6
Frequency	104MHz	104MHz	84 MHz	104MHz	84 MHz	104MHz	84 MHz	104MHz

3. PIN CONFIGURATIONS

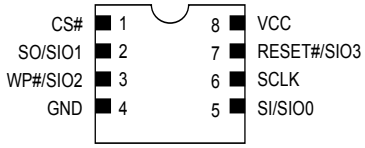
8-PIN SOP (200mil)



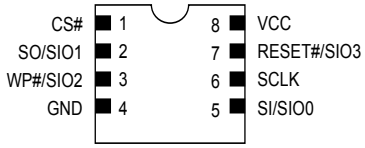
8-LAND WSON (6x5mm)



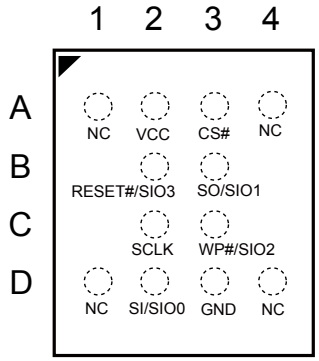
8-LAND USON (4x3mm)



8-LAND XSON(4x4mm)



12-BALL BGA (WLCSP) TOP View

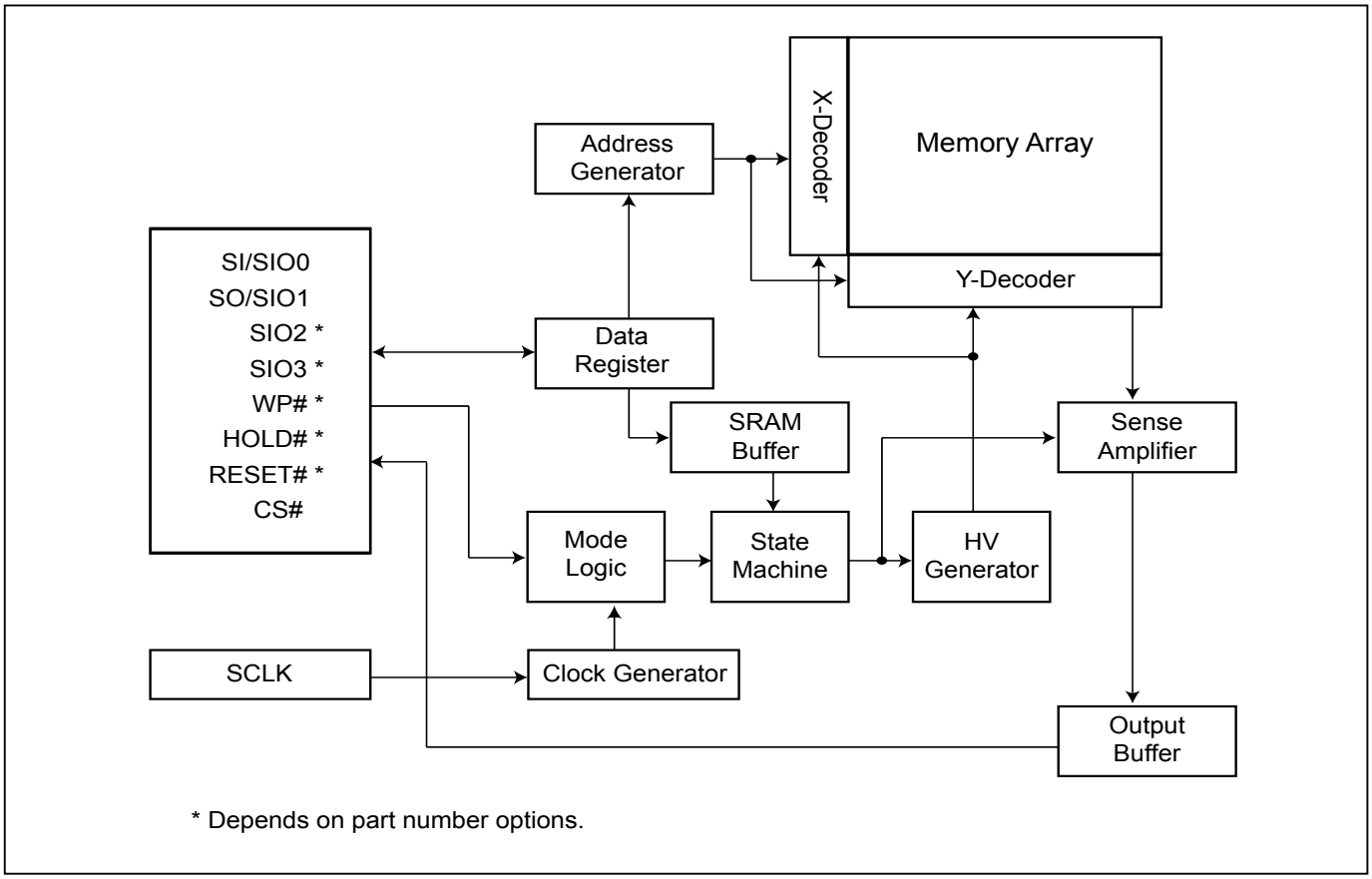


4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
RESET#/SIO3	Hardware Reset Pin Active low or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground

Note: The pin of RESET#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to RESET#/SIO3 or WP#/SIO2 pin.

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset (internal timer) may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except the Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, protected block 63rd)
0	0	1	0	2 (2blocks, protected block 62nd-63rd)
0	0	1	1	3 (4blocks, protected block 60th-63rd)
0	1	0	0	4 (8blocks, protected block 56th-63rd)
0	1	0	1	5 (16blocks, protected block 48th-63rd)
0	1	1	0	6 (32blocks, protected block 32nd-63rd)
0	1	1	1	7 (64blocks, protected all)
1	0	0	0	8 (64blocks, protected all)
1	0	0	1	9 (32blocks, protected block 0th-31st)
1	0	1	0	10 (48blocks, protected block 0th-47th)
1	0	1	1	11 (56blocks, protected block 0th-55th)
1	1	0	0	12 (60blocks, protected block 0th-59th)
1	1	0	1	13 (62blocks, protected block 0th-61st)
1	1	1	0	14 (63blocks, protected block 0th-62nd)
1	1	1	1	15 (64blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 9. Security Register Definition"* for security register bit definition and *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

- **Note:** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010-xxx1FF	3968-bit	N/A	

7. MEMORY ORGANIZATION

Table 4. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
63	127	1023	3FF000h	3FFFFFh
		⋮		
		1016	3F8000h	3F8FFFh
	126	1015	3F7000h	3F7FFFh
		⋮		
		1008	3F0000h	3F0FFFh
62	125	1007	3EF000h	3EFFFFh
		⋮		
		1000	3E8000h	3E8FFFh
	124	999	3E7000h	3E7FFFh
		⋮		
		992	3E0000h	3E0FFFh
61	123	991	3DF000h	3DFFFFh
		⋮		
		984	3D8000h	3D8FFFh
	122	983	3D7000h	3D7FFFh
		⋮		
		976	3D0000h	3D0FFFh
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

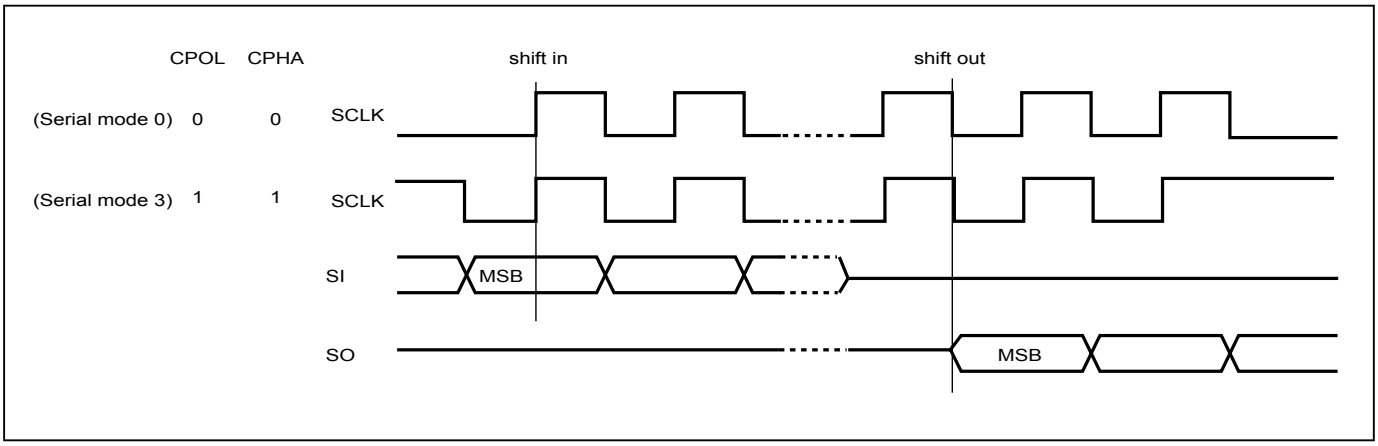
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, DREAD, 2READ, QREAD, 4READ, W4READ, RDSFDP, RES, REMS, QPIID, RDBLOCK, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

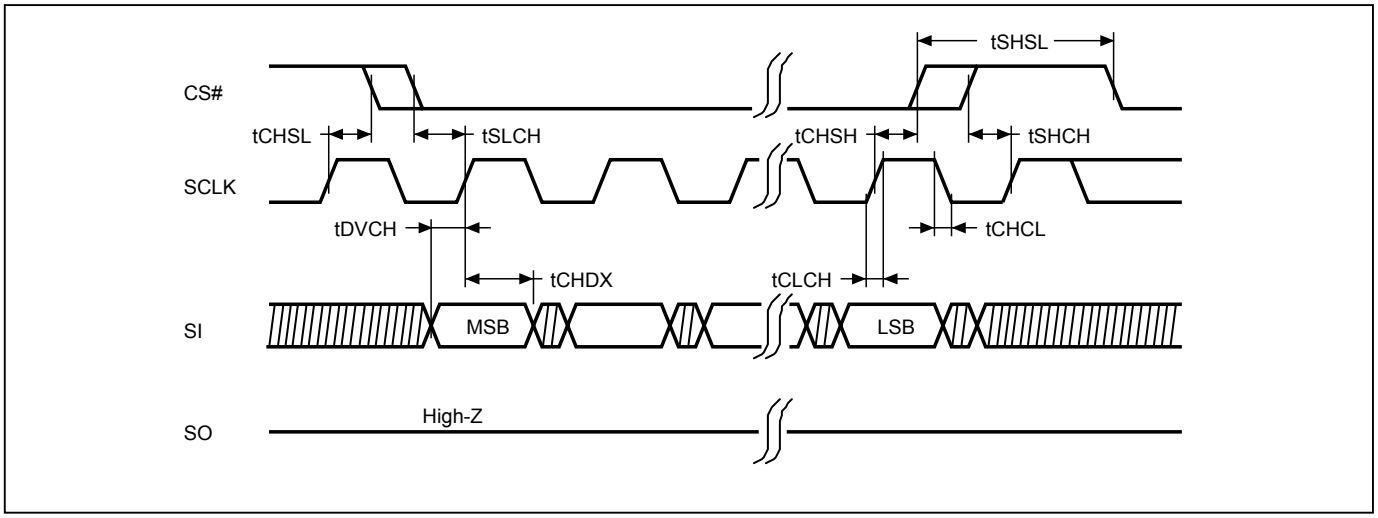
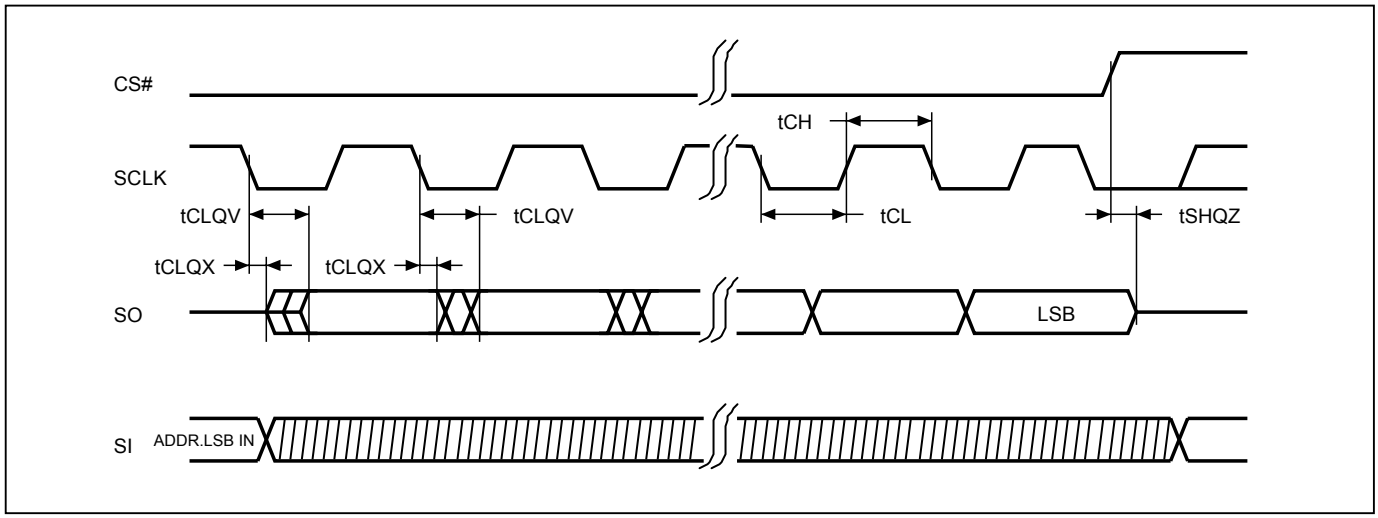


Figure 3. Output Timing



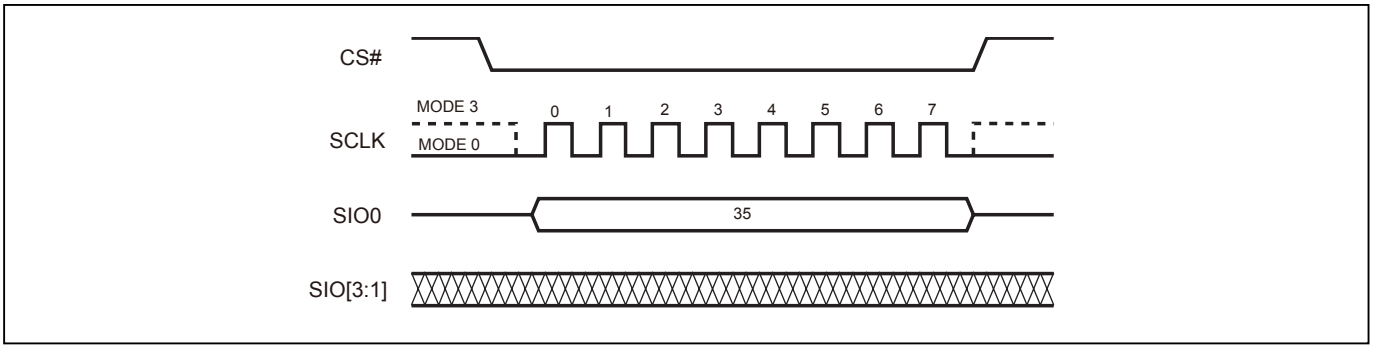
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing EQIO command (35h), the QPI mode is enabled.

Figure 4. Enable QPI Sequence (Command 35h)

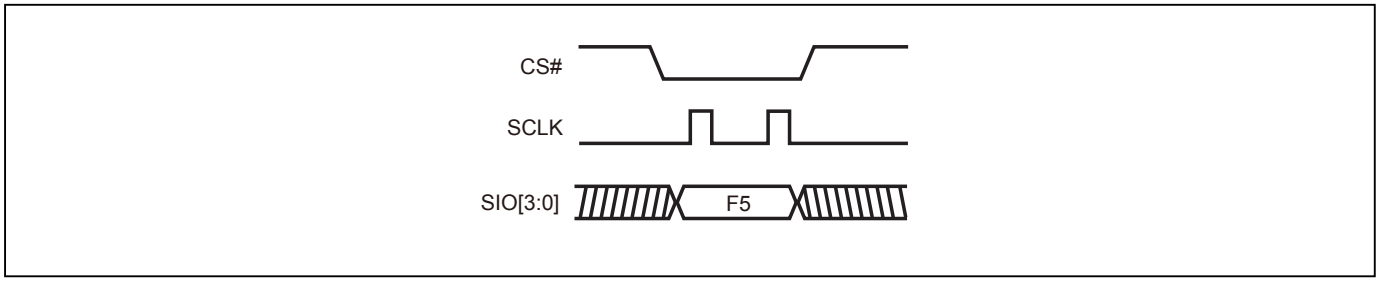


Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note: For EQIO and RSTQIO commands, CS# high width has to follow "From Write/Erase/Program to Read Status Register" specification of tSHSL (as defined in *"Table 20. AC Characteristics"*) for next instruction.

Figure 5. Reset QPI Mode (Command F5h)



9. COMMAND DESCRIPTION

Table 5. Command Set

Read/Write Array Commands

Mode	SPI	SPI/QPI	SPI	SPI	SPI/QPI	SPI
Command (byte)	READ (normal read)	FAST READ (fast read data)	DREAD (1I / 2O read command)	2READ (2 x I/O read command)Note1	4READ (4 x I/O read)	W4READ
1st byte	03 (hex)	0B (hex)	3B (hex)	BB (hex)	EB (hex)	E7 (hex)
2nd byte	ADD1(8)	ADD1(8)	ADD1(8)	ADD1(4)	ADD1(2)	ADD1(2)
3rd byte	ADD2(8)	ADD2(8)	ADD2(8)	ADD2(4)	ADD2(2)	ADD2(2)
4th byte	ADD3(8)	ADD3(8)	ADD3(8)	ADD3(4)	ADD3(2)	ADD3(2)
5th byte		Dummy(8)/(4)*	Dummy(8)	Dummy(4)	Dummy(6)	Dummy(4)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by Dual Output until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	Quad I/O read with 6 dummy cycles	Quad I/O read for with 4 dummy cycles

Mode	SPI	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI
Command (byte)	QREAD (1I/4O read)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)
1st byte	6B (hex)	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)
2nd byte	ADD1(8)	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2(8)	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3(8)	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	Dummy(8)					
Action	n bytes read out by Quad output until CS# goes high	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block

Mode	SPI/QPI
Command (byte)	CE (chip erase)
1st byte	60 or C7 (hex)
2nd byte	
3rd byte	
4th byte	
5th byte	
Action	to erase whole chip

Note: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

* The fast read command (0Bh) when under QPI mode, the dummy cycle is 4 clocks.

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	WRSR (write status register)	WPSEL (Write Protect Selection)	EQIO (Enable QPI)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI
1st byte	06 (hex)	04 (hex)	05 (hex)	01 (hex)	68 (hex)	35 (hex)
2nd byte				Values		
3rd byte						
4th byte						
5th byte						
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to write new values of the status register	to enter and enable individal block protect mode	Entering the QPI mode

Command (byte)	RSTQIO (Reset QPI)	PGM/ERS Suspend (Suspends Program/Erase)	PGM/ERS Resume (Resumes Program/Erase)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)
Mode	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	F5 (hex)	B0 (hex)	30 (hex)	B9 (hex)	AB (hex)	C0 (hex)
2nd byte						Value
3rd byte						
4th byte						
5th byte						
Action	Exiting the QPI mode			enters deep power down mode	release from deep power down mode	to set Burst length

ID/Security Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1(8)		
3rd byte		x	x		ADD2(8)		
4th byte		x	ADD *(Note 2)*		ADD3(8)		
5th byte					Dummy(8)		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	ID in QPI interface	Read SFDP mode	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode

COMMAND (byte)	RDSCUR (read security register)	WRSCUR (write security register)	SBLK (single block lock	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	2B (hex)	2F (hex)	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)
2nd byte			ADD1	ADD1	ADD1		
3rd byte			ADD2	ADD2	ADD2		
4th byte			ADD3	ADD3	ADD3		
5th byte							
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect

Reset Commands

COMMAND (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			*(Note 4)*

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1 which is different from 1 x I/O condition.
Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 4: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

Figure 6. Write Enable (WREN) Sequence (SPI Mode)

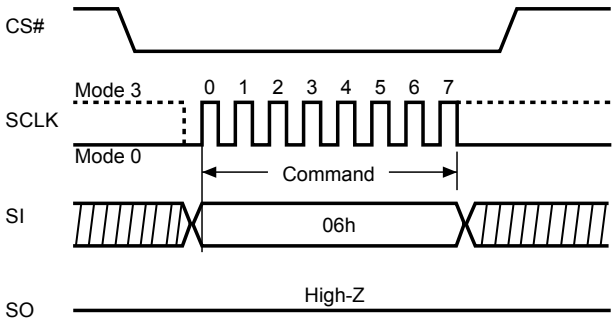
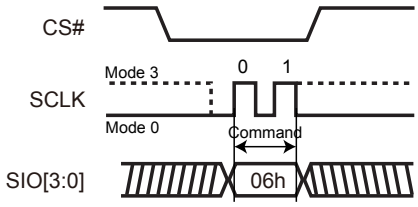


Figure 7. Write Enable (WREN) Sequence (QPI Mode)



9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Program/Erase Suspend
- Completion of Softreset command
- Completion of Write Security Register (WRSCUR) command
- Completion of Write Protection Selection (WPSEL) command

Figure 8. Write Disable (WRDI) Sequence (SPI Mode)

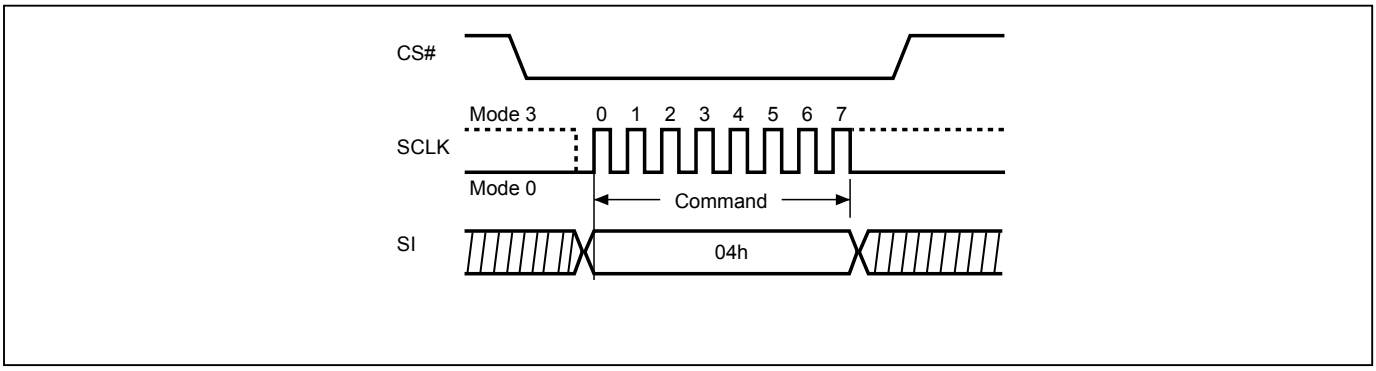
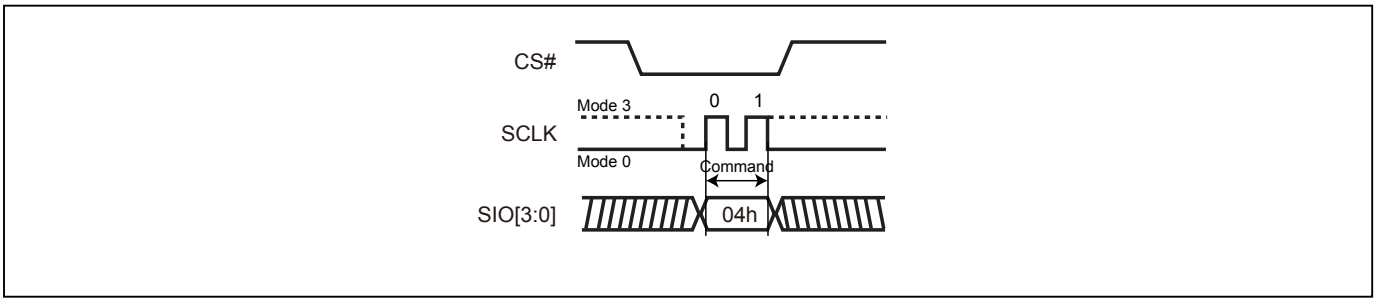


Figure 9. Write Disable (WRDI) Sequence (QPI Mode)



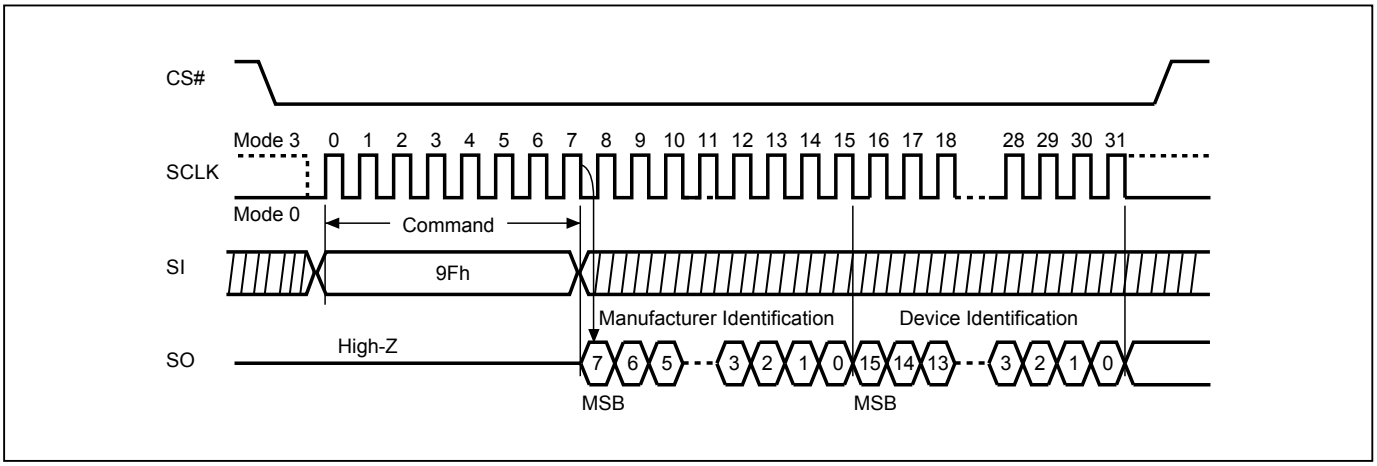
9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 6. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 10. Read Identification (RDID) Sequence (SPI mode only)



9-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 20. AC Characteristics"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. RESET# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are "don't care" in SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 11. Read Electronic Signature (RES) Sequence (SPI Mode)

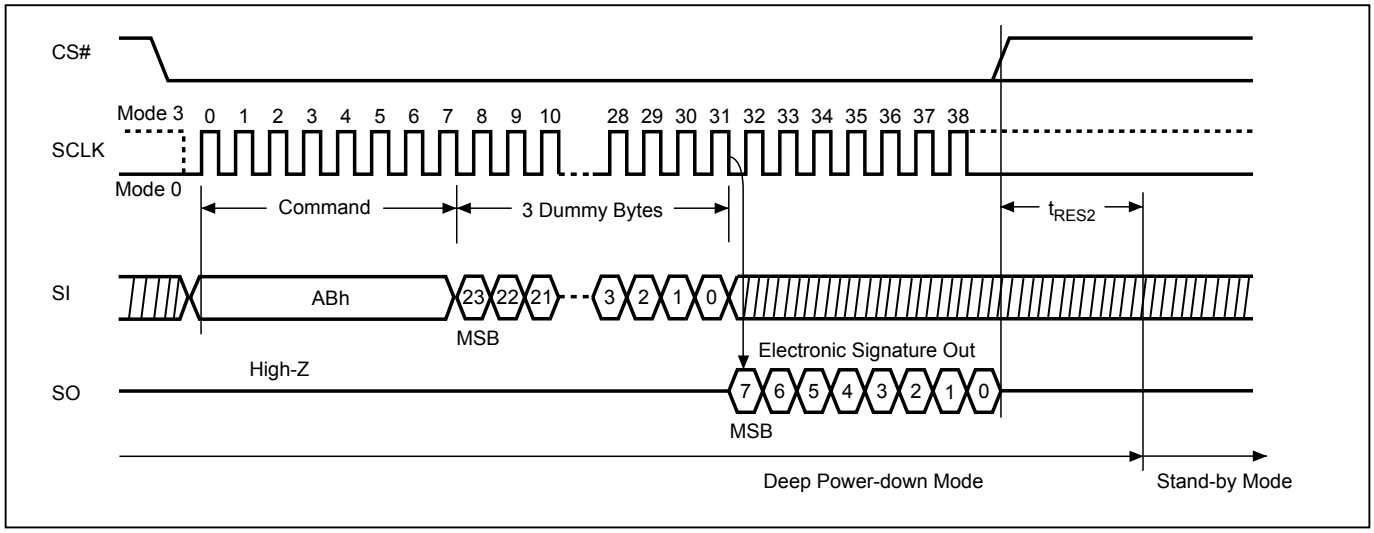


Figure 12. Read Electronic Signature (RES) Sequence (QPI Mode)

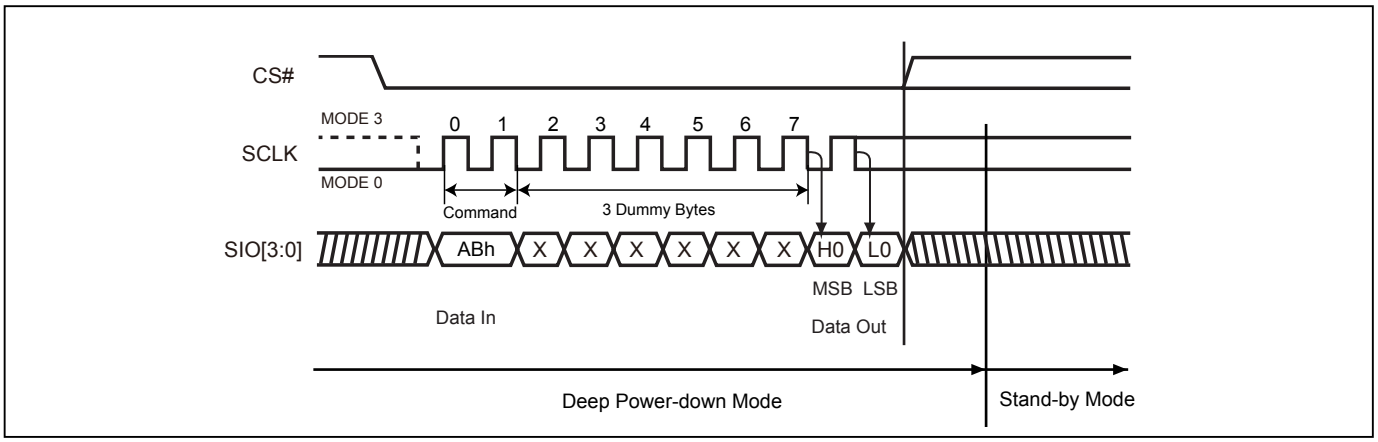


Figure 13. Release from Deep Power-down (RDP) Sequence (SPI Mode)

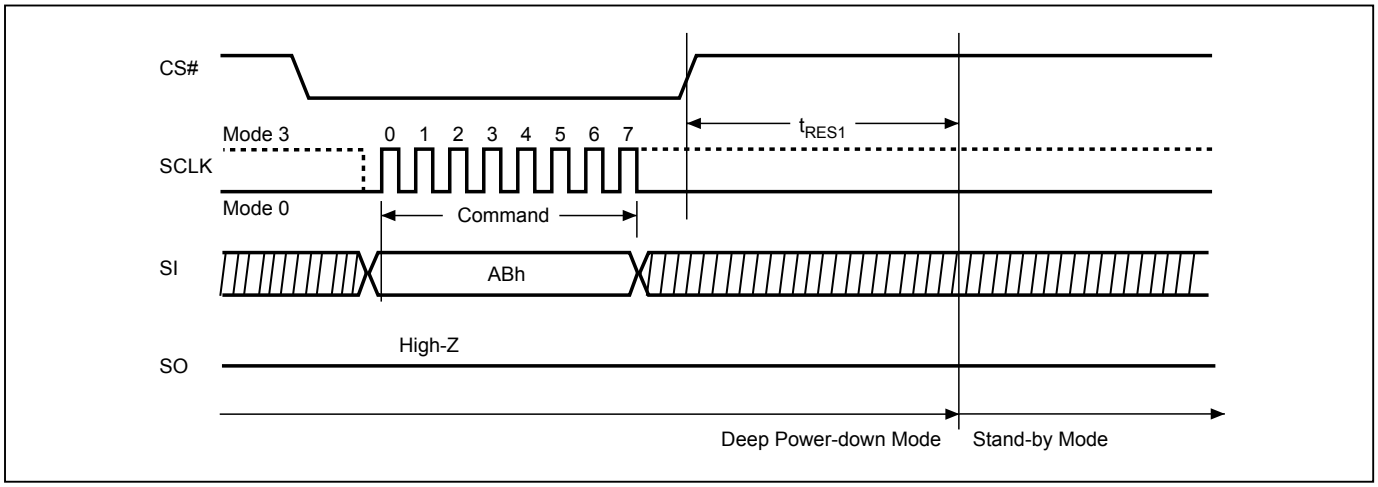


Figure 14. Release from Deep Power-down (RDP) Sequence (QPI Mode)