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MACRONIX
INTERNATIONAL Co., LTD.

MX25U8035E

MX25U8035E DATASHEET

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8M-BIT [x 1/x 2/x 4] 1.8V CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY**1.FEATURES****GENERAL**

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 8M : 8,388,608 x 1 bit structure or 4,194,304 x 2 bits (two I/O read mode) structure or 2,097,152 x 4 bits (four I/O read mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
 - Any Block can be erased individually
- Single Power Supply Operation
 - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V

PERFORMANCE

- High Performance
 - Fast read for SPI mode
 - 1 I/O: 104MHz with 8 dummy cycles
 - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
 - 4 I/O: 104MHz with 6 dummy cycles, equivalent to 416MHz
 - Fast read for QPI mode
 - 4 I/O: 84MHz with 4 dummy cycles, equivalent to 336MHz
 - 4 I/O: 104MHz with 6 dummy cycles, equivalent to 416MHz
 - Fast program time: 1.2ms(typ.) and 3ms(max.)/page (256-byte per page)
 - Byte program time: 10us (typical)
 - 8/16/32/64 byte Wrap-Around Burst Read Mode
 - Fast erase time: 45ms (typ.)/sector (4K-byte per sector); 250ms(typ.) /block (32K-byte per block); 500ms(typ.) /block (64K-byte per block); 5s(typ.) /chip
- Low Power Consumption
 - Low active read current: 20mA(max.) at 104MHz, 15mA(max.) at 84MHz
 - Low active erase/programming current: 20mA (typ.)
 - Standby current: 25uA (typ.)
- Deep Power Down: 2uA(typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
 - Additional 4k-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
 - Automatically erases and verifies data at selected sector or block
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)

- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID
 - RES command for 1-byte Device ID
 - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SIO0
 - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
 - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
 - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- NC/SIO3
 - NC pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
 - 8-pin SOP (150mil)
 - 8-pin SOP (200mil)
 - 8-land WSON (6x5mm)
 - 8-land USON (4x4mm)
 - **All devices are RoHS Compliant and Halogen-free**

2.GENERAL DESCRIPTION

The MX25U8035E are 8,388,608 bit serial Flash memory, which is configured as 1,048,576 x 8 internally. When it is in two or four I/O read mode, the structure becomes 4,194,304 bits x 2 or 2,097,152 bits x 4. MX25U8035E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin and WP# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U8035E MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25U8035E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

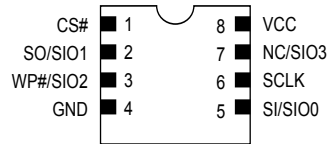
Table 1. Additional Feature Comparison

Part Name	Additional Features	Protection and Security		Read Performance					
				SPI				QPI	
		Flexible Block Protection (BP0-BP3)	4K-bit security OTP	1 I/O (104 MHz)	2 I/O (84 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)	4 I/O (84 MHz)	4 I/O (104 MHz)
MX25U8035E		V	V	V	V	V	V	V	V

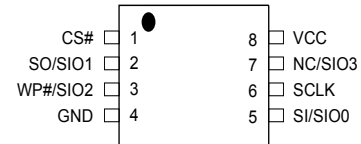
Part Name	Additional Features	Identifier			
		RES (command: AB hex)	REMS (command: 90 hex)	RDID (command: 9F hex)	QPIID (Command: AF hex)
		MX25U8035E	34 (hex)	C2 34 (hex) (if ADD=0)	C2 25 34

3. PIN CONFIGURATIONS

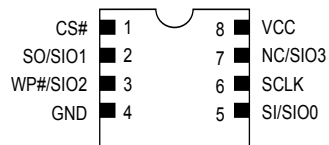
8-LAND USON (4x4mm)



8-PIN SOP (150mil) / 8-PIN SOP (200mil)



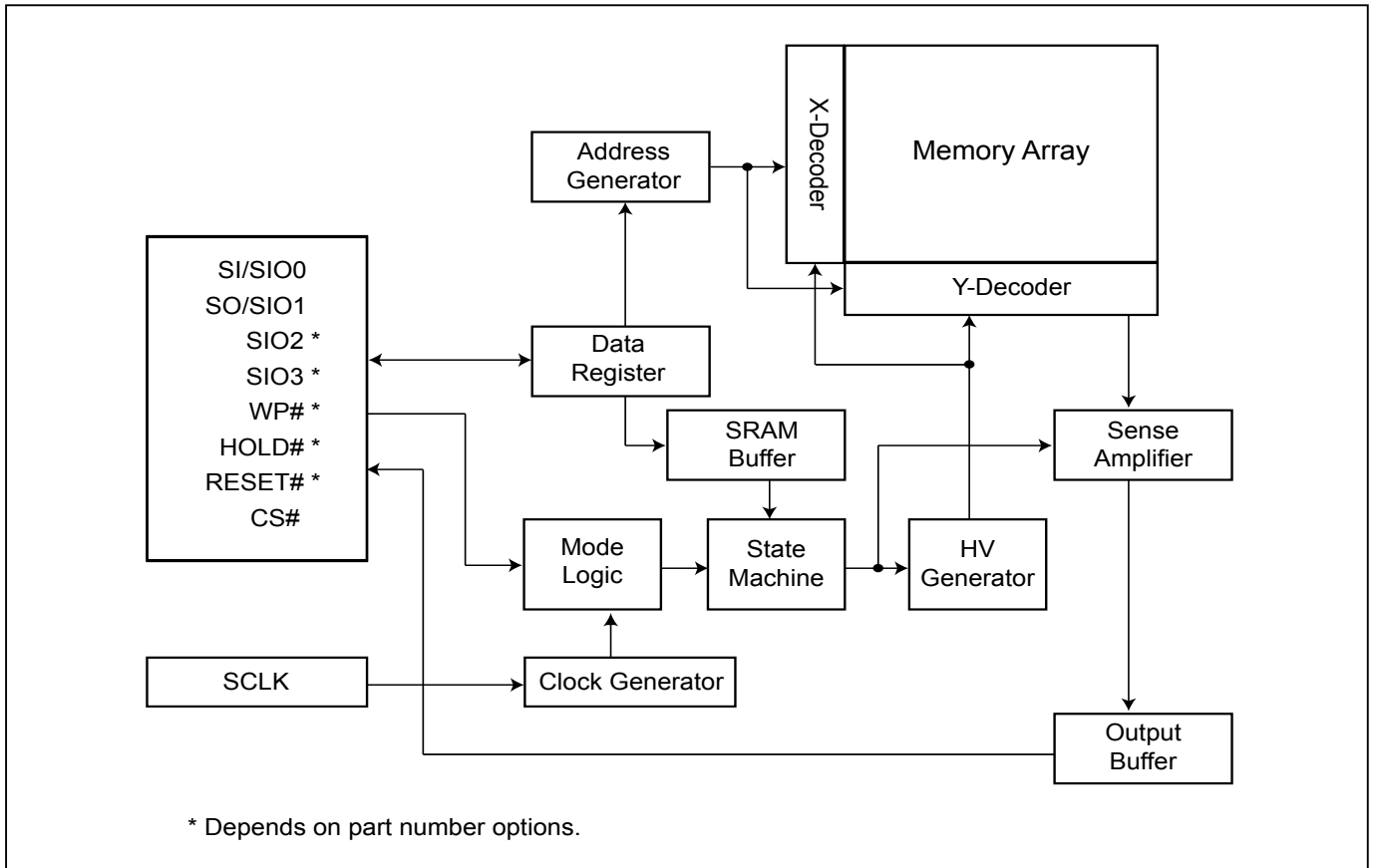
8-LAND WSON (6x5mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC pin (Not connected) or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 1.8V Power Supply
GND	Ground

5.BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
 - Power-up
 - Write Disable (WRDI) command completion
 - Write Status Register (WRSR) command completion
 - Page Program (PP) command completion
 - Sector Erase (SE) command completion
 - Block Erase 32KB (BE32K) command completion
 - Block Erase (BE) command completion
 - Chip Erase (CE) command completion
 - Program/Erase Suspend
 - Softreset command completion
 - Write Security Register (WRSCUR) command completion
 - Write Protection Selection (WPSEL) command completion
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES) and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as "[Table 2. Protected Area Sizes](#)", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits. Please refer to "[Table 2. Protected Area Sizes](#)".
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status bit				Protect Level
BP3	BP2	BP1	BP0	8Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, protected block 15th)
0	0	1	0	2(2blocks, protected block 14th~15th)
0	0	1	1	3 (4blocks, protected block 12th~15th)
0	1	0	0	4 (8blocks, protected block 8th~15th)
0	1	0	1	5 (16blocks, protected all)
0	1	1	0	6 (16blocks, protected all)
0	1	1	1	7 (16blocks, protected all)
1	0	0	0	8 (16blocks, protected all)
1	0	0	1	9 (16blocks, protected all)
1	0	1	0	10 (16blocks, protected all)
1	0	1	1	11 (8blocks, protected block 0th~7th)
1	1	0	0	12 (12blocks, protected block 0th~11th)
1	1	0	1	13 (14blocks, protected block 0th~13th)
1	1	1	0	14 (15blocks, protected block 0th~14th)
1	1	1	1	15 (16blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to ["Table 3. 4K-bit Secured OTP Definition"](#).

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP (ENSO) command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP (EXSO) command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to ["Table 9. Security Register Definition"](#) for security register bit definition and ["Table 3. 4K-bit Secured OTP Definition"](#) for address range definition.
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7.Memory Organization

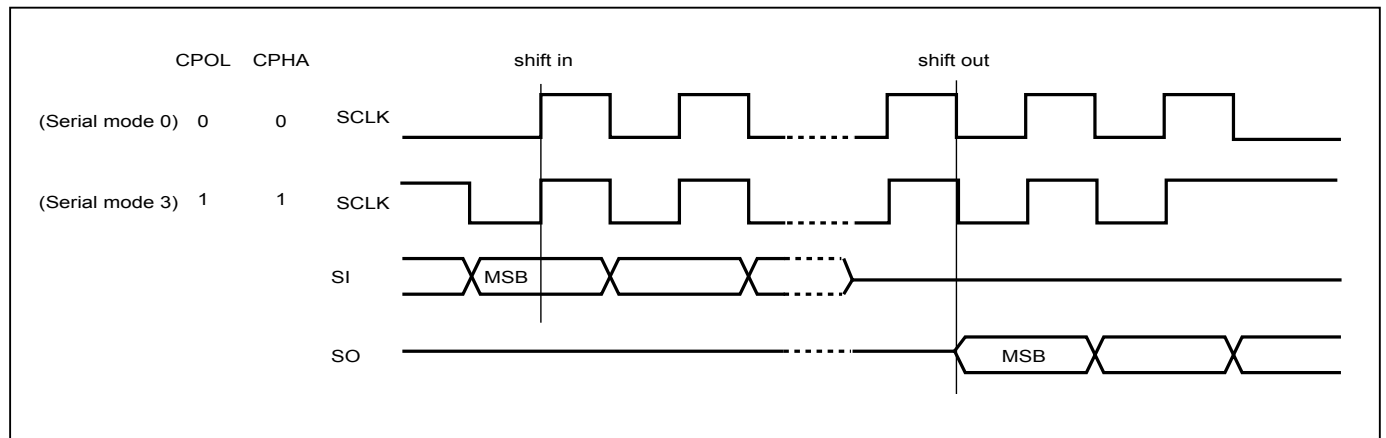
Table 4. Memory Organization (8Mb)

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
15	31	255	0FF000h	0FFFFFFh
		:	:	:
	30	240	0F0000h	0F0FFFh
14	29	239	0EF000h	0EFFFFh
		:	:	:
	28	224	0E0000h	0E0FFFh
13	27	223	0DF000h	0DFFFFh
		:	:	:
	26	208	0D0000h	0D0FFFh
12	25	207	0CF000h	0CFFFFh
		:	:	:
	24	192	0C0000h	0C0FFFh
11	23	191	0BF000h	0BFFFFh
		:	:	:
	22	176	0B0000h	0B0FFFh
10	21	175	0AF000h	0AFFFFh
		:	:	:
	20	160	0A0000h	0A0FFFh
9	19	159	09F000h	09FFFFh
		:	:	:
	18	144	090000h	090FFFh
8	17	143	08F000h	08FFFFh
		:	:	:
	16	128	080000h	080FFFh
7	15	127	07F000h	07FFFFh
		:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
		:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
		:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
		:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
		:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
		:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		:	:	:
	2	16	010000h	010FFFh
0		15	00F000h	00FFFFh
		:	:	:
		2	002000h	002FFFh
		1	001000h	001FFFh
	0	000000h	000FFFh	

8.DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "[Figure 1. Serial Modes Supported](#)".
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, 4READ, RES, REMS, SQIID, RDBLOCK, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, SBLK, SBULK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

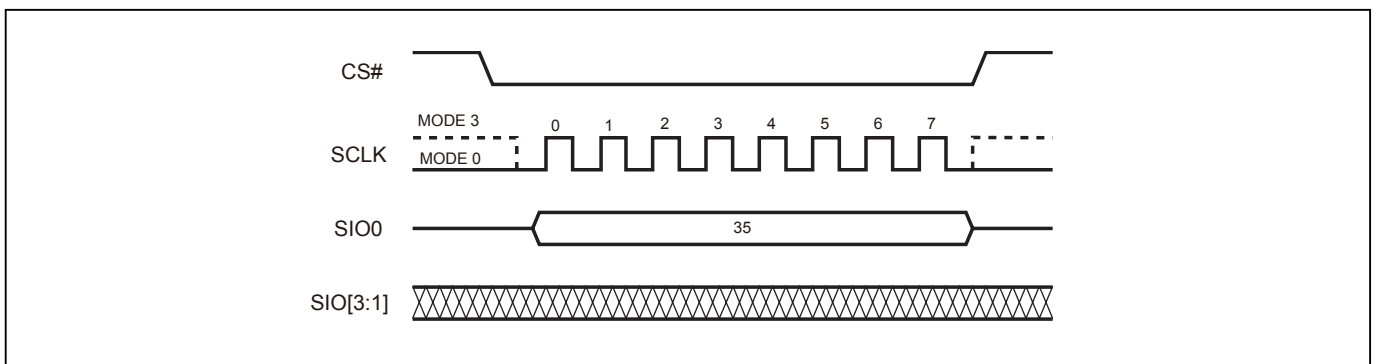
8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enable.

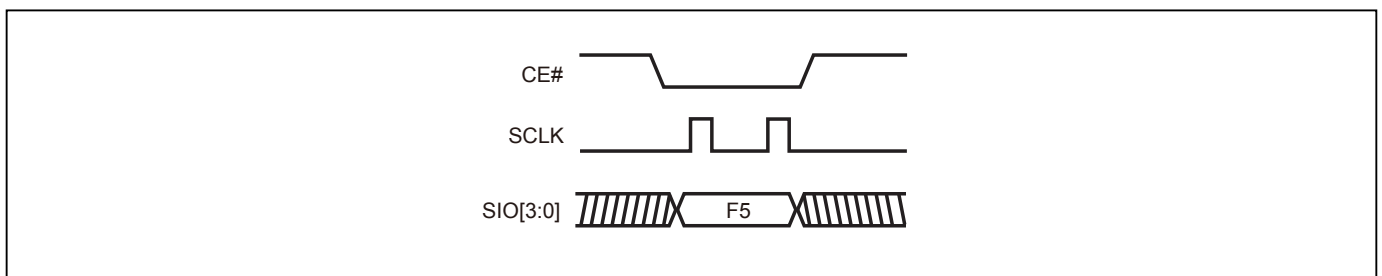
Figure 2. Enable QPI Sequence (Command 35H)



Reset QPI mode

By issuing F5H command, the device is reset to 1-I/O SPI mode.

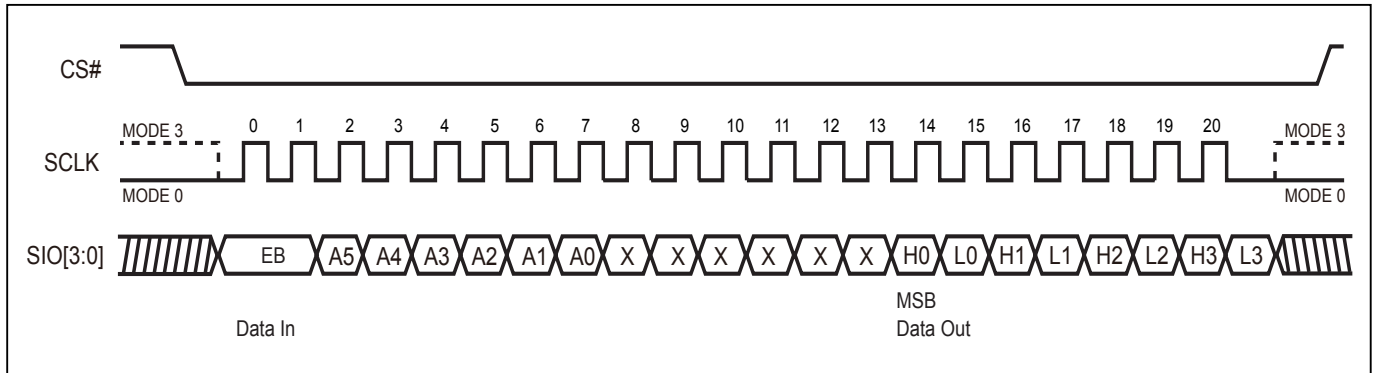
Figure 3. Reset QPI Mode (Command F5H)



Fast QPI Read mode (FASTRDQ)

To increase the code transmission speed, the device provides a "Fast QPI Read Mode" (FASTRDQ). By issuing command code EBH, the FASTRDQ mode is enable. The number of dummy cycle increase from 4 to 6 cycles. The read cycle frequency will increase from 84MHz to 104MHz.

Figure 4. Figure 5. Fast QPI Read Mode (FASTRDQ) (Command EBH)



9.COMMAND DESCRIPTION

Table 5. Command Set

Read Commands

I/O	1	1	1	2	4	4	4	4
Read Mode	SPI	SPI	SPI	SPI	SPI	SPI	QPI	QPI
Command (byte)	READ (normal read)	FAST READ * (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command) Note1	W4READ	4READ * (4 x I/O read command) Note1	FAST READ * (fast read data)	4READ * (4 x I/O read command) Note1
Clock rate (MHz)	33	104	104	84	84	104	84	104
1st byte	03 (hex)	0B (hex)	5A (hex)	BB (hex)	E7 (hex)	EB (hex)	0B (hex)	EB (hex)
2nd byte	AD1(8)	AD1(8)	AD1(8)	AD1(4)	AD1(2)	AD1(2)	AD1(2)	AD1(2)
3rd byte	AD2(8)	AD2(8)	AD2(8)	AD2(4)	AD2(2)	AD2(2)	AD2(2)	AD2(2)
4th byte	AD3(8)	AD3(8)	AD3(8)	AD3(4)	AD3(2)	AD3(2)	AD3(2)	AD3(2)
5th byte		Dummy(8)	Dummy(8)	Dummy(4)	Dummy(4)	Dummy(6)	Dummy(4)	Dummy(6)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high	Quad I/O read with 4 dummy cycles in 84MHz	Quad I/O read with 6 dummy cycles in 104MHz	n bytes read out until CS# goes high	Quad I/O read with 6 dummy cycles in 104MHz

Program/Erase Commands

Command (byte)	WREN* (write enable)	WRDI * (write disable)	RDSR * (read status register)	WRSR * (write status register)	4PP (quad page program)	SE * (sector erase)	BE 32K * (block erase 32KB)
1st byte	06 (hex)	04 (hex)	05 (hex)	01 (hex)	38 (hex)	20 (hex)	52 (hex)
2nd byte				Values	AD1	AD1	AD1
3rd byte					AD2	AD2	AD2
4th byte					AD3	AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to write new values of the status register	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block

Command (byte)	BE * (block erase 64KB)	CE * (chip erase)	PP * (page program)	DP * (Deep power down)	RDP * (Release from deep power down)	PGM/ERS Suspend * (Suspends Program/ Erase)	PGM/ERS Resume * (Resumes Program/ Erase)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	B0 (hex)	30 (hex)
2nd byte	AD1		AD1				
3rd byte	AD2		AD2				
4th byte	AD3		AD3				
Action	to erase the selected block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode		

Security/ID/Mode Setting/Reset Commands

Command (byte)	RDID (read identification)	RES * (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO * (enter secured OTP)	EXSO * (exit secured OTP)	RDSCUR * (read security register)	WRSCUR * (write security register)
1st byte	9F (hex)	AB (hex)	90 (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte		x	x				
3rd byte		x	x				
4th byte		x	ADD (Note 2)				
5th byte							
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

COMMAND (byte)	SBLK * (single block lock)	SBULK * (single block unlock)	RDBLOCK * (block protect read)	GBLK * (gang block lock)	GBULK * (gang block unlock)	NOP * (No Operation)	RSTEN * (Reset Enable)
1st byte	36 (hex)	39 (hex)	3C (hex)	7E (hex)	98 (hex)	00 (hex)	66 (hex)
2nd byte	AD1	AD1	AD1				
3rd byte	AD2	AD2	AD2				
4th byte	AD3	AD3	AD3				
Action	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect		

COMMAND (byte)	RST * (Reset Memory)	EQIO (Enable Quad I/O)	RSTQIO (Reset Quad I/O)	QPIID (QPI ID Read)	SBL * (Set Burst Length)	WPSEL * (Write Protect Selection)
1st byte	99 (hex)	35 (hex)	F5 (hex)	AF (hex)	C0 (hex)	68 (hex)
2nd byte					Value	
3rd byte						
4th byte						
Action		Entering the QPI mode	Exiting the QPI mode	ID in QPI interface	to set Burst length	to enter and enable individual block protect mode

Note 1: Command set highlighted with (*) are supported both in SPI and QPI mode.

Note 2: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO1 which is different from 1 x I/O condition.

Note 3: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 4: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 5: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode. (Please refer to "[Figure 19. Write Enable \(WREN\) Sequence \(Command 06\) \(SPI Mode\)](#)" and "[Figure 20. Write Enable \(WREN\) Sequence \(Command 06\) \(QPI Mode\)](#)")

9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode. (Please refer to "[Figure 21. Write Disable \(WRDI\) Sequence \(Command 04\) \(SPI Mode\)](#)" and "[Figure 23. Write Disable \(WRDI\) Sequence \(Command 04\) \(QPI Mode\)](#)")

The WEL bit is reset by following situations:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Pgm/Ers Suspend

9-3. Read Identification (RDID)

The RDID instruction is to read the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 25(hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as "[Table 8. ID Definitions](#)"

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

9-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode. (Please refer to "Figure 24. Read Status Register (RDSR) Sequence (Command 05) (SPI Mode)" and "Figure 25. Read Status Register (RDSR) Sequence (Command 05) (QPI Mode)")

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 5. Program/Erase flow with read array data

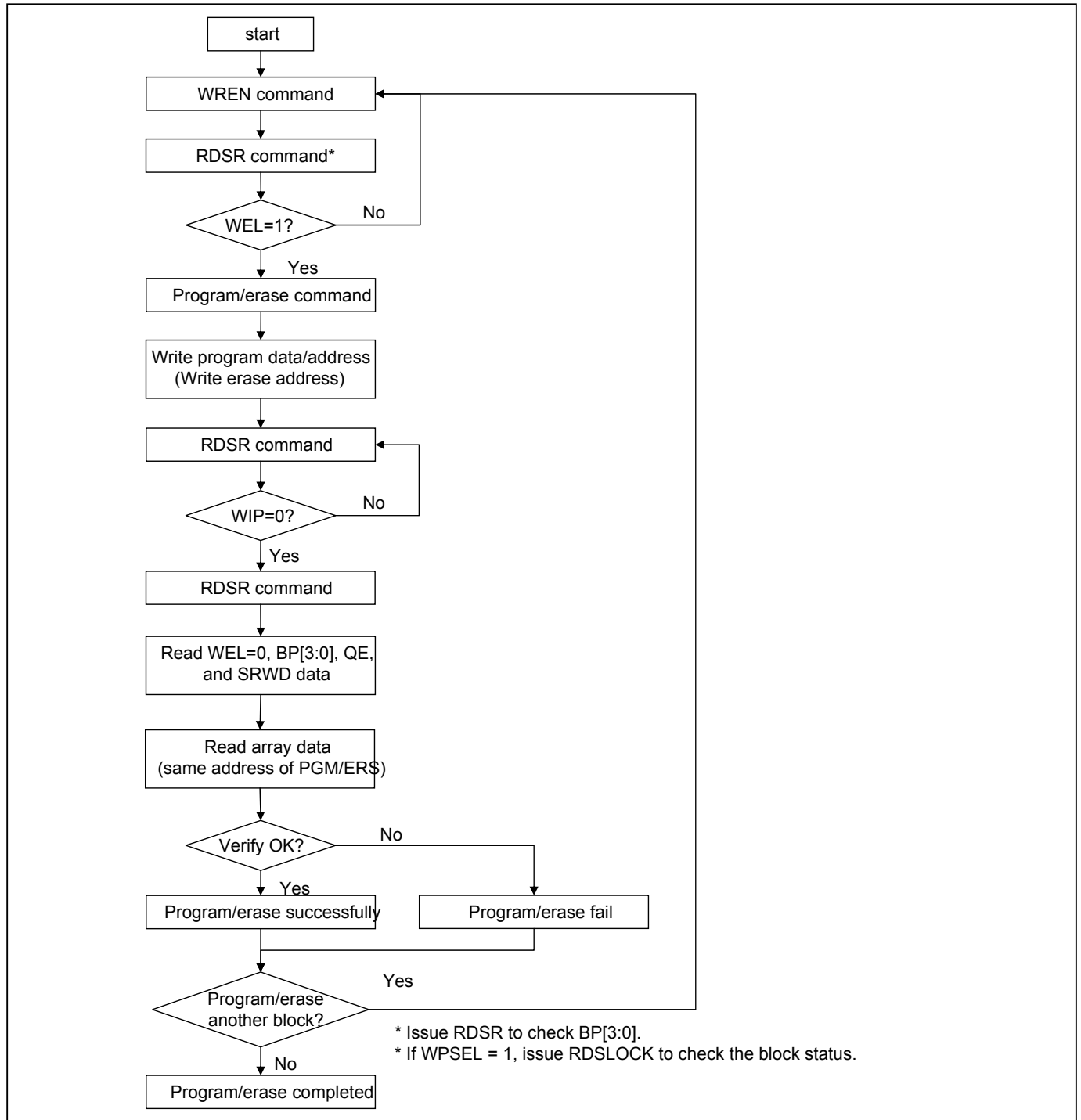


Figure 6. Program/ Erase flow without read array data (read P_FAIL/E_FAIL flag)

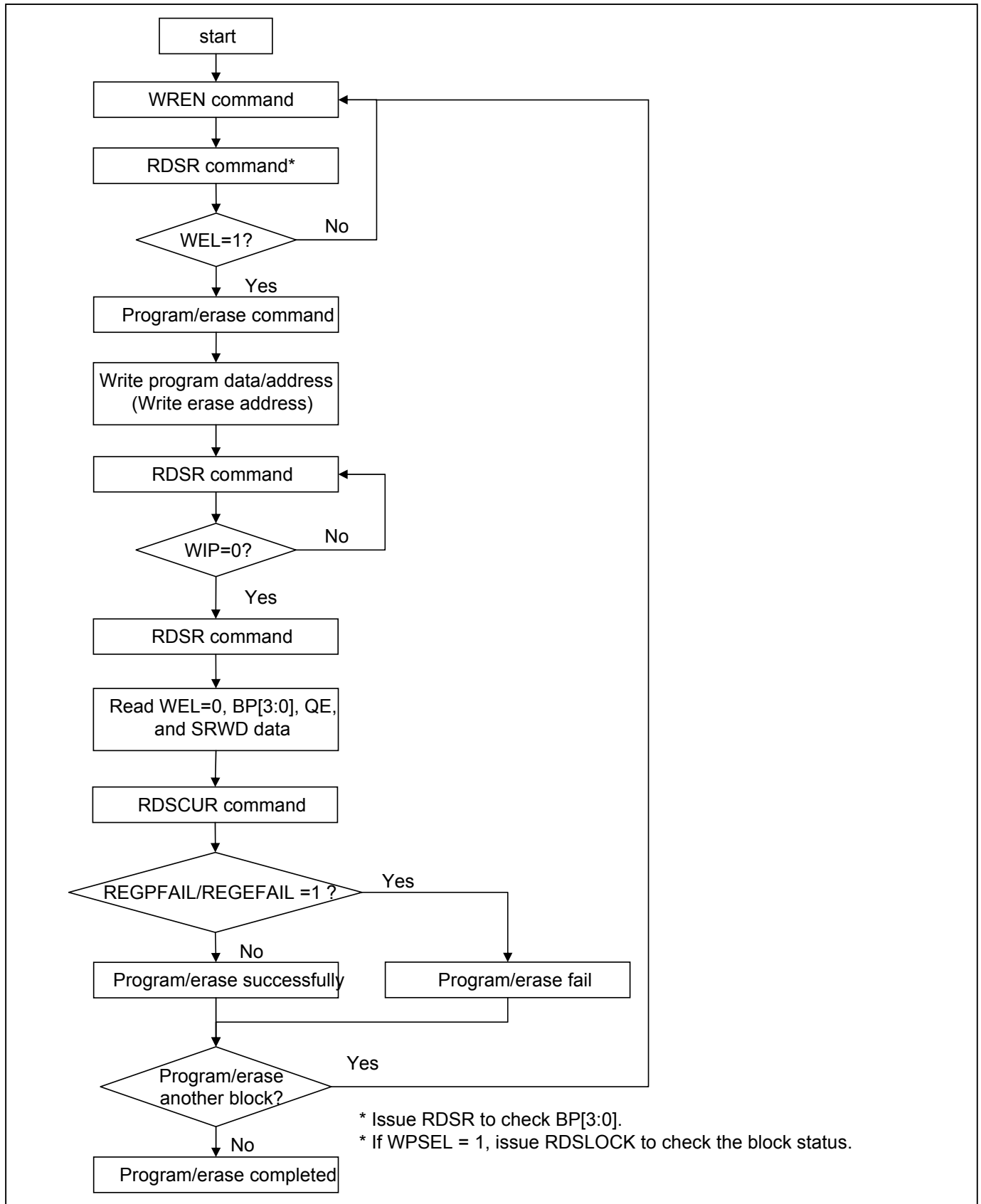
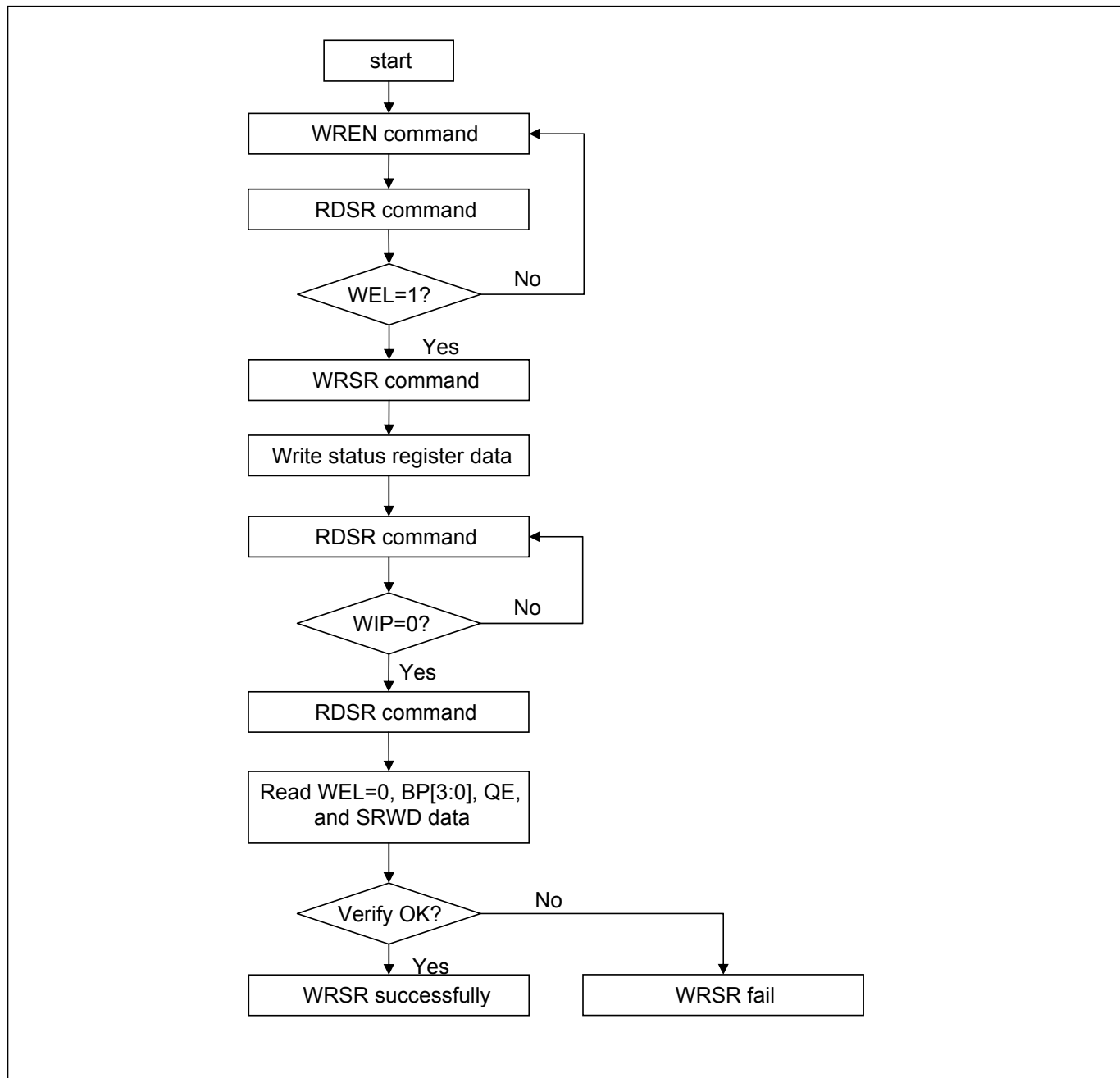


Figure 7. WRSR flow



The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in "[Table 2. Protected Area Sizes](#)") of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is unprotected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, performs SPI Quad modes when it is reset to "0" (factory default) to enable WP# or is set to "1" to enable Quad SIO2 and SIO3. QE bit is only valid for SPI mode. When operate in SPI mode, and quad IO read is desired (for command EBh/E7h, or quad IO program, 38h). WRSR command has to be set the through Status Register bit 6, the QE bit. Then the SPI Quad I/O commands (EBh/E7h/38h) will be accepted by flash. If QE bit is not set, SPI Quad I/O commands (EBh/E7h/38h) will be invalid commands, the device will not respond to them. Once QE bit is set, all SPI commands are valid. 1I/O commands and 2I/O commands can be issued no matter QE bit is "0" or "1". When in QPI mode, QE bit will not affect the operation of QPI mode at all. Therefore either "0" or "1" value of QE bit does not affect the QPI mode operation.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the "[Table 2. Protected Area Sizes](#)"

9-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in "Table 2. Protected Area Sizes"). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high. (Please refer to "Figure 26. Write Status Register (WRSR) Sequence (Command 01) (SPI Mode)" and "Figure 28. Write Status Register (WRSR) Sequence (Command 01) (QPI Mode)")

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 7. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in "Table 2. Protected Area Sizes".

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

If the system enter QPI or set QE=1, the feature of HPM will be disabled.

9-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out. (Please refer to "[Figure 27. Read Data Bytes \(READ\) Sequence \(Command 03\) \(SPI Mode only\) \(33MHz\)](#)")

9-7. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Read on SPI Mode The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to "[Figure 29. Read at Higher Speed \(FAST_READ\) Sequence \(Command 0B\) \(SPI Mode\) \(104MHz\)](#)")

Read on QPI Mode The sequence of issuing FAST_READ instruction in QPI mode is: CS# goes low→ sending FAST_READ instruction, 2 cycles→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QPI FAST_READ operation can use CS# to high at any time during data out. (Please refer to "[Figure 30. Read at Higher Speed \(FAST_READ\) Sequence \(Command 0B\) \(QPI Mode\) \(84MHz\)](#)")

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-8. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4 dummy cycles on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (Please refer to ["Figure 31. 2 x I/O Read Mode Sequence \(Command BB\) \(SPI Mode only\) \(84MHz\)"](#)).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-9. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out. (Please refer to ["Figure 32. 4 x I/O Read Mode Sequence \(Command EB\) \(SPI Mode\) \(104MHz\)"](#)).

W4READ instruction (E7) is also available is SPI mode for 4 I/O read. The sequence is similar to 4READ, but with only 4 dummy cycles. The clock rate runs at 84MHz.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

Another sequence of issuing 4 READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still CS# goes high → CS# goes low (reduce 4 Read instruction) →24-bit random access address (Please refer to ["Figure 33. 4 x I/O Read enhance performance Mode Sequence \(Command EB\) \(SPI Mode\) \(104MHz\)"](#) and ["Figure 35. 4 x I/O Read enhance performance Mode Sequence \(Command EB\) \(QPI Mode\) \(104MHz\)"](#)).

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-10. Burst Read

This device supports Burst Read in both SPI and QPI mode.

To set the Burst length, following command operation is required

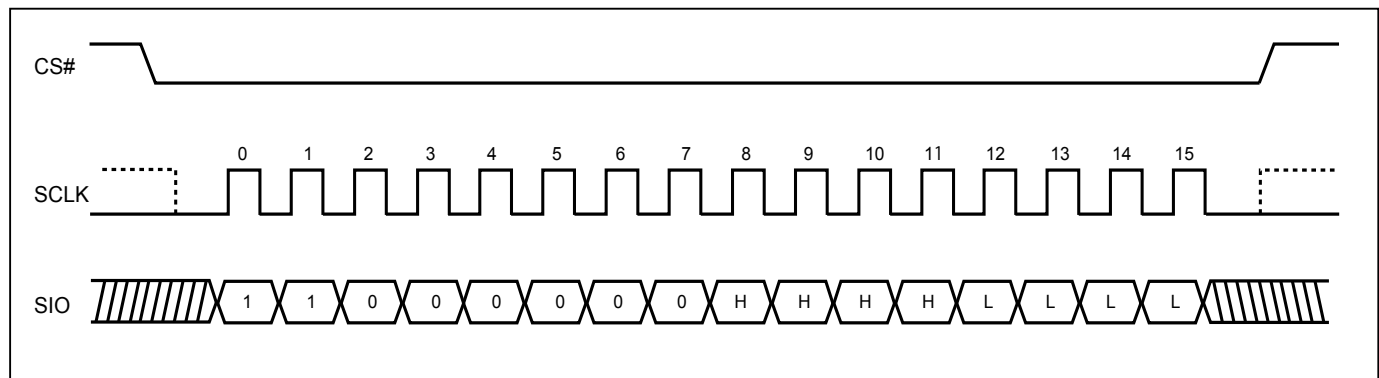
Issuing command: "C0h" in the first Byte (8-clocks), following 4 clocks defining wrap around enable with "0h" and disable with "1h".

Next 4 clocks is to define wrap around depth. Definition as following table:

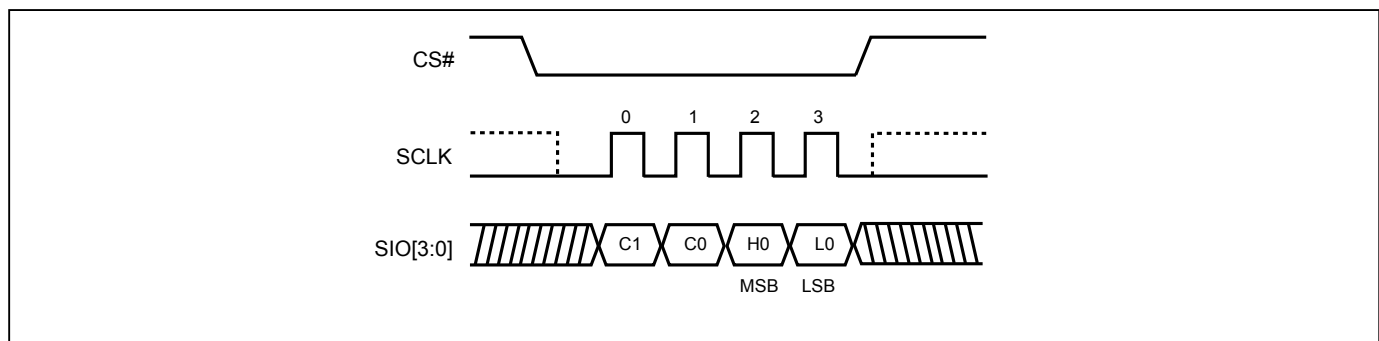
Data	Wrap Around	Wrap Depth	Data	Wrap Around	Wrap Depth
1xh	No	X	00h	Yes	8-byte
1xh	No	X	01h	Yes	16-byte
1xh	No	X	02h	Yes	32-byte
1xh	No	X	03h	Yes	64-byte

The wrap around unit is defined within the 256Byte page, with random initial address. It's defined as "wrap-around mode disable" for the default state of the device. To exit wrap around, it is required to issue another "C0" command in which data='1xh'. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is required to issue another "C0" command in which data="0xh". QPI "0Bh" "EBh" and SPI "EBh" "E7h" support wrap around feature after wrap around enable. Burst read is supported in both SPI and QPI mode. The device id default without Burst read.

SPI Mode



QPI Mode



Note: MSB=Most Significant Bit
LSB=Least Significant Bit