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MX29GL256E DATASHEET

The MX29GL256E product family is not recommended for new designs, while MX29GL256F family is suggested to replace it. Please refer to MX29GL256F datasheet for specifications and ordering information, or contact your local sales representative for additional support.

SINGLE VOLTAGE 3V ONLY FLASH MEMORY

The MX29GL256E product family is not recommended for new designs, while MX29GL256F family is suggested to replace it. Please refer to MX29GL256F datasheet for specifications and ordering information, or contact your local sales representative for additional support.

FEATURES

GENERAL FEATURES

- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
  - MX29GL256E H/L: VI/O=VCC=2.7V~3.6V, VI/O voltage must tight with VCC
  - MX29GL256E U/D: VI/O=1.65V~3.6V for Input/Output
- Byte/Word mode switchable
  - 33,554,432 x 8 / 16,777,216 x 16
- 64KW/128KB uniform sector architecture
  - 256 equal sectors
- 16-byte/8-word page read buffer
- 64-byte/32-word write buffer
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced sector protection function (Solid and Password Protect)
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode

PERFORMANCE

- High Performance
  - Fast access time:
    - MX29GL256E H/L: 100ns (VCC=2.7~3.6V), 90ns (VCC=3.0~3.6V)
    - MX29GL256E U/D: 110ns (VCC=2.7~3.6V, V I/O=1.65 to Vcc)
  - Page access time:
    - MX29GL256E H/L: 25ns
    - MX29GL256E U/D: 30ns
  - Fast program time: 10us/word
  - Fast erase time: 0.5s/sector
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 20uA (typical)
- Typical 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

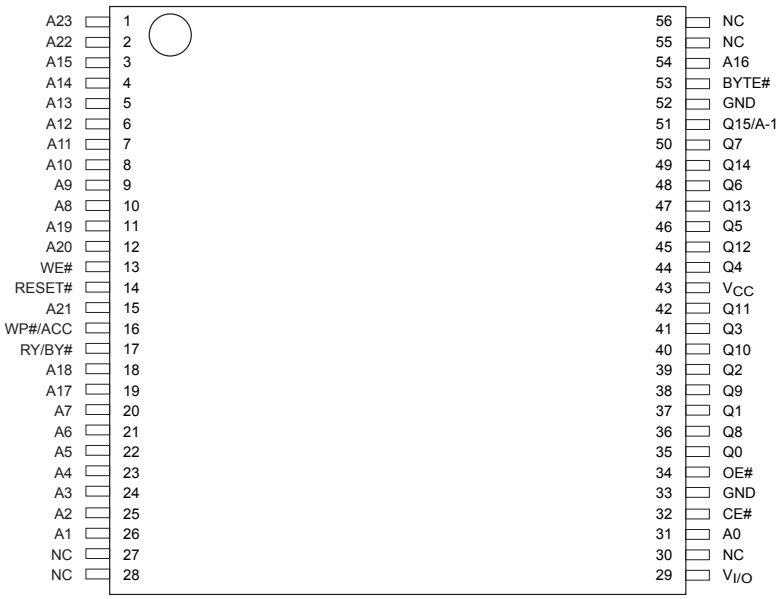
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability

PACKAGE

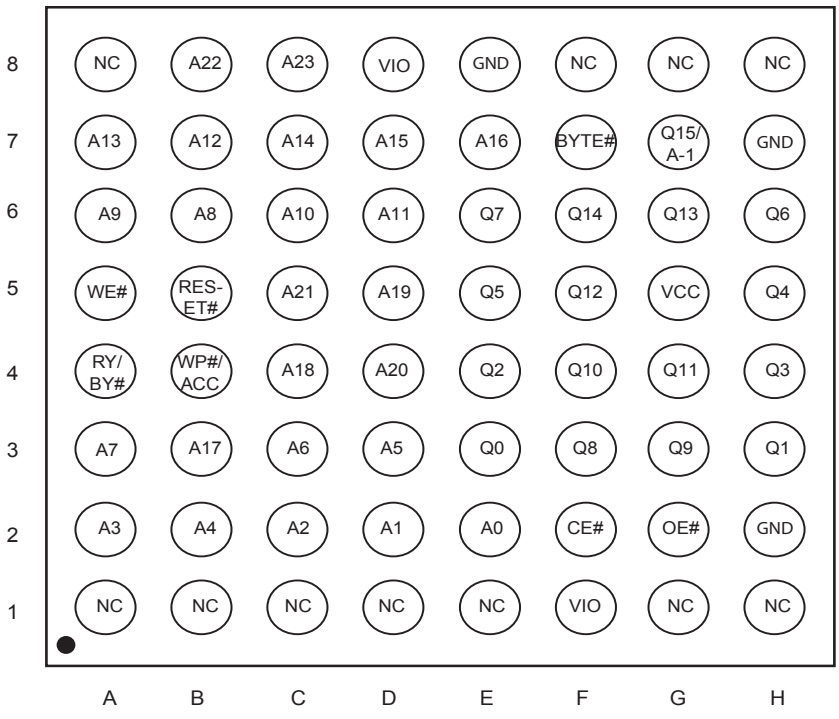
- 56-Pin TSOP
- 64-Ball FBGA (10mm x 13mm)
- 64-Ball LFBGA (11mm x 13mm)
- 70-Pin SSOP
- **All devices are RoHS Compliant and Halogen-free**

PIN CONFIGURATION

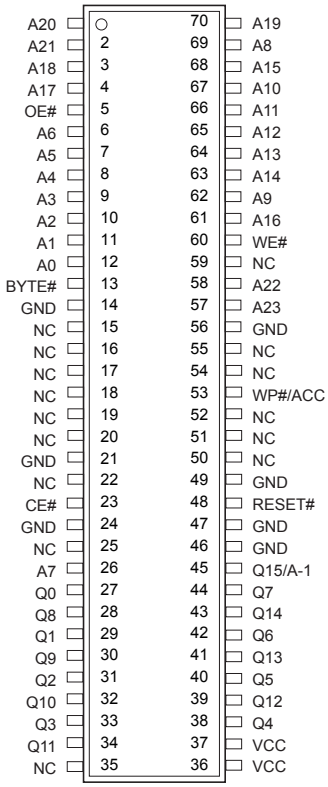
56 TSOP



64 FBGA/64 LFBGA



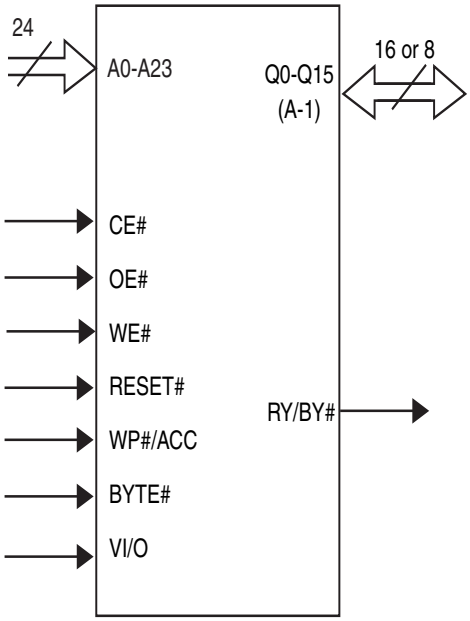
70 SSOP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A23	Address Input
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC*	Hardware Write Protect/Programming Acceleration input
RY/BY#	Ready/Busy Output
BYTE#	Selects 8 bits or 16 bits mode
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally
VI/O	Power Supply for Input/Output

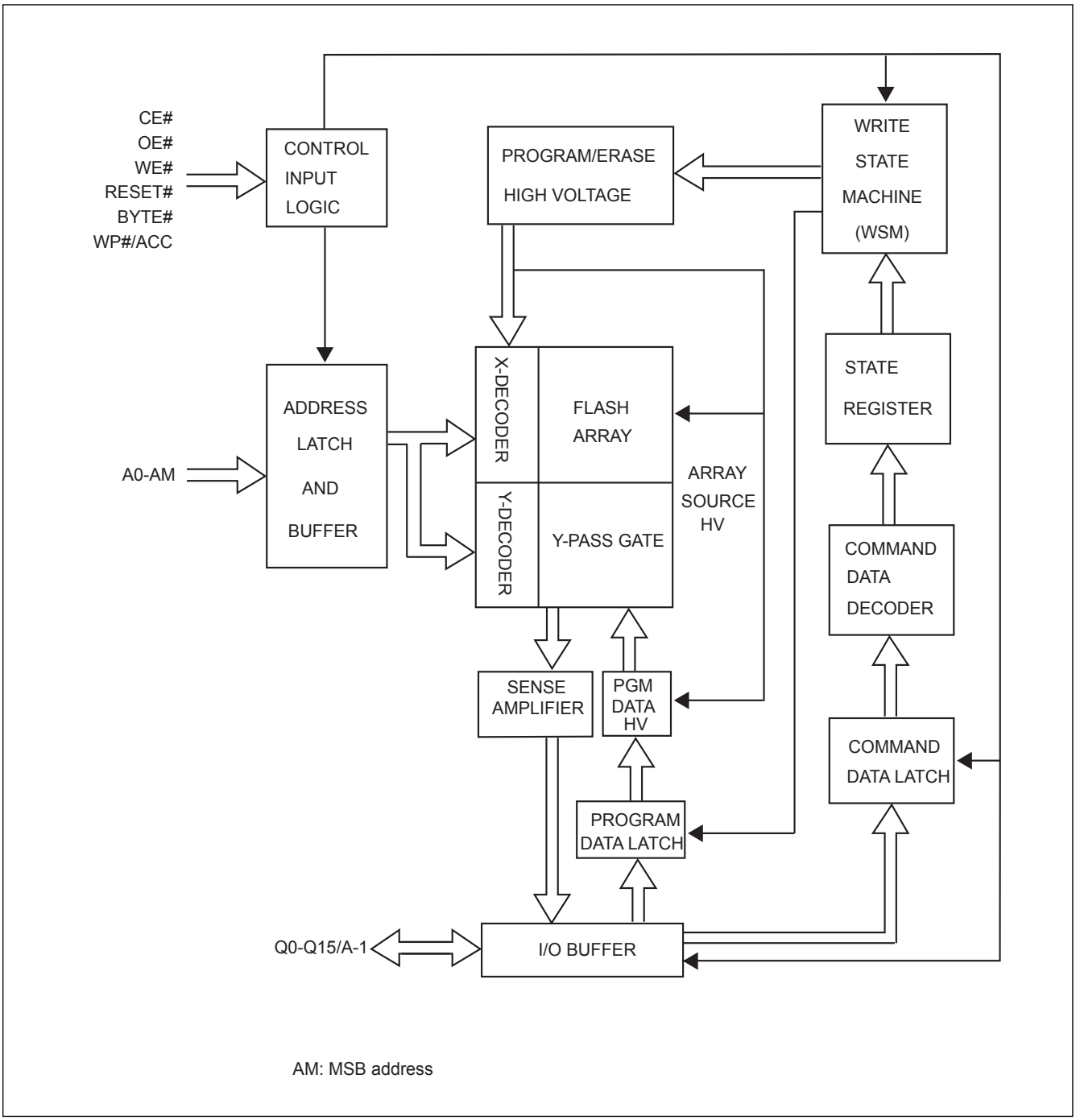
LOGIC SYMBOL



Notes:

1. WP#/ACC has internal pull up.
2. For MX29GL256E H/L VI/O voltage must tight with VCC.
   VI/O = VCC =2.7V~3.6V.

BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

The *block diagram* on Page 5 illustrates a simplified architecture of this device. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(A23). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

ARRAY ARCHITECTURE

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in *Table 1*.

BLOCK STRUCTURE

Table 1. MX29GL256E SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address	(x16)
Kbytes	Kwords		A23-A16	Address Range
128	64	SA0	00000000	000000h-00FFFFh
128	64	SA1	00000001	010000h-01FFFFh
128	64	SA2	00000010	020000h-02FFFFh
128	64	SA3	00000011	030000h-03FFFFh
128	64	SA4	00000100	040000h-04FFFFh
128	64	SA5	00000101	050000h-05FFFFh
128	64	SA6	00000110	060000h-06FFFFh
128	64	SA7	00000111	070000h-07FFFFh
128	64	SA8	00001000	080000h-08FFFFh
128	64	SA9	00001001	090000h-09FFFFh
128	64	SA10	00001010	0A0000h-0AFFFFh
128	64	SA11	00001011	0B0000h-0BFFFFh
128	64	SA12	00001100	0C0000h-0CFFFFh
128	64	SA13	00001101	0D0000h-0DFFFFh
128	64	SA14	00001110	0E0000h-0EFFFFh
128	64	SA15	00001111	0F0000h-0FFFFFh
128	64	SA16	00010000	100000h-10FFFFh
128	64	SA17	00010001	110000h-11FFFFh
128	64	SA18	00010010	120000h-12FFFFh
128	64	SA19	00010011	130000h-13FFFFh
128	64	SA20	00010100	140000h-14FFFFh
128	64	SA21	00010101	150000h-15FFFFh
128	64	SA22	00010110	160000h-16FFFFh
128	64	SA23	00010111	170000h-17FFFFh
128	64	SA24	00011000	180000h-18FFFFh
128	64	SA25	00011001	190000h-19FFFFh
128	64	SA26	00011010	1A0000h-1AFFFFh
128	64	SA27	00011011	1B0000h-1BFFFFh
128	64	SA28	00011100	1C0000h-1CFFFFh
128	64	SA29	00011101	1D0000h-1DFFFFh
128	64	SA30	00011110	1E0000h-1EFFFFh
128	64	SA31	00011111	1F0000h-1FFFFFh
128	64	SA32	00100000	200000h-20FFFFh
128	64	SA33	00100001	210000h-21FFFFh
128	64	SA34	00100010	220000h-22FFFFh
128	64	SA35	00100011	230000h-23FFFFh
128	64	SA36	00100100	240000h-24FFFFh
128	64	SA37	00100101	250000h-25FFFFh
128	64	SA38	00100110	260000h-26FFFFh
128	64	SA39	00100111	270000h-27FFFFh

Sector Size		Sector	Sector Address A23-A16	(x16) Address Range
Kbytes	Kwords			
128	64	SA40	00101000	280000h-28FFFFh
128	64	SA41	00101001	290000h-29FFFFh
128	64	SA42	00101010	2A0000h-2AFFFFh
128	64	SA43	00101011	2B0000h-2BFFFFh
128	64	SA44	00101100	2C0000h-2CFFFFh
128	64	SA45	00101101	2D0000h-2DFFFFh
128	64	SA46	00101110	2E0000h-2EFFFFh
128	64	SA47	00101111	2F0000h-2FFFFFh
128	64	SA48	00110000	300000h-30FFFFh
128	64	SA49	00110001	310000h-31FFFFh
128	64	SA50	00110010	320000h-32FFFFh
128	64	SA51	00110011	330000h-33FFFFh
128	64	SA52	00110100	340000h-34FFFFh
128	64	SA53	00110101	350000h-35FFFFh
128	64	SA54	00110110	360000h-36FFFFh
128	64	SA55	00110111	370000h-37FFFFh
128	64	SA56	00111000	380000h-38FFFFh
128	64	SA57	00111001	390000h-39FFFFh
128	64	SA58	00111010	3A0000h-3AFFFFh
128	64	SA59	00111011	3B0000h-3BFFFFh
128	64	SA60	00111100	3C0000h-3CFFFFh
128	64	SA61	00111101	3D0000h-3DFFFFh
128	64	SA62	00111110	3E0000h-3EFFFFh
128	64	SA63	00111111	3F0000h-3FFFFFh
128	64	SA64	01000000	400000h-40FFFFh
128	64	SA65	01000001	410000h-41FFFFh
128	64	SA66	01000010	420000h-42FFFFh
128	64	SA67	01000011	430000h-43FFFFh
128	64	SA68	01000100	440000h-44FFFFh
128	64	SA69	01000101	450000h-45FFFFh
128	64	SA70	01000110	460000h-46FFFFh
128	64	SA71	01000111	470000h-47FFFFh
128	64	SA72	01001000	480000h-48FFFFh
128	64	SA73	01001001	490000h-49FFFFh
128	64	SA74	01001010	4A0000h-4AFFFFh
128	64	SA75	01001011	4B0000h-4BFFFFh
128	64	SA76	01001100	4C0000h-4CFFFFh
128	64	SA77	01001101	4D0000h-4DFFFFh
128	64	SA78	01001110	4E0000h-4EFFFFh
128	64	SA79	01001111	4F0000h-4FFFFFh
128	64	SA80	01010000	500000h-50FFFFh
128	64	SA81	01010001	510000h-51FFFFh

Sector Size		Sector	Sector Address A23-A16	(x16) Address Range
Kbytes	Kwords			
128	64	SA82	01010010	520000h-52FFFFh
128	64	SA83	01010011	530000h-53FFFFh
128	64	SA84	01010100	540000h-54FFFFh
128	64	SA85	01010101	550000h-55FFFFh
128	64	SA86	01010110	560000h-56FFFFh
128	64	SA87	01010111	570000h-57FFFFh
128	64	SA88	01011000	580000h-58FFFFh
128	64	SA89	01011001	590000h-59FFFFh
128	64	SA90	01011010	5A0000h-5AFFFFh
128	64	SA91	01011011	5B0000h-5BFFFFh
128	64	SA92	01011100	5C0000h-5CFFFFh
128	64	SA93	01011101	5D0000h-5DFFFFh
128	64	SA94	01011110	5E0000h-5EFFFFh
128	64	SA95	01011111	5F0000h-5FFFFFh
128	64	SA96	01100000	600000h-60FFFFh
128	64	SA97	01100001	610000h-61FFFFh
128	64	SA98	01100010	620000h-62FFFFh
128	64	SA99	01100011	630000h-63FFFFh
128	64	SA100	01100100	640000h-64FFFFh
128	64	SA101	01100101	650000h-65FFFFh
128	64	SA102	01100110	660000h-66FFFFh
128	64	SA103	01100111	670000h-67FFFFh
128	64	SA104	01101000	680000h-68FFFFh
128	64	SA105	01101001	690000h-69FFFFh
128	64	SA106	01101010	6A0000h-6AFFFFh
128	64	SA107	01101011	6B0000h-6BFFFFh
128	64	SA108	01101100	6C0000h-6CFFFFh
128	64	SA109	01101101	6D0000h-6DFFFFh
128	64	SA110	01101110	6E0000h-6EFFFFh
128	64	SA111	01101111	6F0000h-6FFFFFh
128	64	SA112	01110000	700000h-70FFFFh
128	64	SA113	01110001	710000h-71FFFFh
128	64	SA114	01110010	720000h-72FFFFh
128	64	SA115	01110011	730000h-73FFFFh
128	64	SA116	01110100	740000h-74FFFFh
128	64	SA117	01110101	750000h-75FFFFh
128	64	SA118	01110110	760000h-76FFFFh
128	64	SA119	01110111	770000h-77FFFFh
128	64	SA120	01111000	780000h-78FFFFh
128	64	SA121	01111001	790000h-79FFFFh
128	64	SA122	01111010	7A0000h-7AFFFFh
128	64	SA123	01111011	7B0000h-7BFFFFh

Sector Size		Sector	Sector Address A23-A16	(x16) Address Range
Kbytes	Kwords			
128	64	SA124	01111100	7C0000h-7CFFFFh
128	64	SA125	01111101	7D0000h-7DFFFFh
128	64	SA126	01111110	7E0000h-7EFFFFh
128	64	SA127	01111111	7F0000h-7FFFFFh
128	64	SA128	10000000	800000h-80FFFFh
128	64	SA129	10000001	810000h-81FFFFh
128	64	SA130	10000010	820000h-82FFFFh
128	64	SA131	10000011	830000h-83FFFFh
128	64	SA132	10000100	840000h-84FFFFh
128	64	SA133	10000101	850000h-85FFFFh
128	64	SA134	10000110	860000h-86FFFFh
128	64	SA135	10000111	870000h-87FFFFh
128	64	SA136	10001000	880000h-88FFFFh
128	64	SA137	10001001	890000h-89FFFFh
128	64	SA138	10001010	8A0000h-8AFFFFh
128	64	SA139	10001011	8B0000h-8BFFFFh
128	64	SA140	10001100	8C0000h-8CFFFFh
128	64	SA141	10001101	8D0000h-8DFFFFh
128	64	SA142	10001110	8E0000h-8EFFFFh
128	64	SA143	10001111	8F0000h-8FFFFFh
128	64	SA144	10010000	900000h-90FFFFh
128	64	SA145	10010001	910000h-91FFFFh
128	64	SA146	10010010	920000h-92FFFFh
128	64	SA147	10010011	930000h-93FFFFh
128	64	SA148	10010100	940000h-94FFFFh
128	64	SA149	10010101	950000h-95FFFFh
128	64	SA150	10010110	960000h-96FFFFh
128	64	SA151	10010111	970000h-97FFFFh
128	64	SA152	10011000	980000h-98FFFFh
128	64	SA153	10011001	990000h-99FFFFh
128	64	SA154	10011010	9A0000h-9AFFFFh
128	64	SA155	10011011	9B0000h-9BFFFFh
128	64	SA156	10011100	9C0000h-9CFFFFh
128	64	SA157	10011101	9D0000h-9DFFFFh
128	64	SA158	10011110	9E0000h-9EFFFFh
128	64	SA159	10011111	9F0000h-9FFFFFh
128	64	SA160	10100000	A00000h-A0FFFFh
128	64	SA161	10100001	A10000h-A1FFFFh
128	64	SA162	10100010	A20000h-A2FFFFh
128	64	SA163	10100011	A30000h-A3FFFFh
128	64	SA164	10100100	A40000h-A4FFFFh
128	64	SA165	10100101	A50000h-A5FFFFh

Sector Size		Sector	Sector Address A23-A16	(x16) Address Range
Kbytes	Kwords			
128	64	SA166	10100110	A60000h-A6FFFFh
128	64	SA167	10100111	A70000h-A7FFFFh
128	64	SA168	10101000	A80000h-A8FFFFh
128	64	SA169	10101001	A90000h-A9FFFFh
128	64	SA170	10101010	AA0000h-AAFFFFh
128	64	SA171	10101011	AB0000h-ABFFFFh
128	64	SA172	10101100	AC0000h-ACFFFFh
128	64	SA173	10101101	AD0000h-ADFFFFh
128	64	SA174	10101110	AE0000h-AEFFFFh
128	64	SA175	10101111	AF0000h-AFFFFFh
128	64	SA176	10110000	B00000h-B0FFFFh
128	64	SA177	10110001	B10000h-B1FFFFh
128	64	SA178	10110010	B20000h-B2FFFFh
128	64	SA179	10110011	B30000h-B3FFFFh
128	64	SA180	10110100	B40000h-B4FFFFh
128	64	SA181	10110101	B50000h-B5FFFFh
128	64	SA182	10110110	B60000h-B6FFFFh
128	64	SA183	10110111	B70000h-B7FFFFh
128	64	SA184	10111000	B80000h-B8FFFFh
128	64	SA185	10111001	B90000h-B9FFFFh
128	64	SA186	10111010	BA0000h-BAFFFFh
128	64	SA187	10111011	BB0000h-BBFFFFh
128	64	SA188	10111100	BC0000h-BCFFFFh
128	64	SA189	10111101	BD0000h-BDFFFFh
128	64	SA190	10111110	BE0000h-BEFFFFh
128	64	SA191	10111111	BF0000h-BFFFFFh
128	64	SA192	11000000	C00000h-C0FFFFh
128	64	SA193	11000001	C10000h-C1FFFFh
128	64	SA194	11000010	C20000h-C2FFFFh
128	64	SA195	11000011	C30000h-C3FFFFh
128	64	SA196	11000100	C40000h-C4FFFFh
128	64	SA197	11000101	C50000h-C5FFFFh
128	64	SA198	11000110	C60000h-C6FFFFh
128	64	SA199	11000111	C70000h-C7FFFFh
128	64	SA200	11001000	C80000h-C8FFFFh
128	64	SA201	11001001	C90000h-C9FFFFh
128	64	SA202	11001010	CA0000h-CAFFFFh
128	64	SA203	11001011	CB0000h-CBFFFFh
128	64	SA204	11001100	CC0000h-CCFFFFh
128	64	SA205	11001101	CD0000h-CDFFFFh
128	64	SA206	11001110	CE0000h-CEFFFFh
128	64	SA207	11001111	CF0000h-CFFFFFh

Sector Size		Sector	Sector Address A23-A16	(x16) Address Range
Kbytes	Kwords			
128	64	SA208	11010000	D00000h-D0FFFFh
128	64	SA209	11010001	D10000h-D1FFFFh
128	64	SA210	11010010	D20000h-D2FFFFh
128	64	SA211	11010011	D30000h-D3FFFFh
128	64	SA212	11010100	D40000h-D4FFFFh
128	64	SA213	11010101	D50000h-D5FFFFh
128	64	SA214	11010110	D60000h-D6FFFFh
128	64	SA215	11010111	D70000h-D7FFFFh
128	64	SA216	11011000	D80000h-D8FFFFh
128	64	SA217	11011001	D90000h-D9FFFFh
128	64	SA218	11011010	DA0000h-DAFFFFh
128	64	SA219	11011011	DB0000h-DBFFFFh
128	64	SA220	11011100	DC0000h-DCFFFFh
128	64	SA221	11011101	DD0000h-DDFFFFh
128	64	SA222	11011110	DE0000h-DEFFFFh
128	64	SA223	11011111	DF0000h-DFFFFFh
128	64	SA224	11100000	E00000h-E0FFFFh
128	64	SA225	11100001	E10000h-E1FFFFh
128	64	SA226	11100010	E20000h-E2FFFFh
128	64	SA227	11100011	E30000h-E3FFFFh
128	64	SA228	11100100	E40000h-E4FFFFh
128	64	SA229	11100101	E50000h-E5FFFFh
128	64	SA230	11100110	E60000h-E6FFFFh
128	64	SA231	11100111	E70000h-E7FFFFh
128	64	SA232	11101000	E80000h-E8FFFFh
128	64	SA233	11101001	E90000h-E9FFFFh
128	64	SA234	11101010	EA0000h-EAFFFFh
128	64	SA235	11101011	EB0000h-EBFFFFh
128	64	SA236	11101100	EC0000h-ECFFFFh
128	64	SA237	11101101	ED0000h-EDFFFFh
128	64	SA238	11101110	EE0000h-EEFFFFh
128	64	SA239	11101111	EF0000h-EFFFFFh
128	64	SA240	11110000	F00000h-F0FFFFh
128	64	SA241	11110001	F10000h-F1FFFFh
128	64	SA242	11110010	F20000h-F2FFFFh
128	64	SA243	11110011	F30000h-F3FFFFh
128	64	SA244	11110100	F40000h-F4FFFFh
128	64	SA245	11110101	F50000h-F5FFFFh
128	64	SA246	11110110	F60000h-F6FFFFh
128	64	SA247	11110111	F70000h-F7FFFFh
128	64	SA248	11111000	F80000h-F8FFFFh
128	64	SA249	11111001	F90000h-F9FFFFh

Sector Size		Sector	Sector Address A23-A16	(x16) Address Range
Kbytes	Kwords			
128	64	SA250	11111010	FA0000h-FAFFFFh
128	64	SA251	11111011	FB0000h-FBFFFFh
128	64	SA252	11111100	FC0000h-FCFFFFh
128	64	SA253	11111101	FD0000h-FDFFFFh
128	64	SA254	11111110	FE0000h-FEFFFFh
128	64	SA255	11111111	FF0000h-FFFFFFh

BUS OPERATION

Table 2-1. BUS OPERATION

Mode Select	RE-SET#	CE#	WE#	OE#	Address (Note4)	Data I/O Q7~Q0	Byte# Vil Data (I/O) Q15~Q8	Byte# Vih Data (I/O) Q15~Q8	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ	L/H
Standby Mode	Vcc ± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ	H
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ, Q15=A-1	DOUT	L/H
Write	H	L	L	H	AIN	DIN		DIN	Note1,2
Accelerate Program	H	L	L	H	AIN	DIN		DIN	Vhv

Notes:
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.

Table 2-2. BUS OPERATION

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q7 ~ Q0	Q15 ~ Q8
	CE#	WE#	OE#											
Sector Lock Status Verification	L	H	L	SA	X	V_{hv}	X	L	X	L	H	L	01h or 00h (Note 1)	X
Read Silicon ID Manufacturer Code	L	H	L	X	X	V_{hv}	X	L	X	L	L	L	C2H	X
Read Silicon ID -- MX29GL256E														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H(Word), XXH(Byte)
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	22H	22H(Word), XXH(Byte)
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	01H	22H(Word), XXH(Byte)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects high address sector: 99h.
   WP# protects low address sector: 89h
   Factory unlocked code: WP# protects high address sector: 19h.
   WP# protects low address sector: 09h
3. AM: MSB of address.

FUNCTIONAL OPERATION DESCRIPTION

READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

PAGE READ

This device is able to conduct MXIC MaskROM compatible high performance page read. Page size is 16 bytes or 8 words. The higher address Amax ~ A3 select the certain page, while A2~A0 for word mode, A2~A-1 for byte mode select the particular word or byte in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in *Figure 4*. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Byte or Word Data (I/O) pins will drive data.

BYTE/WORD SELECTION

The BYTE# input pin is used to select the organization of the array data and how the data is input/output on the Data (I/O) pins. If the BYTE# pin is held HIGH, Word mode will be selected and all 16 data lines (Q0 to Q15) will be active.

If BYTE# is forced LOW, Byte mode will be active and only data lines Q0 to Q7 will be active. Data lines Q8 to Q14 will remain in a high impedance state and Q15 becomes the A-1 address input pin.

HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

WRITE BUFFER PROGRAMMING OPERATION

Programs 64bytes/32words in a programming operation. To trigger the Write Buffer Programming, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined programming Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax-A5.

"Write-Buffer-Page" address has to be the same for all address/ data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it'll return to normal READ mode.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

WRITE BUFFER PROGRAMMING OPERATION (cont'd)

ABORT will be executed for the Write Buffer Programming Sequence if following condition occurs:
- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle.
A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

SECTOR PROTECT OPERATION

The device provides user programmable protection operations for selected sectors. Please refer to *Table 1* which show all Sector assignments.

During the protection operation, the sector address of any sector may be used to specify the Sector being protected.

AUTOMATIC SELECT BUS OPERATIONS

The following five bus operations require A9 to be raised to Vhv. Please see AUTOMATIC SELECT COMMAND SEQUENCE in the COMMAND OPERATIONS section for details of equivalent command operations that do not require the use of Vhv.

SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins A23 to A12, address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q7 to Q0.

READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 99h(H)/89h(L) will be present on data bits Q7 to Q0. Otherwise, the factory unlocked code of 19h(H)/09h(L) will be present.

INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

COMMAND OPERATIONS

READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to *READ OPERATION* in the *BUS OPERATIONS* section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding 20us) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector (s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct *cycle* defined in the *Table 3* (including 2 unlock cycles and the A0H program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

COMMAND OPERATIONS (cont'd)

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY (cont'd)

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

Status	Q7*1	Q6*1	Q5	Q1	RY/BY# (Note)
In progress	Q7#	Toggling	0	0	0
Exceed time limit	Q7#	Toggling	1	N/A	0

Note: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in Section *Advanced Sector Protection/Un-protection*.

SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. *Note that the 50us timer-out counter is restarted after every erase command sequence.* If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

COMMAND OPERATIONS (cont'd)

SECTOR ERASE (cont'd)

The system can determine the status of the embedded sector erase operation by the following methods:

Status	Q7	Q6	Q5	Q3*1	Q2	RY/BY#*2
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Exceeded time limit	0	Toggling	1	1	Toggling	0

Notes:
1. The Q3 status bit is the 50us time-out indicator. When Q3=0, the 50us time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the 50us time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.
2. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector (s), the erase operation will abort thus preventing any data changes in the protected sector (s). Q7 will output "0" and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector (s) will remain unchanged.
4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#*1
In progress	0	Toggling	0	Toggling	0
Exceed time limit	0	Toggling	1	Toggling	0

*1: RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.

COMMAND OPERATIONS (cont'd)

ERASE SUSPEND/RESUME

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until 20us time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector (s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle	N/A	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 400us interval between Ease Resume and the next Erase Suspend command.

COMMAND OPERATIONS (cont'd)

PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend is the only valid command that may be issued. The system can determine if the device has entered the Program-Suspended Read mode through Q6 and RY/BY#.

After the device has entered Program-Suspended mode, the system can read any sector (s) except those being programmed by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Program suspend read in program suspended sector	Invalid						1
Program suspend read in non-program suspended sector	Data	Data	Data	Data	Data	Data	1

When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security silicon.

PROGRAM RESUME

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a 5us interval between Program Resume and the next Program Suspend command.

BUFFER WRITE ABORT

Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read status register shown as following table:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Buffer Write Busy	Q7#	Toggle	0	N/A	N/A	0	0
Buffer Write Abort	Q7#	Toggle	0	N/A	N/A	1	0
Buffer Write Exceeded Time Limit	Q7#	Toggle	1	N/A	N/A	0	0