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MX29GL512G / MX68GL1G0G

SINGLE VOLTAGE 3V ONLY FLASH MEMORY

Key Features

- *2.7 to 3.6 volt for read, erase, and program operations*
- *64KW/128KB uniform equal sectors architecture*
- *16 word page read buffer/256 word write buffer*
- *Program/Erase Suspend & Program/Erase Resume*

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SINGLE VOLTAGE 3V ONLY FLASH MEMORY

1. FEATURES

GENERAL FEATURES

- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
    - H/L: VI/O=VCC=2.7V~3.6V, VI/O voltage must tight with VCC
    - U/D: VI/O=1.65V~3.6V for Input/Output
- Byte/Word mode switchable
  - 512Mb: 67,108,864 x 8 / 33,554,432 x 16
  - 1Gb: 134,217,728 x 8 / 67,108,864 x 16
- 64KW/128KB uniform equal sectors architecture
- 32 byte/16 word page read buffer
- 256 word write buffer
- Extra 512 word sector for security
  - Features factory locked and identifiable, and customer lockable
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time:
    - H/L: 100ns
    - U/D: 110ns
  - Page access time:
    - H/L: 15ns
    - U/D: 25ns
  - Word program time: 30us
  - Write Buffer Program Through: 1.8MB/Sec, 2.6MB/Sec with Accelerated Program mode
  - Sector erase time: 0.25sec
- Low Power Consumption
  - Low active read current: 12mA (typ.) at 5MHz
  - Low standby current: 512Mb/1Gb: 20/40uA (typ.)
  - Deep power down current: 3uA(typ.)
- 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Support Common Flash Interface (CFI)
- Advanced sector protection function (Solid and Password Protect)
- Status Register(Data Polling/Toggle), Extended Status Register(volatile bit) and Ready/Busy pin methods to determine device status
- Deep power down mode

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability
- BYTE# input pin
  - Selects 8 bits or 16 bits mode

PACKAGE

- 56-Pin TSOP
- 64-Ball LFBGA (11mm x 13mm)
- **All devices are RoHS Compliant and Halogen-free**

2. PIN CONFIGURATION

56 TSOP

Top View

Signal	Pin	Pin	Signal
A23	1	56	A24
A22	2	55	A25, NC for MX29GL512G
A15	3	54	A16
A14	4	53	BYTE#
A13	5	52	GND
A12	6	51	Q15/A-1
A11	7	50	Q7
A10	8	49	Q14
A9	9	48	Q6
A8	10	47	Q13
A19	11	46	Q5
A20	12	45	Q12
WE#	13	44	Q4
RESET#	14	43	VCC
A21	15	42	Q11
WP#/ACC	16	41	Q3
RY/BY#	17	40	Q10
A18	18	39	Q2
A17	19	38	Q9
A7	20	37	Q1
A6	21	36	Q8
A5	22	35	Q0
A4	23	34	OE#
A3	24	33	GND
A2	25	32	CE#
A1	26	31	A0
NC	27	30	NC
NC	28	29	VI/O

64 LFBGA

Top View

	A	B	C	D	E	F	G	H
8	NC	A22	A23	VI/O	GND	A24	A25*	NC
7	A13	A12	A14	A15	A16	BYTE#	Q15/A-1	GND
6	A9	A8	A10	A11	Q7	Q14	Q13	Q6
5	WE#	RES-ET#	A21	A19	Q5	Q12	VCC	Q4
4	RY/BY#	WP#/ACC	A18	A20	Q2	Q10	Q11	Q3
3	A7	A17	A6	A5	Q0	Q8	Q9	Q1
2	A3	A4	A2	A1	A0	CE#	OE#	GND
1	NC	NC	NC	NC	NC	VI/O	NC	NC

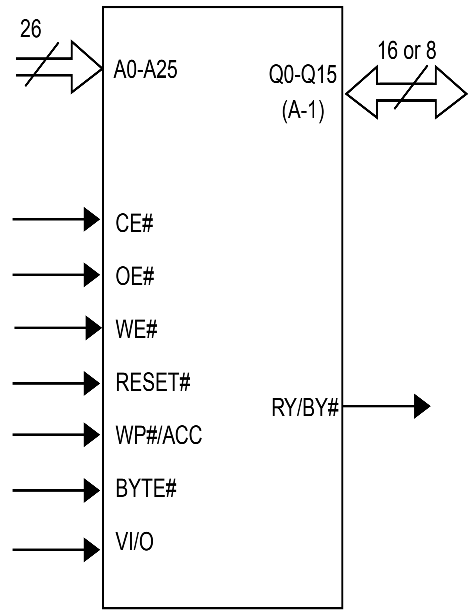
Note: * G8(A25) is NC for MX29GL512G

3. PIN DESCRIPTION

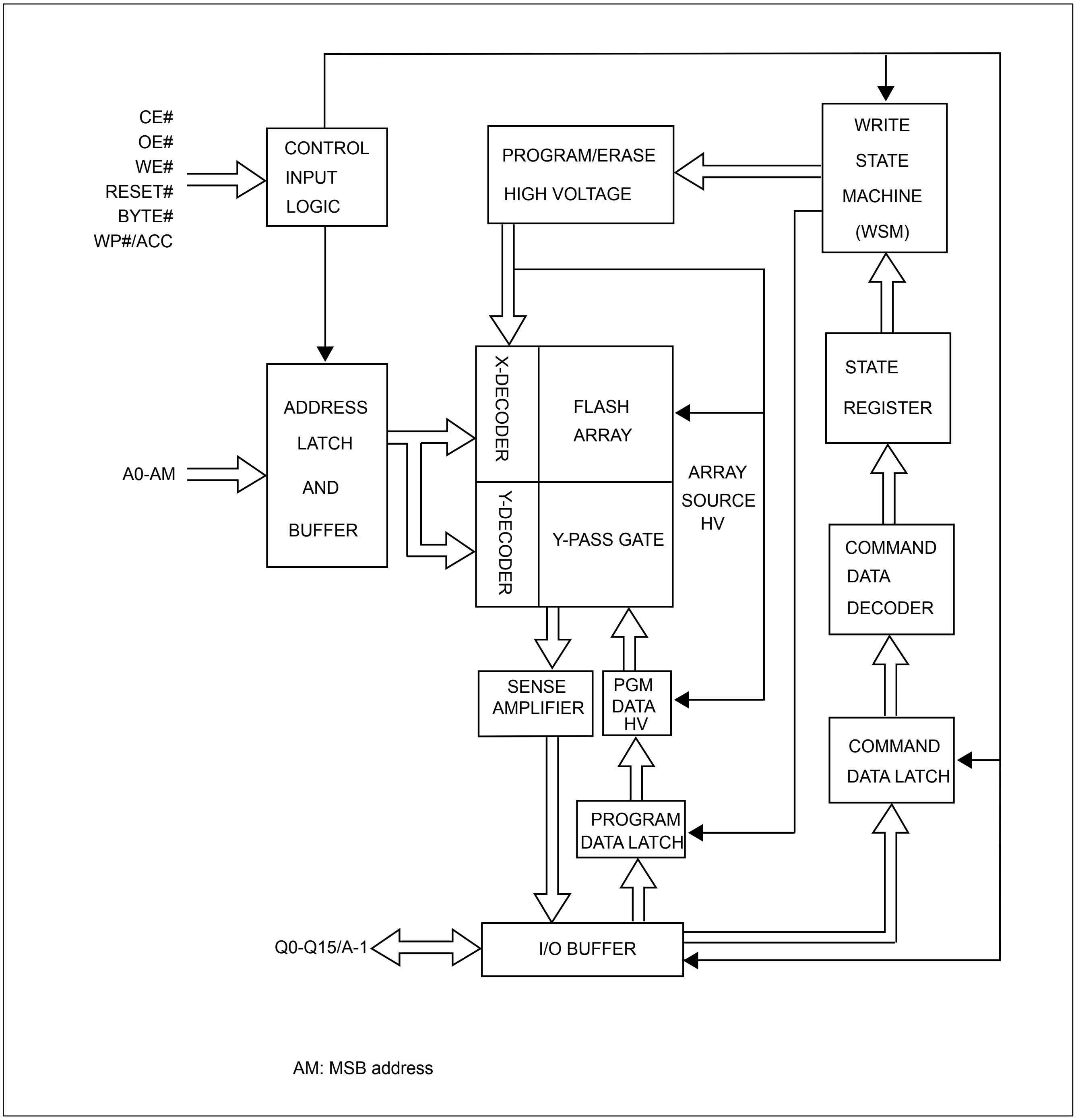
SYMBOL	PIN NAME
A0~A25	Address Input A0~A24 is for MX29GL512G A0~A25 is for MX68GL1G0G
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC *	Hardware Write Protect/Program Acceleration input
RY/BY#	Ready/Busy Output
BYTE# *	Selects 8 bits or 16 bits mode
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally
VI/O	Power Supply for Input/Output

***Note:** WP#/ACC and BYTE# has internal pull up.

LOGIC SYMBOL



4. BLOCK DIAGRAM



5. BLOCK DIAGRAM DESCRIPTION

The "4. BLOCK DIAGRAM" illustrates a simplified architecture of this device. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM (AM=A24 is for MX29GL512G, AM=A25 is for MX68GL1G0G). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

ARRAY ARCHITECTURE

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in "6. BLOCK STRUCTURE".

6. BLOCK STRUCTURE

Table 1. MX29GL512G SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address A24-A16	Address Range (x16)
Kbytes	Kwords			
128	64	SA0	000000000	0000000h-000FFFFh
128	64	SA1	000000001	0010000h-001FFFFh
128	64	SA2	000000010	0020000h-002FFFFh
:	:	:	:	:
128	64	SA511	111111111	1FF0000h-1FFFFFFh

Table 2. MX68GL1G0G SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address A25-A16	Address Range (x16)
Kbytes	Kwords			
128	64	SA0	0000000000	0000000h-000FFFFh
128	64	SA1	0000000001	0010000h-001FFFFh
128	64	SA2	0000000010	0020000h-002FFFFh
:	:	:	:	:
128	64	SA1023	1111111111	3FF0000h-3FFFFFFh

7. BUS OPERATION

Table 3. BUS OPERATION

<table>
<tr><th rowspan="3">Mode Select</th><th rowspan="3">RE-SET#</th><th rowspan="3">CE#</th><th rowspan="3">WE#</th><th rowspan="3">OE#</th><th rowspan="3">Address (Note4)</th><th rowspan="3">Data I/O Q7~Q0</th><th colspan="2">Byte#</th><th rowspan="3">WP#/ ACC</th></tr>
<tr><th>Vil</th><th>Vih</th></tr>
<tr><th colspan="2">Data (I/O) Q15~Q8</th></tr>
<tr><td>Device Reset</td><td>L</td><td>X</td><td>X</td><td>X</td><td>X</td><td>HighZ</td><td>HighZ</td><td>HighZ</td><td>L/H</td></tr>
<tr><td>Standby Mode</td><td>Vcc ± 0.3V</td><td>Vcc± 0.3V</td><td>X</td><td>X</td><td>X</td><td>HighZ</td><td>HighZ</td><td>HighZ</td><td>H</td></tr>
<tr><td>Output Disable</td><td>H</td><td>L</td><td>H</td><td>H</td><td>X</td><td>HighZ</td><td>HighZ</td><td>HighZ</td><td>L/H</td></tr>
<tr><td>Read Mode</td><td>H</td><td>L</td><td>H</td><td>L</td><td>AIN</td><td>DOUT</td><td rowspan="3">Q8-Q14= HighZ, Q15=A-1</td><td>DOUT</td><td>L/H</td></tr>
<tr><td>Write</td><td>H</td><td>L</td><td>L</td><td>H</td><td>AIN</td><td>DIN</td><td>DIN</td><td>Note1,2</td></tr>
<tr><td>Accelerate Program</td><td>H</td><td>L</td><td>L</td><td>H</td><td>AIN</td><td>DIN</td><td>DIN</td><td>Vhv</td></tr>
</table>

Notes:
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.

8. FUNCTIONAL OPERATION DESCRIPTION

8-1. READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

8-2. PAGE READ

This device is able to conduct Macronix compatible high performance page read. Page size is 32 bytes or 16 words. The higher address Amax ~ A4 select the certain page, while A3~A0 for word mode, A3~A-1 for byte mode select the particular word or byte in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

8-3. WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in *"Figure 18. COMMAND WRITE TIMING WAVEFORM (WE# CONTROLLED)".* The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

8-4. DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

8-5. STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

8-6. OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Byte or Word Data (I/O) pins will drive data.

8-7. BYTE/WORD SELECTION

The BYTE# input pin is used to select the organization of the array data and how the data is input/output on the Data (I/O) pins. If the BYTE# pin is held HIGH, Word mode will be selected and all 16 data lines (Q0 to Q15) will be active.

If BYTE# is forced LOW, Byte mode will be active and only data lines Q0 to Q7 will be active. Data lines Q8 to Q14 will remain in a high impedance state and Q15 becomes the A-1 address input pin.

8-8. HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

8-9. ACCELERATED PROGRAM OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Program mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated program, the current drawn from the WP#/ACC pin is no more than Icp1.

8-10. WRITE BUFFER PROGRAM OPERATION

Programs 256 word in word mode program and 256 byte in byte mode program operation. To trigger the Write Buffer Program, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined program Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax~A8.

"Write-Buffer-Page" address has to be the same for all address/data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer program operation is finished, it'll return to normal READ mode.

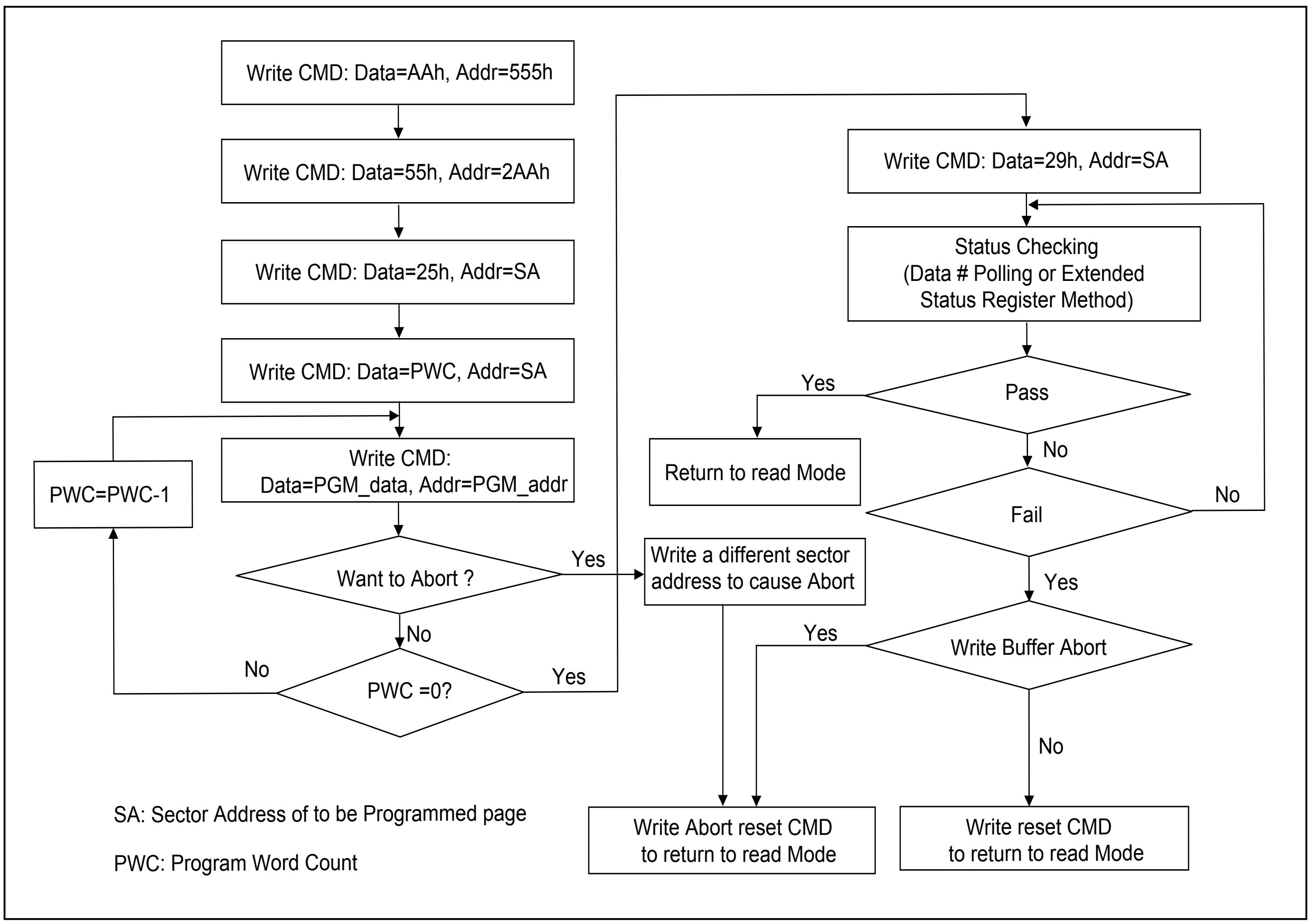
ABORT will be executed for the Write Buffer Program Sequence if following condition occurs:

- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle.
A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer program can be conducted in any sequence. However the CFI functions, autoselect, Security sector are not functional when program operation is in progress. Multiple write buffer program operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can’t be programmed from 0 back to 1.

Figure 1. WRITE BUFFER PROGRAM FLOWCHART



8-11. SECTOR PROTECT OPERATION

The device provides user programmable protection operations for selected sectors. Please refer to *"6. BLOCK STRUCTURE"* which show all Sector assignments.

During the protection operation, the sector address of any sector may be used to specify the sector being protected.

8-12. AUTOMATIC SELECT OPERATIONS

Automatic Select mode is used to access the manufacturer ID, device ID and CFI code. The automatic select mode has four command cycles. There are 2 methods to enter automatic select mode, user can issues the autoselect commands or applies the high voltage on the A9 pin. Please see AUTOMATIC SELECT OPERATIONS in the COMMAND OPERATIONS section.

8-13. INHERENT DATA PROTECTION

To avoid accidental erase or program of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

8-14. COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

8-15. LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write commands are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

8-16. WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

8-17. LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

8-18. POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

8-19. POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

8-20. POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

9. COMMAND OPERATIONS

9-1. READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to READ OPERATION in the BUS OPERATIONS section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding Tesl period) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector(s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

9-2. AUTOMATIC PROGRAM OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct cycle defined in the *"Table 9. COMMAND DEFINITIONS"* (including 2 unlock cycles and the A0H program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for program and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

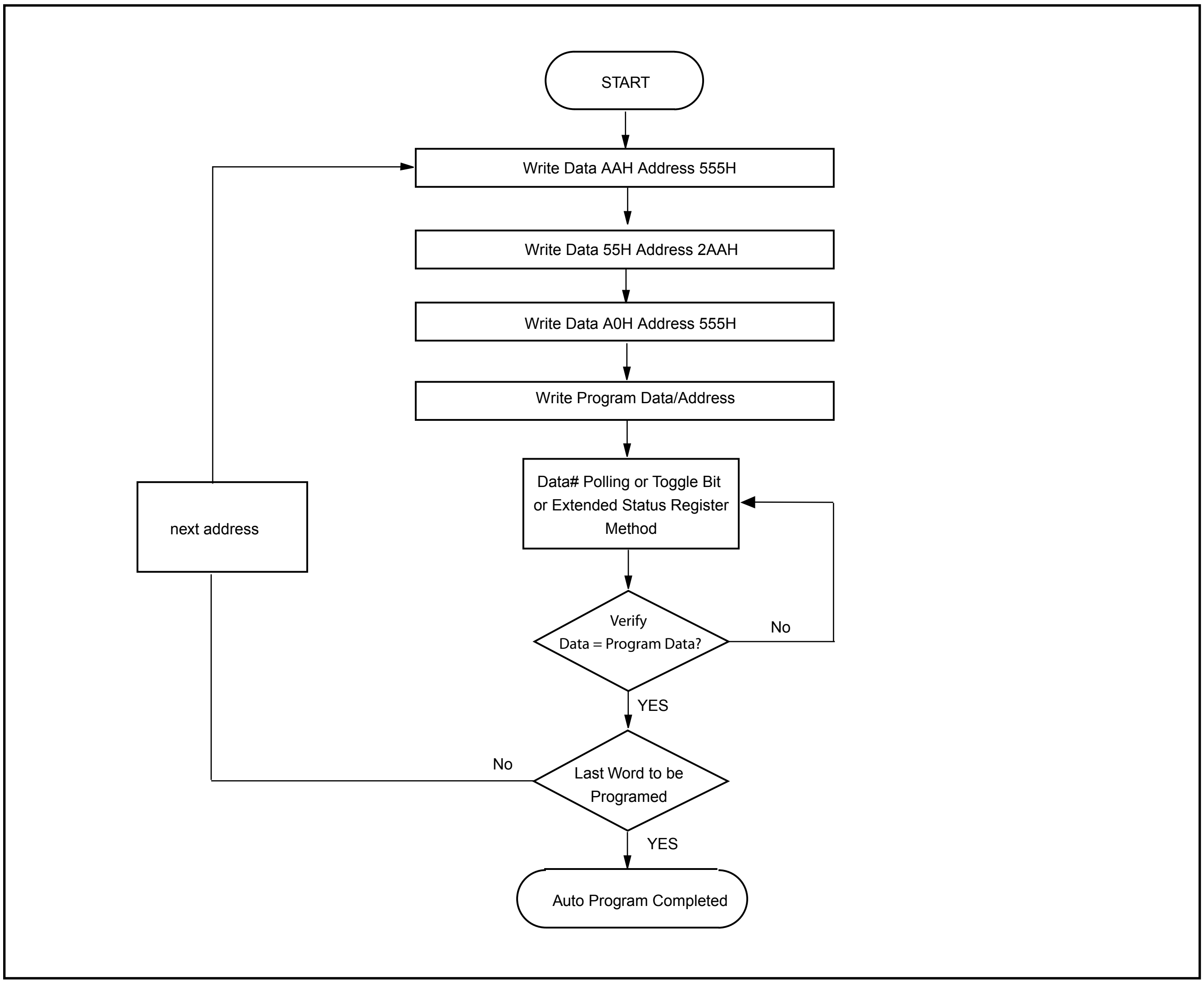
With the internal WSM automatically controlling the program process, the user only needs to enter the program command and data once.

Program will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by program. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

Please refer to the following figure for automatic programming flowchart.

Figure 2. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register.

9-3. ERASING THE MEMORY ARRAY

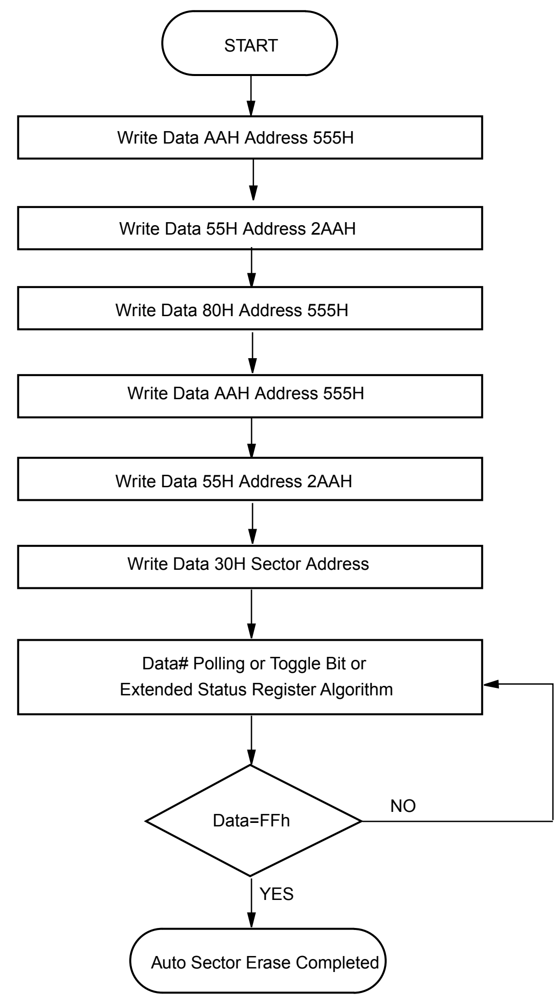
There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, the selected sector shall be erased. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in Section *"9-17. ADVANCED SECTOR PROTECTION/UNPROTECTION"*.

9-4. SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command.

After the embedded sector erase operation begins, all commands except Erase Suspend and Extended Status Register Read will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode. Please refer to the following figure for sector erase flowchart.

Figure 3. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART



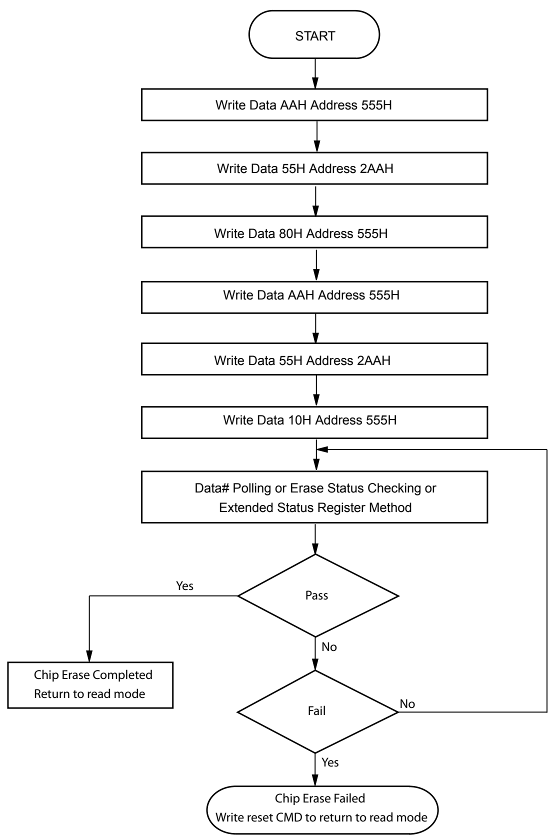
The system can determine the status of the automatic sector erase operation by the status register, see the STATUS REGISTER for the details.

9-5. CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode. See following figure for chip erase flowchart.

Figure 4. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



The system can determine the status of the embedded chip erase operation by the status register, see the STATUS REGISTER for the details.

9-6. ERASE SUSPEND/RESUME

After beginning a sector erase operation, Erase Suspend and read Extended Status Register are the valid commands that may be issued. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until Tesl period has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY# of Status Register or Extended Status Register.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector (s) except this suspended sector. Reading this sector being erased will return the contents of status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. See following figure for erase suspend/resume flowchart.

9-7. SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a Ters interval between Ease Resume and the next Erase Suspend command.

9-8. PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend and read Extended Status Register are the valid commands that may be issued. If the system issues an Program Suspend command after the program operation has already begun, the device will not enter Program-Suspended Read mode until Tpsl period has elapsed. The system can determine if the device has entered the Program-Suspended Read mode through Q6 and RY/BY# of Status Register or Extended Status Register.

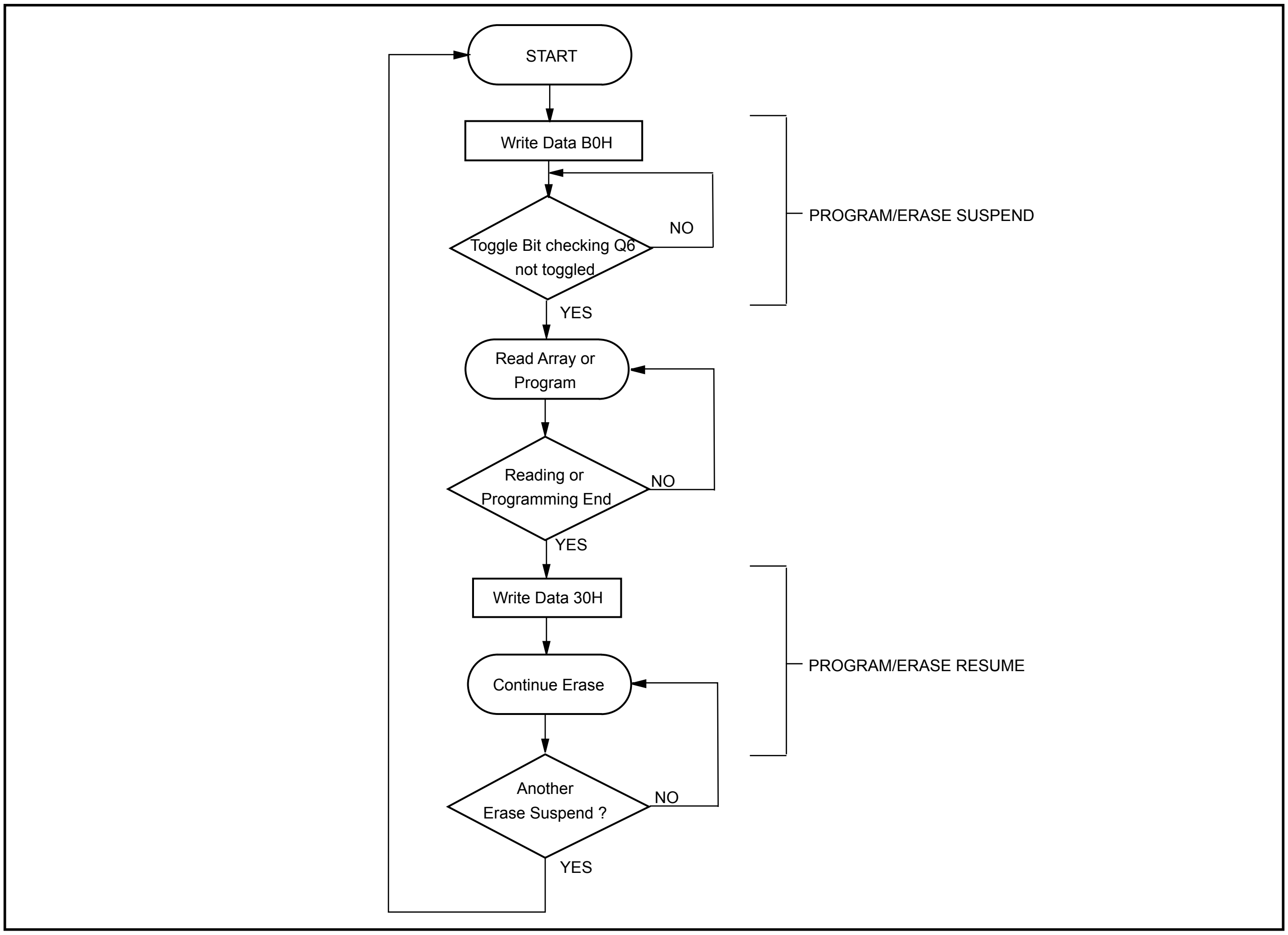
After the device has entered Program-Suspended mode, the system can read any sector(s) except those being programmed by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device, see the STATUS REGISTER for the details.

When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security sector.

9-9. PROGRAM RESUME

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a Tprs interval between Program Resume and the next Program Suspend command.

Figure 5. PROGRAM/ERASE SUSPEND/RESUME ALGORITHM FLOWCHART



The system can use the status register bits shown in the following table to determine the current state of the device, see the STATUS REGISTER for the details.

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as Automatic select, program, CFI query and erase resume.

9-10. BLANK CHECK

Blank Check command can check if the erase operation works correctly in the selected sector. During the Blank Check, array read operation will return the contents of status register.

Write data 33h to address 555h into the sector to start the Blank Check.

In the following operations, Blank Check may not be written successfully:

1. program
2. erase
3. suspend

Device Ready (bit 7) of Extended Status Register or Status Register can display if the Blank Check is in progress or not.
Erase status (bit 5) of the Extended Status Register or Status Register can display the blank check result.