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MX29GL320E T/B, MX29GL320E H/L

DATASHEET

Contents

SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
  - V I/O voltage must tight with VCC
    - VI/O=VCC=2.7V~3.6V
- Byte/Word mode switchable
  - 4,194,304 x 8 / 2,097,152 x 16
- Sector architecture
  - MX29GL320E T/B: 63 x 32Kword(64KB) + 8 x 4Kword(8KB) boot sector
  - MX29GL320E H/L: 64 x 32Kword(64KB) Uniform sector
- 16-byte/8-word page read buffer
- 32-byte/16-word write buffer
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced sector protection function (Persifent and Password Protect)
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode

PERFORMANCE

- High Performance
  - Fast access time: 70ns
  - Page access time: 25ns
  - Fast program time: 10us/word
  - Fast erase time: 0.5s/sector
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 20uA (typical)
- Typical 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

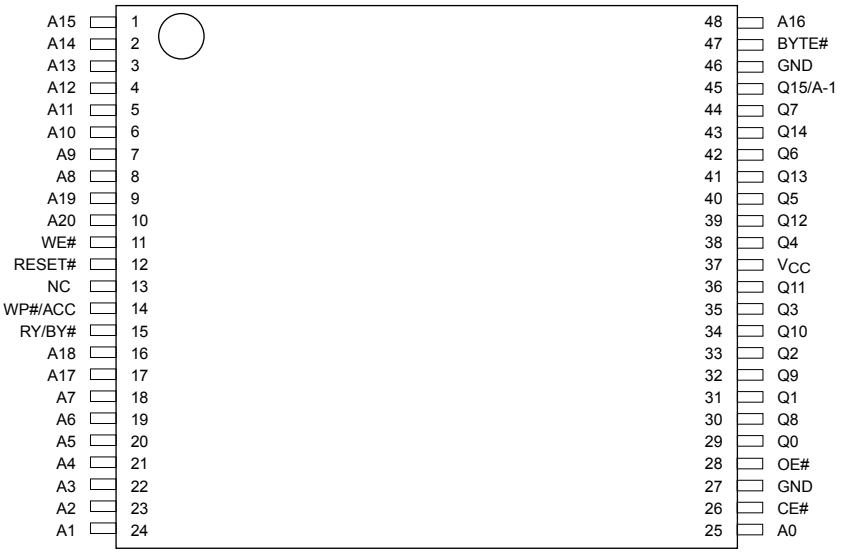
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability
  - MX29GL320E T/B: Protect Top or Bottom two sectors if WP#/ACC=Vil
  - MX29GL320E H/L: Protect first or last sector if WP#/ACC=Vil

PACKAGE

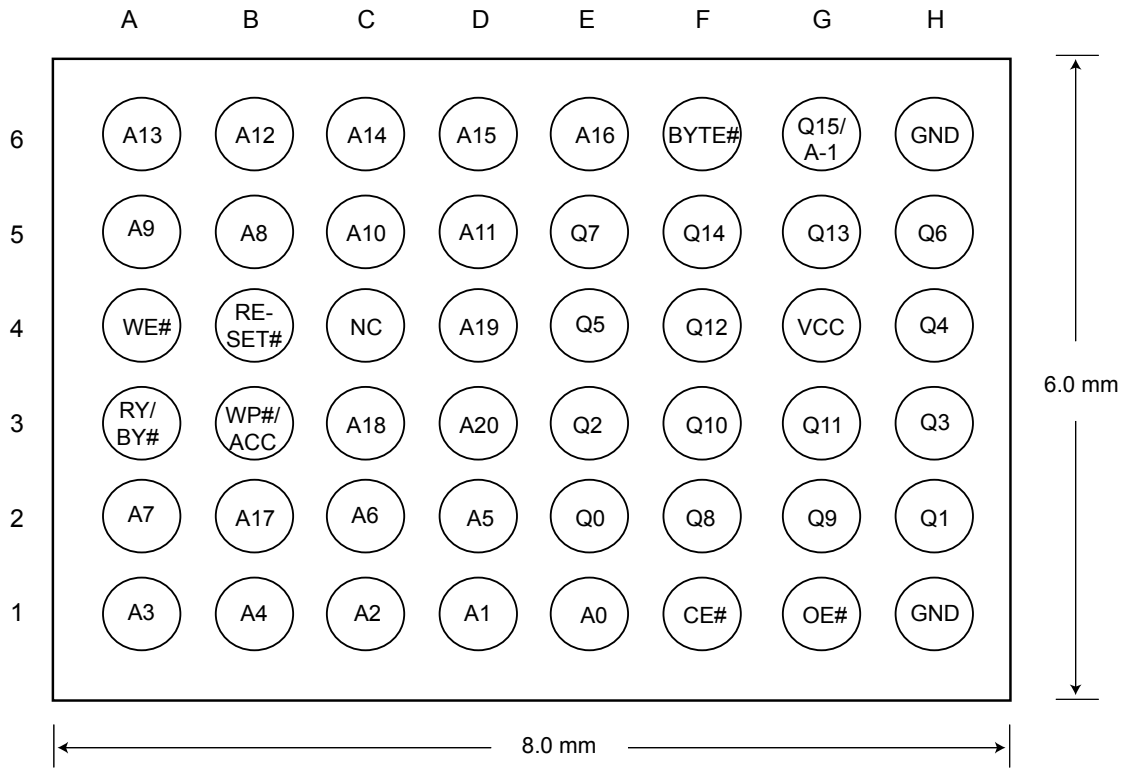
- MX29GL320E T/B
  - 48-pin TSOP
  - 48-ball LFBGA (6x8mm)
- MX29GL320E H/L
  - 56-pin TSOP
  - 64-ball LFBGA (11x13mm)
- **All devices are RoHS Compliant and Halogen-free**

PIN CONFIGURATION for MX29GL320E T/B

48 TSOP

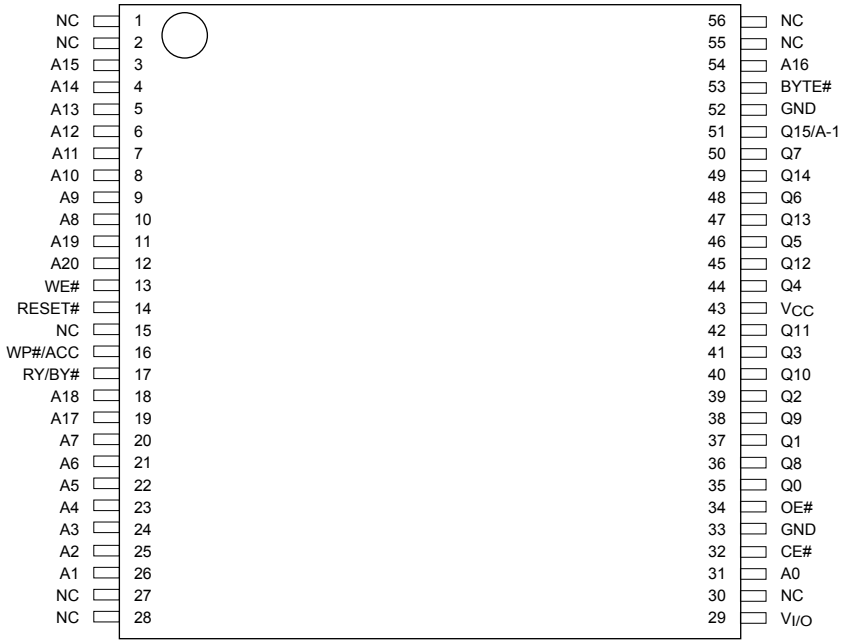


48 LFBGA

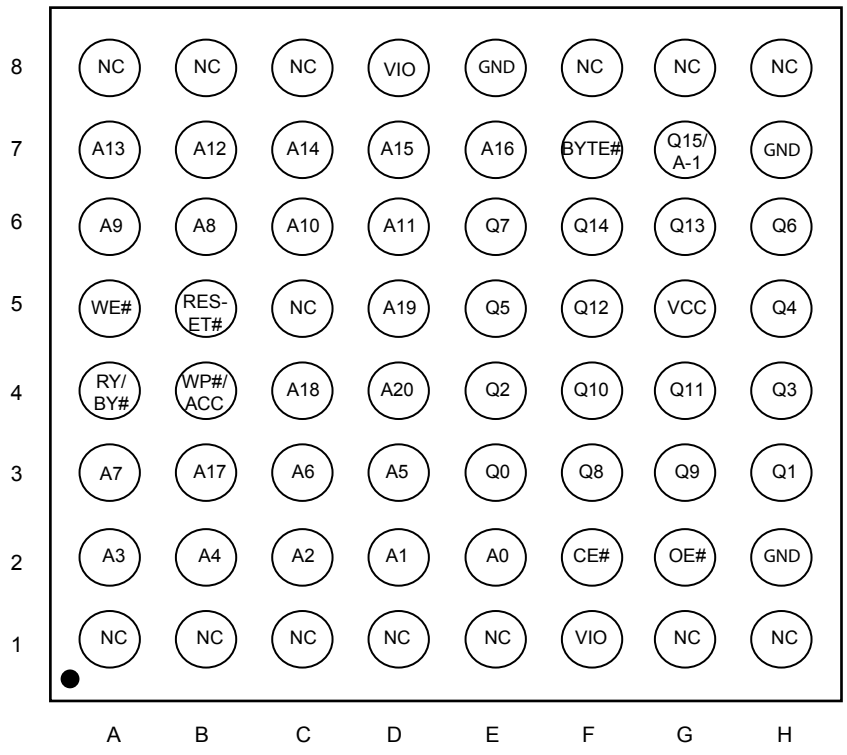


PIN CONFIGURATION for MX29GL320E H/L

56 TSOP



64 LFBGA

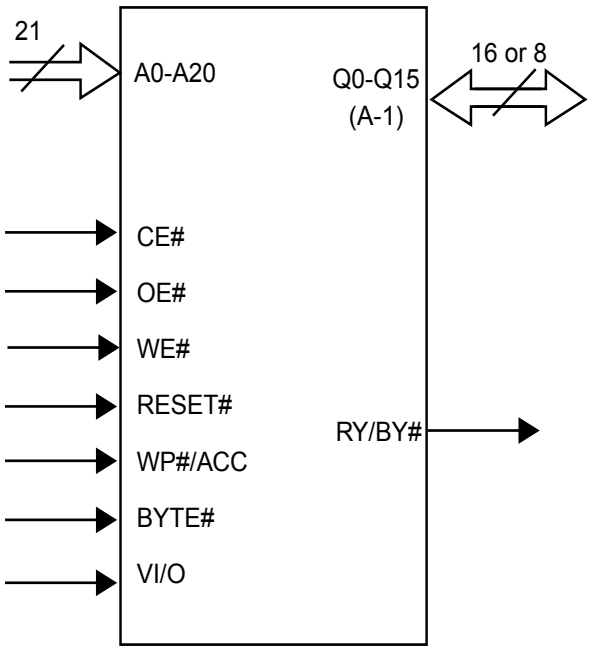


PIN DESCRIPTION

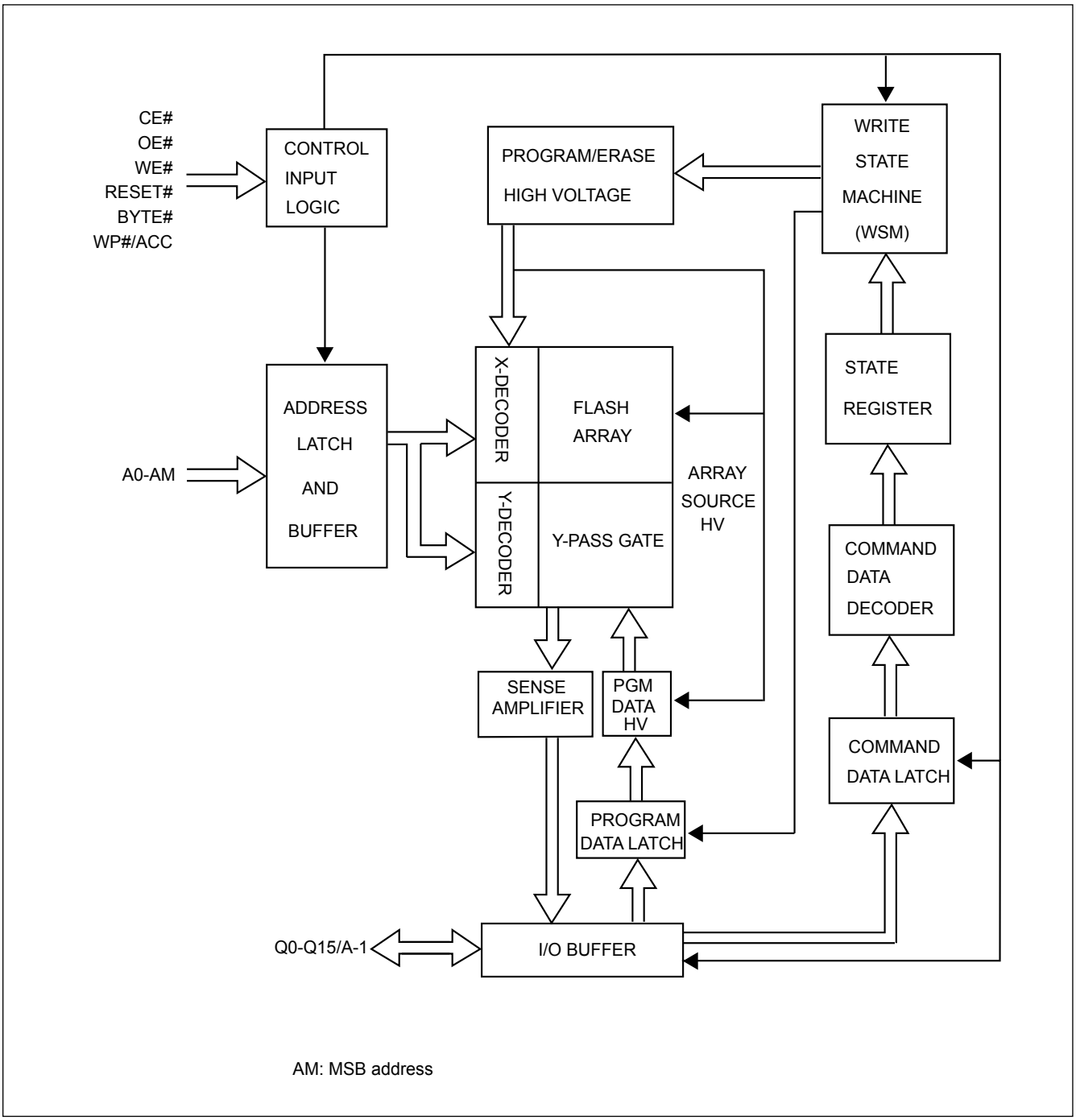
SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC*	Hardware Write Protect/Programming Acceleration input
RY/BY#	Read/Busy Output
BYTE#	Selects 8 bits or 16 bits mode
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally
VI/O	Power Supply for Input/Output

Notes:
1. WP#/ACC has internal pull up.
2. VI/O voltage must tight with VCC.
   VI/O = VCC =2.7V~3.6V.

LOGIC SYMBOL



BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

The block diagram on Page 9 illustrates a simplified architecture of this device. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM. The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

ARRAY ARCHITECTURE

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in Table 1.

BLOCK STRUCTURE

Table 1-1. MX29GL320ET SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address	(x8)	(x16)
Kbytes	Kwords		A20-A12	Address Range	Address Range
64	32	SA0	0000000xxx	000000h-00FFFFh	000000h-07FFFh
64	32	SA1	0000001xxx	010000h-01FFFFh	008000h-0FFFFh
64	32	SA2	0000010xxx	020000h-02FFFFh	010000h-17FFFh
64	32	SA3	0000011xxx	030000h-03FFFFh	018000h-01FFFFh
64	32	SA4	0000100xxx	040000h-04FFFFh	020000h-027FFFh
64	32	SA5	0000101xxx	050000h-05FFFFh	028000h-02FFFFh
64	32	SA6	0000110xxx	060000h-06FFFFh	030000h-037FFFh
64	32	SA7	0000111xxx	070000h-07FFFFh	038000h-03FFFFh
64	32	SA8	0001000xxx	080000h-08FFFFh	040000h-047FFFh
64	32	SA9	0001001xxx	090000h-09FFFFh	048000h-04FFFFh
64	32	SA10	0001010xxx	0A0000h-0AFFFFh	050000h-057FFFh
64	32	SA11	0001011xxx	0B0000h-0BFFFFh	058000h-05FFFFh
64	32	SA12	0001100xxx	0C0000h-0CFFFFh	060000h-067FFFh
64	32	SA13	0001101xxx	0D0000h-0DFFFFh	068000h-06FFFFh
64	32	SA14	0001110xxx	0E0000h-0EFFFFh	070000h-077FFFh
64	32	SA15	0001111xxx	0F0000h-0FFFFFh	078000h-07FFFFh
64	32	SA16	0010000xxx	100000h-10FFFFh	080000h-087FFFh
64	32	SA17	0010001xxx	110000h-11FFFFh	088000h-08FFFFh
64	32	SA18	0010010xxx	120000h-12FFFFh	090000h-097FFFh
64	32	SA19	0010011xxx	130000h-13FFFFh	098000h-09FFFFh
64	32	SA20	0010100xxx	140000h-14FFFFh	0A0000h-0A7FFFh
64	32	SA21	0010101xxx	150000h-15FFFFh	0A8000h-0AFFFFh
64	32	SA22	0010110xxx	160000h-16FFFFh	0B0000h-0B7FFFh
64	32	SA23	0010111xxx	170000h-17FFFFh	0B8000h-0BFFFFh
64	32	SA24	0011000xxx	180000h-18FFFFh	0C0000h-0C7FFFh
64	32	SA25	0011001xxx	190000h-19FFFFh	0C8000h-0CFFFFh
64	32	SA26	0011010xxx	1A0000h-1AFFFFh	0D0000h-0D7FFFh
64	32	SA27	0011011xxx	1B0000h-1BFFFFh	0D8000h-0DFFFFh
64	32	SA28	0011100xxx	1C0000h-1CFFFFh	0E0000h-0E7FFFh
64	32	SA29	0011101xxx	1D0000h-1DFFFFh	0E8000h-0EFFFFh
64	32	SA30	0011110xxx	1E0000h-1EFFFFh	0F0000h-0F7FFFh
64	32	SA31	0011111xxx	1F0000h-1FFFFFh	0F8000h-0FFFFFh
64	32	SA32	0100000xxx	200000h-20FFFFh	100000h-107FFFh
64	32	SA33	0100001xxx	210000h-21FFFFh	108000h-10FFFFh
64	32	SA34	0100010xxx	220000h-22FFFFh	110000h-117FFFh
64	32	SA35	0100011xxx	230000h-23FFFFh	118000h-11FFFFh
64	32	SA36	0100100xxx	240000h-24FFFFh	120000h-127FFFh
64	32	SA37	0100101xxx	250000h-25FFFFh	128000h-12FFFFh
64	32	SA38	0100110xxx	260000h-26FFFFh	130000h-137FFFh
64	32	SA39	0100111xxx	270000h-27FFFFh	138000h-13FFFFh

Sector Size		Sector	Sector Address A20-A12	(x8) Address Range	(x16) Address Range
Kbytes	Kwords				
64	32	SA40	0101000xxx	280000h-28FFFFh	140000h-147FFFh
64	32	SA41	0101001xxx	290000h-29FFFFh	148000h-14FFFFh
64	32	SA42	0101010xxx	2A0000h-2AFFFFh	150000h-157FFFh
64	32	SA43	0101011xxx	2B0000h-2BFFFFh	158000h-15FFFFh
64	32	SA44	0101100xxx	2C0000h-2CFFFFh	160000h-147FFFh
64	32	SA45	0101101xxx	2D0000h-2DFFFFh	168000h-14FFFFh
64	32	SA46	0101110xxx	2E0000h-2EFFFFh	170000h-177FFFh
64	32	SA47	0101111xxx	2F0000h-2FFFFFh	178000h-17FFFFh
64	32	SA48	0110000xxx	300000h-30FFFFh	180000h-187FFFh
64	32	SA49	0110001xxx	310000h-31FFFFh	188000h-18FFFFh
64	32	SA50	0110010xxx	320000h-32FFFFh	190000h-197FFFh
64	32	SA51	0110011xxx	330000h-33FFFFh	198000h-19FFFFh
64	32	SA52	0110100xxx	340000h-34FFFFh	1A0000h-1A7FFFh
64	32	SA53	0110101xxx	350000h-35FFFFh	1A8000h-1AFFFFh
64	32	SA54	0110110xxx	360000h-36FFFFh	1B0000h-1B7FFFh
64	32	SA55	0110111xxx	370000h-37FFFFh	1B8000h-1BFFFFh
64	32	SA56	0111000xxx	380000h-38FFFFh	1C0000h-1C7FFFh
64	32	SA57	0111001xxx	390000h-39FFFFh	1C8000h-1CFFFFh
64	32	SA58	0111010xxx	3A0000h-3AFFFFh	1D0000h-1D7FFFh
64	32	SA59	0111011xxx	3B0000h-3BFFFFh	1D8000h-1DFFFFh
64	32	SA60	0111100xxx	3C0000h-3CFFFFh	1E0000h-1E7FFFh
64	32	SA61	0111101xxx	3D0000h-3DFFFFh	1E8000h-1EFFFFh
64	32	SA62	0111110xxx	3E0000h-3EFFFFh	1F0000h-1F7FFFh
8	4	SA63	1111111000	3F0000h-3F1FFFh	1F8000h-1FFFFFh
8	4	SA64	1111111001	3F2000h-3F3FFFh	1F9000h-1F9FFFh
8	4	SA65	1111111010	3F4000h-3F5FFFh	1FA000h-1FAFFFh
8	4	SA66	1111111011	3F6000h-3F7FFFh	1FB000h-1FBFFFh
8	4	SA67	1111111100	3F8000h-3F9FFFh	1FC000h-1FCFFFh
8	4	SA68	1111111101	3FA000h-3FBFFFh	1FD000h-1FDFFFh
8	4	SA69	1111111110	3FC000h-3FDFFFh	1FE000h-1FEFFFh
8	4	SA70	1111111111	3FE000h-3FFFFFh	1FF000h-1FFFFFh

Table 1-2. MX29GL320EB SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address	(x8)	(x16)
Kbytes	Kwords		A20-A12	Address Range	Address Range
8	4	SA0	0000000000	000000h-001FFFh	000000h-000FFFh
8	4	SA1	0000000001	002000h-003FFFh	001000h-001FFFh
8	4	SA2	0000000010	004000h-005FFFh	002000h-002FFFh
8	4	SA3	0000000011	006000h-007FFFh	003000h-003FFFh
8	4	SA4	0000000100	008000h-009FFFh	004000h-004FFFh
8	4	SA5	0000000101	00A000h-00BFFFh	005000h-005FFFh
8	4	SA6	0000000110	00C000h-00DFFFh	006000h-006FFFh
8	4	SA7	0000000111	00E000h-00FFFFh	007000h-007FFFh
64	32	SA8	0000001xxx	010000h-01FFFFh	008000h-00FFFFh
64	32	SA9	0000010xxx	020000h-02FFFFh	010000h-017FFFh
64	32	SA10	0000011xxx	030000h-03FFFFh	018000h-01FFFFh
64	32	SA11	0000100xxx	040000h-04FFFFh	020000h-027FFFh
64	32	SA12	0000101xxx	050000h-05FFFFh	028000h-02FFFFh
64	32	SA13	0000110xxx	060000h-06FFFFh	030000h-037FFFh
64	32	SA14	0000111xxx	070000h-07FFFFh	038000h-03FFFFh
64	32	SA15	0001000xxx	080000h-08FFFFh	040000h-047FFFh
64	32	SA16	0001001xxx	090000h-09FFFFh	048000h-04FFFFh
64	32	SA17	0001010xxx	0A0000h-0AFFFFh	050000h-057FFFh
64	32	SA18	0001011xxx	0B0000h-0BFFFFh	058000h-05FFFFh
64	32	SA19	0001100xxx	0C0000h-0CFFFFh	060000h-067FFFh
64	32	SA20	0001101xxx	0D0000h-0DFFFFh	068000h-06FFFFh
64	32	SA21	0001110xxx	0E0000h-0EFFFFh	070000h-077FFFh
64	32	SA22	0001111xxx	0F0000h-0FFFFFh	078000h-07FFFFh
64	32	SA23	0010000xxx	100000h-10FFFFh	080000h-087FFFh
64	32	SA24	0010001xxx	110000h-11FFFFh	088000h-08FFFFh
64	32	SA25	0010010xxx	120000h-12FFFFh	090000h-097FFFh
64	32	SA26	0010011xxx	130000h-13FFFFh	098000h-09FFFFh
64	32	SA27	0010100xxx	140000h-14FFFFh	0A0000h-0A7FFFh
64	32	SA28	0010101xxx	150000h-15FFFFh	0A8000h-0AFFFFh
64	32	SA29	0010110xxx	160000h-16FFFFh	0B0000h-0B7FFFh
64	32	SA30	0010111xxx	170000h-17FFFFh	0B8000h-0BFFFFh
64	32	SA31	0011000xxx	180000h-18FFFFh	0C0000h-0C7FFFh
64	32	SA32	0011001xxx	190000h-19FFFFh	0C8000h-0CFFFFh
64	32	SA33	0011010xxx	1A0000h-1AFFFFh	0D0000h-0D7FFFh
64	32	SA34	0011011xxx	1B0000h-1BFFFFh	0D8000h-0DFFFFh
64	32	SA35	0011100xxx	1C0000h-1CFFFFh	0E0000h-0E7FFFh
64	32	SA36	0011101xxx	1D0000h-1DFFFFh	0E8000h-0EFFFFh
64	32	SA37	0011110xxx	1E0000h-1EFFFFh	0F0000h-0F7FFFh
64	32	SA38	0011111xxx	1F0000h-1FFFFFh	0F8000h-0FFFFFh
64	32	SA39	0100000xxx	200000h-20FFFFh	100000h-107FFFh
64	32	SA40	0100001xxx	210000h-21FFFFh	108000h-10FFFFh
64	32	SA41	0100010xxx	220000h-22FFFFh	110000h-117FFFh

Sector Size		Sector	Sector Address A20-A12	(x8) Address Range	(x16) Address Range
Kbytes	Kwords				
64	32	SA42	0100011xxx	230000h-23FFFFh	118000h-11FFFFh
64	32	SA43	0100100xxx	240000h-24FFFFh	120000h-127FFFh
64	32	SA44	0100101xxx	250000h-25FFFFh	128000h-12FFFFh
64	32	SA45	0100110xxx	260000h-26FFFFh	130000h-137FFFh
64	32	SA46	0100111xxx	270000h-27FFFFh	138000h-13FFFFh
64	32	SA47	0101000xxx	280000h-28FFFFh	140000h-147FFFh
64	32	SA48	0101001xxx	290000h-29FFFFh	148000h-14FFFFh
64	32	SA49	0101010xxx	2A0000h-2AFFFFh	150000h-157FFFh
64	32	SA50	0101011xxx	2B0000h-2BFFFFh	158000h-15FFFFh
64	32	SA51	0101100xxx	2C0000h-2CFFFFh	160000h-167FFFh
64	32	SA52	0101101xxx	2D0000h-2DFFFFh	168000h-16FFFFh
64	32	SA53	0101110xxx	2E0000h-2EFFFFh	170000h-177FFFh
64	32	SA54	0101111xxx	2F0000h-2FFFFFh	178000h-17FFFFh
64	32	SA55	0110000xxx	300000h-30FFFFh	180000h-187FFFh
64	32	SA56	0110001xxx	310000h-31FFFFh	188000h-18FFFFh
64	32	SA57	0110010xxx	320000h-32FFFFh	190000h-197FFFh
64	32	SA58	0110011xxx	330000h-33FFFFh	198000h-19FFFFh
64	32	SA59	0110100xxx	340000h-34FFFFh	1A0000h-1A7FFFh
64	32	SA60	0110101xxx	350000h-35FFFFh	1A8000h-1AFFFFh
64	32	SA61	0110110xxx	360000h-36FFFFh	1B0000h-1B7FFFh
64	32	SA62	0110111xxx	370000h-37FFFFh	1B8000h-1BFFFFh
64	32	SA63	0111000xxx	380000h-38FFFFh	1C0000h-1C7FFFh
64	32	SA64	0111001xxx	390000h-39FFFFh	1C8000h-1CFFFFh
64	32	SA65	0111010xxx	3A0000h-3AFFFFh	1D0000h-1D7FFFh
64	32	SA66	0111011xxx	3B0000h-3BFFFFh	1D8000h-1DFFFFh
64	32	SA67	0111100xxx	3C0000h-3CFFFFh	1E0000h-1E7FFFh
64	32	SA68	0111101xxx	3D0000h-3DFFFFh	1E8000h-1EFFFFh
64	32	SA69	0111110xxx	3E0000h-3EFFFFh	1F0000h-1F7FFFh
64	32	SA70	0111111xxx	3F0000h-3FFFFFh	1F8000h-1FFFFFh

Table 1-3. MX29GL320E H/L SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address	(x8)	(x16)
Kbytes	Kwords		A20-A15	Address Range	Address Range
64	32	SA0	0000000	000000h-00FFFFh	000000h-007FFFh
64	32	SA1	0000001	010000h-01FFFFh	008000h-00FFFFh
64	32	SA2	0000010	020000h-02FFFFh	010000h-017FFFh
64	32	SA3	0000011	030000h-03FFFFh	018000h-01FFFFh
64	32	SA4	0000100	040000h-04FFFFh	020000h-027FFFh
64	32	SA5	0000101	050000h-05FFFFh	028000h-02FFFFh
64	32	SA6	0000110	060000h-06FFFFh	030000h-037FFFh
64	32	SA7	0000111	070000h-07FFFFh	038000h-03FFFFh
64	32	SA8	0001000	080000h-08FFFFh	040000h-047FFFh
64	32	SA9	0001001	090000h-09FFFFh	048000h-04FFFFh
64	32	SA10	0001010	0A0000h-0AFFFFh	050000h-057FFFh
64	32	SA11	0001011	0B0000h-0BFFFFh	058000h-05FFFFh
64	32	SA12	0001100	0C0000h-0CFFFFh	060000h-067FFFh
64	32	SA13	0001101	0D0000h-0DFFFFh	068000h-06FFFFh
64	32	SA14	0001110	0E0000h-0EFFFFh	070000h-077FFFh
64	32	SA15	0001111	0F0000h-0FFFFFh	078000h-07FFFFh
64	32	SA16	0010000	100000h-10FFFFh	080000h-087FFFh
64	32	SA17	0010001	110000h-11FFFFh	088000h-08FFFFh
64	32	SA18	0010010	120000h-12FFFFh	090000h-097FFFh
64	32	SA19	0010011	130000h-13FFFFh	098000h-09FFFFh
64	32	SA20	0010100	140000h-14FFFFh	0A0000h-0A7FFFh
64	32	SA21	0010101	150000h-15FFFFh	0A8000h-0AFFFFh
64	32	SA22	0010110	160000h-16FFFFh	0B0000h-0B7FFFh
64	32	SA23	0010111	170000h-17FFFFh	0B8000h-0BFFFFh
64	32	SA24	0011000	180000h-18FFFFh	0C0000h-0C7FFFh
64	32	SA25	0011001	190000h-19FFFFh	0C8000h-0CFFFFh
64	32	SA26	0011010	1A0000h-1AFFFFh	0D0000h-0D7FFFh
64	32	SA27	0011011	1B0000h-1BFFFFh	0D8000h-0DFFFFh
64	32	SA28	0011100	1C0000h-1CFFFFh	0E0000h-0E7FFFh
64	32	SA29	0011101	1D0000h-1DFFFFh	0E8000h-0EFFFFh
64	32	SA30	0011110	1E0000h-1EFFFFh	0F0000h-0F7FFFh
64	32	SA31	0011111	1F0000h-1FFFFFh	0F8000h-0FFFFFh
64	32	SA32	0100000	200000h-20FFFFh	100000h-107FFFh
64	32	SA33	0100001	210000h-21FFFFh	108000h-10FFFFh
64	32	SA34	0100010	220000h-22FFFFh	110000h-117FFFh
64	32	SA35	0100011	230000h-23FFFFh	118000h-11FFFFh
64	32	SA36	0100100	240000h-24FFFFh	120000h-127FFFh
64	32	SA37	0100101	250000h-25FFFFh	128000h-12FFFFh
64	32	SA38	0100110	260000h-26FFFFh	130000h-137FFFh
64	32	SA39	0100111	270000h-27FFFFh	138000h-13FFFFh
64	32	SA40	0101000	280000h-28FFFFh	140000h-147FFFh

Sector Size		Sector	Sector Address	(x8)	(x16)
Kbytes	Kwords		A20-A15	Address Range	Address Range
64	32	SA41	0101001	290000h-29FFFFh	148000h-14FFFFh
64	32	SA42	0101010	2A0000h-2AFFFFh	150000h-157FFFh
64	32	SA43	0101011	2B0000h-2BFFFFh	158000h-15FFFFh
64	32	SA44	0101100	2C0000h-2CFFFFh	160000h-167FFFh
64	32	SA45	0101101	2D0000h-2DFFFFh	168000h-16FFFFh
64	32	SA46	0101110	2E0000h-2EFFFFh	170000h-177FFFh
64	32	SA47	0101111	2F0000h-2FFFFFh	178000h-17FFFFh
64	32	SA48	0110000	300000h-30FFFFh	180000h-187FFFh
64	32	SA49	0110001	310000h-31FFFFh	188000h-18FFFFh
64	32	SA50	0110010	320000h-32FFFFh	190000h-197FFFh
64	32	SA51	0110011	330000h-33FFFFh	198000h-19FFFFh
64	32	SA52	0110100	340000h-34FFFFh	1A0000h-1A7FFFh
64	32	SA53	0110101	350000h-35FFFFh	1A8000h-1AFFFFh
64	32	SA54	0110110	360000h-36FFFFh	1B0000h-1B7FFFh
64	32	SA55	0110111	370000h-37FFFFh	1B8000h-1BFFFFh
64	32	SA56	0111000	380000h-38FFFFh	1C0000h-1C7FFFh
64	32	SA57	0111001	390000h-39FFFFh	1C8000h-1CFFFFh
64	32	SA58	0111010	3A0000h-3AFFFFh	1D0000h-1D7FFFh
64	32	SA59	0111011	3B0000h-3BFFFFh	1D8000h-1DFFFFh
64	32	SA60	0111100	3C0000h-3CFFFFh	1E0000h-1E7FFFh
64	32	SA61	0111101	3D0000h-3DFFFFh	1E8000h-1EFFFFh
64	32	SA62	0111110	3E0000h-3EFFFFh	1F0000h-1F7FFFh
64	32	SA63	0111111	3F0000h-3FFFFFh	1F8000h-1FFFFFh

BUS OPERATION

Table 2-1. BUS OPERATION

Mode Select	RE-SET#	CE#	WE#	OE#	Address (Note4)	Data I/O Q0~Q7	Byte# Vil Data (I/O) Q8~Q15	Byte# Vih Data (I/O) Q8~Q15	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ	L/H
Standby Mode	Vcc ± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ	H
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ, Q15=A1	DOUT	L/H
Write	H	L	L	H	AIN	DIN		DIN	Note1,2
Accelerate Program	H	L	L	H	AIN	DIN		DIN	Vhv

Notes:
1. MX29GL320E T/B: Protect Top or Bottom two sectors if WP#/ACC=Vil.
   MX29GL320E H/L: Protect first or last sector if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.

Table 2-2. BUS OPERATION

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q0 ~ Q7	Q8 ~ Q15
	CE#	WE#	OE#											
Sector Lock Status Verification	L	H	L	SA	X	V_{hv}	X	L	X	L	H	L	01h or 00h (Note 1)	X
Read Silicon ID Manufacturer Code	L	H	L	X	X	V_{hv}	X	L	X	L	L	L	C2H	X
Read Silicon ID -- MX29GL320E T/B														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H(Word), XXH(Byte)
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	1AH	22H(Word), XXH(Byte)
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	01H (Top) 00H (Bottom)	22H(Word), XXH(Byte)
Read Silicon ID -- MX29GL320E H/L														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H(Word), XXH(Byte)
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	1DH	22H(Word), XXH(Byte)
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	00H	22H(Word), XXH(Byte)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects high address sector: 9Ah.
   WP# protects low address sector: 8Ah
   Factory unlocked code: WP# protects high address sector: 1Ah.
   WP# protects low address sector: 0Ah
3. AM: MSB of address.

FUNCTIONAL OPERATION DESCRIPTION

READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

PAGE READ

This device is able to conduct MXIC MaskROM compatible high performance page read. Page size is 16 bytes or 8 words. The higher address Amax ~ A3 select the certain page, while A2~A0 for word mode, A2~A-1 for byte mode select the particular word or byte in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in Figure 4. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Byte or Word Data (I/O) pins will drive data.

BYTE/WORD SELECTION

The BYTE# input pin is used to select the organization of the array data and how the data is input/output on the Data (I/O) pins. If the BYTE# pin is held HIGH, Word mode will be selected and all 16 data lines (Q0 to Q15) will be active.

If BYTE# is forced LOW, Byte mode will be active and only data lines Q0 to Q7 will be active. Data lines Q8 to Q14 will remain in a high impedance state and Q15 becomes the A-1 address input pin.

HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The Top or Bottom two sectors (for MX29GL320E T/B) and the highest or lowest sector (for MX29GL320E H/L) was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

WRITE BUFFER PROGRAMMING OPERATION

Programs 32bytes/16words in a programming operation. To trigger the Write Buffer Programming, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined programming Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax-A4.

"Write-Buffer-Page" address has to be the same for all address/ data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it'll return to normal READ mode.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

WRITE BUFFER PROGRAMMING OPERATION (cont'd)

ABORT will be executed for the Write Buffer Programming Sequence if following condition occurs:
- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during
  the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle.
A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

SECTOR PROTECT OPERATION

The device provides user programmable protection operations for selected sectors. Please refer to Table 1 which show all Sector assignments.

During the protection operation, the sector address of any sector may be used to specify the Sector being protected.

AUTOMATIC SELECT BUS OPERATIONS

The following five bus operations require A9 to be raised to Vhv. Please see AUTOMATIC SELECT COMMAND SEQUENCE in the COMMAND OPERATIONS section for details of equivalent command operations that do not require the use of Vhv.

SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins A20 to A12, address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q7 to Q0.

READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 9Ah(H)/8Ah(L) will be present on data bits Q7 to Q0. Otherwise, the factory unlocked code of 1Ah(H)/0Ah(L) will be present.

INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

COMMAND OPERATIONS

READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to READ OPERATION in the BUS OPERATIONS section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding 20us) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector(s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct cycle defined in the Table 3 (including 2 unlock cycles and the A0H program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

COMMAND OPERATIONS (cont'd)

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY (cont'd)

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hard ware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

Status	Q7[*1]	Q6[*1]	Q5	Q1	RY/BY# (Note)
In progress	Q7#	Toggling	0	0	0
Exceed time limit	Q7#	Toggling	1	N/A	0

Note: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in section 5.

SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. Note that the 50us timer-out counter is restarted after every erase command sequence. If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.