



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MACRONIX
INTERNATIONAL Co., LTD.

MX29LV400C T/B
MX29LV800C T/B
MX29LV160C T/B

MX29LV400C T/B, MX29LV800C T/B, MX29LV160C T/B DATASHEET

The MX29LV160C T/B product family has been discontinued. The MX29LV160C T/B product family is not recommended for new designs. The MX29LV160D T/B family is the recommended replacement. Please refer to MX29LV160D T/B datasheet for full specifications and ordering information, or contact your local sales representative for additional support.

SINGLE VOLTAGE 3V ONLY FLASH MEMORY

The MX29LV160C T/B product family has been discontinued. The MX29LV160C T/B product family is not recommended for new designs. The MX29LV160D T/B family is the recommended replacement. Please refer to MX29LV160D T/B datasheet for full specifications and ordering information, or contact your local sales representative for additional support.

FEATURES

GENERAL FEATURES

- Byte/Word mode switchable:
 - 524,288 x8 / 262,144 x16 (MX29LV400C)
 - 1,048,576 x8 / 524,288 x16 (MX29LV800C)
 - 2,097,152 x8 / 1,048,576 x16 (MX29LV160C)
- Sector Structure
 - 16K-Byte x 1, 8K-Byte x 2, 32K-Byte x 1
64K-Byte x 7 (MX29LV400C), 64K-Byte x 15 (MX29LV800C), 64K-Byte x 31 (MX29LV160C)
 - Provides sector protect function to prevent program or erase operation in the protected sector
 - Provides chip unprotect function to allow code changing
 - Provides temporary sector unprotect function for code changing in previously protected sector
- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit : Vcc ≤ 1.4V
- Compatible with JEDEC standard
 - Pinout and software compatible to single power supply Flash
- **Functional compatible with MX29LV400B/MX29LV800B/MX29LV160B device**

PERFORMANCE

- High Performance
 - Fast access time: 45R (MX29LV400C and MX29LV800C only), 55R/70/90ns
 - Fast program time: 7us/word typical utilizing accelerate function
 - Fast erase time: 0.7s/sector, 15s/chip (typical, MX29LV160C)
- Low Power Consumption
 - Low active read current: 10mA (typical) at 5MHz
 - Low standby current: 200nA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
 - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
 - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

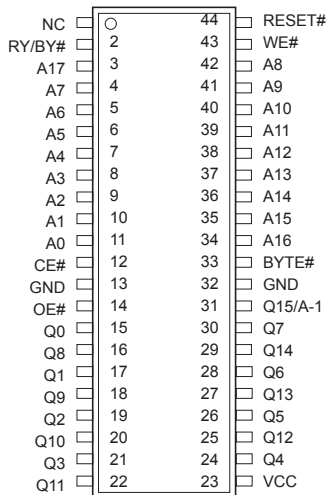
- Ready/Busy# (RY/BY#) Output
 - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
 - Provides a hardware method to reset the internal state machine to read mode

PACKAGE

- 44-Pin SOP
- 48-Pin TSOP
- 48-Ball TFBGA
- 48-Ball LFBGA
- 48-Ball WFBGA
- 48-Ball XFLGA
- All devices are RoHS Compliant

MX29LV400C PIN CONFIGURATIONS

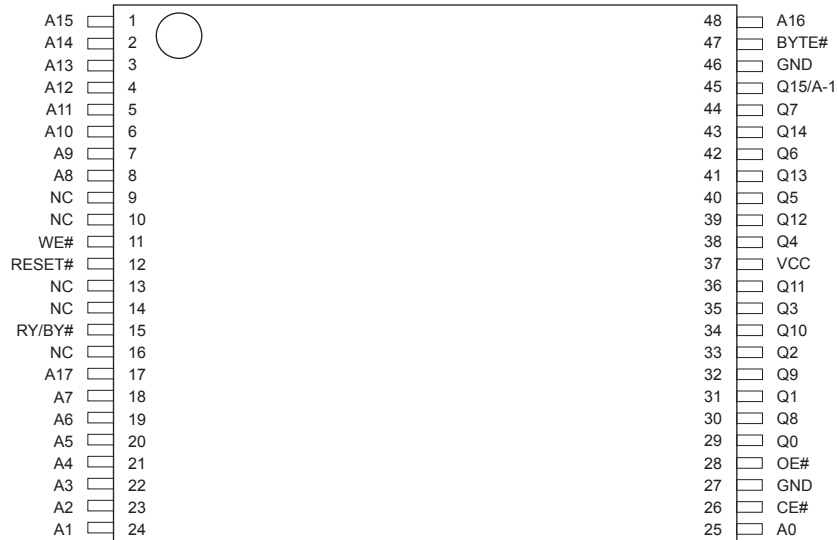
MX29LV400C 44 SOP(500 mil)



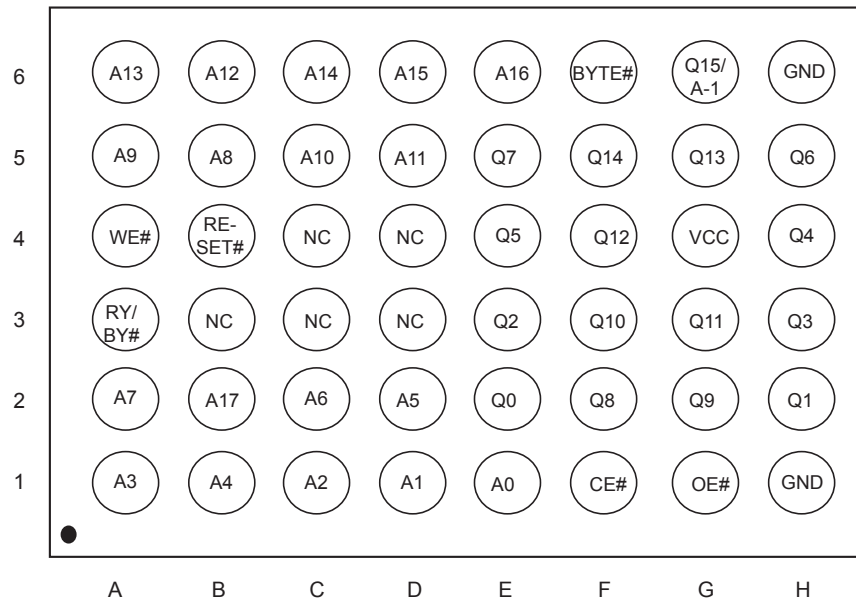
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15 (Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin/Sector Protect Unlock
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin
NC	Pin Not Connected Internally

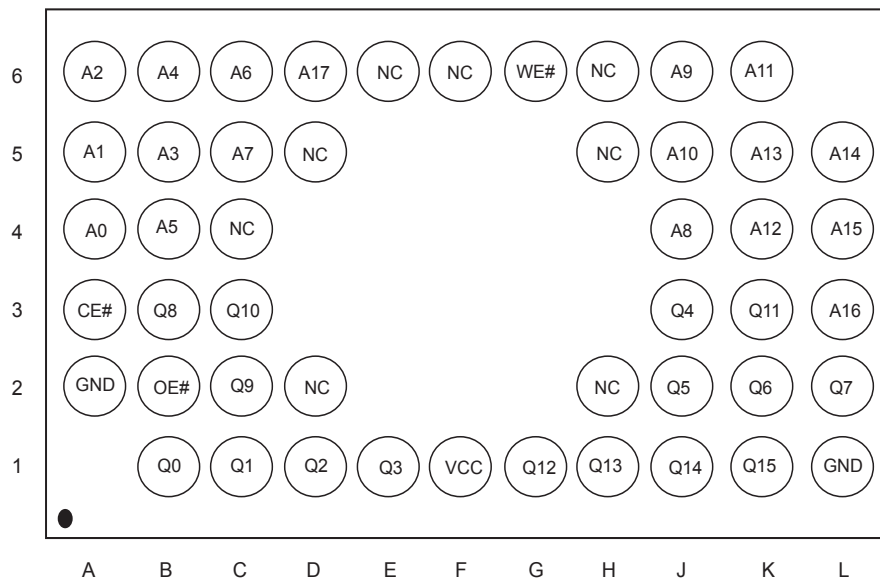
MX29LV400C 48 TSOP (Standard Type) (12mm x 20mm)



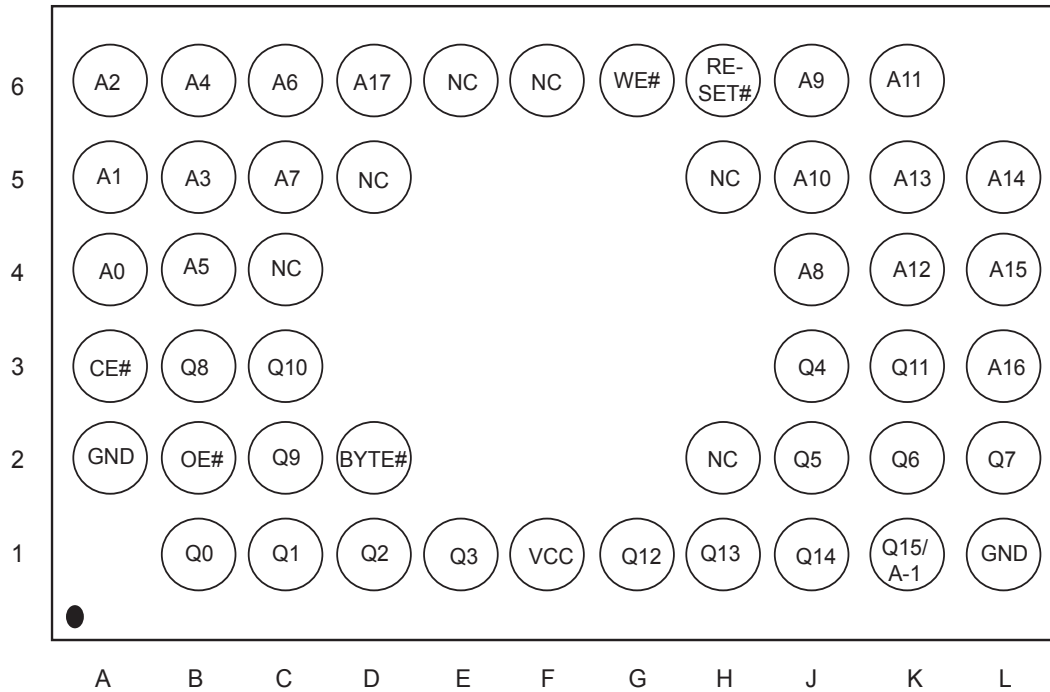
MX29LV400C 48-Ball TFBGA/LFBGA (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



MX29LV400C 48-Ball WFBGA (Balls Facing Down, 4 x 6 x 0.75 mm)

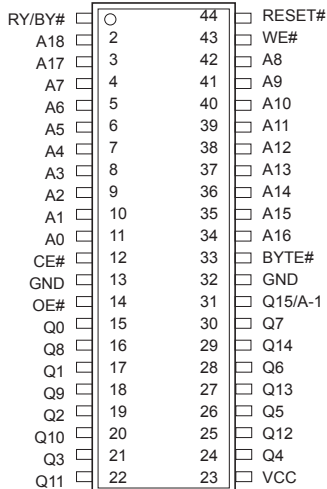


MX29LV400C 48-Ball XFLGA (Balls Facing Down, 4 x 6 x 0.5 mm)



MX29LV800C PIN CONFIGURATIONS

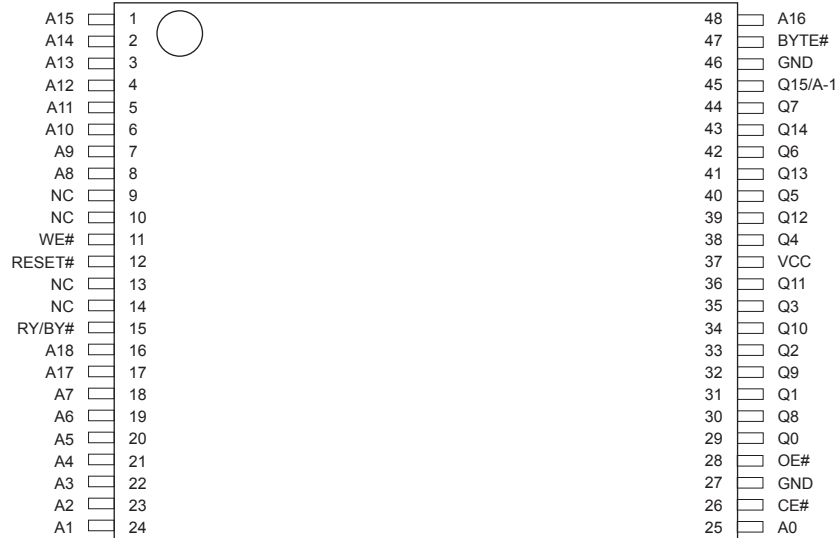
MX29LV800C 44 SOP(500 mil)



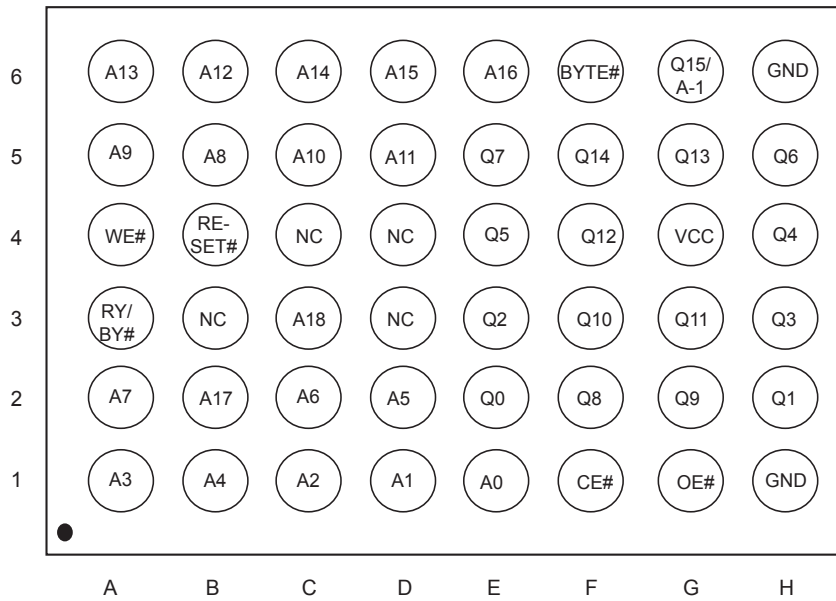
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin
NC	Pin Not Connected Internally

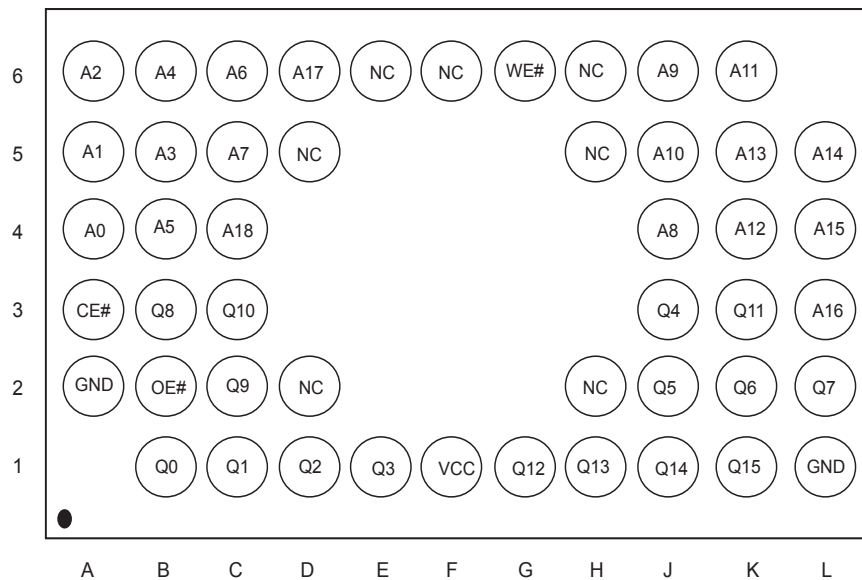
MX29LV800C 48 TSOP (Standard Type) (12mm x 20mm)



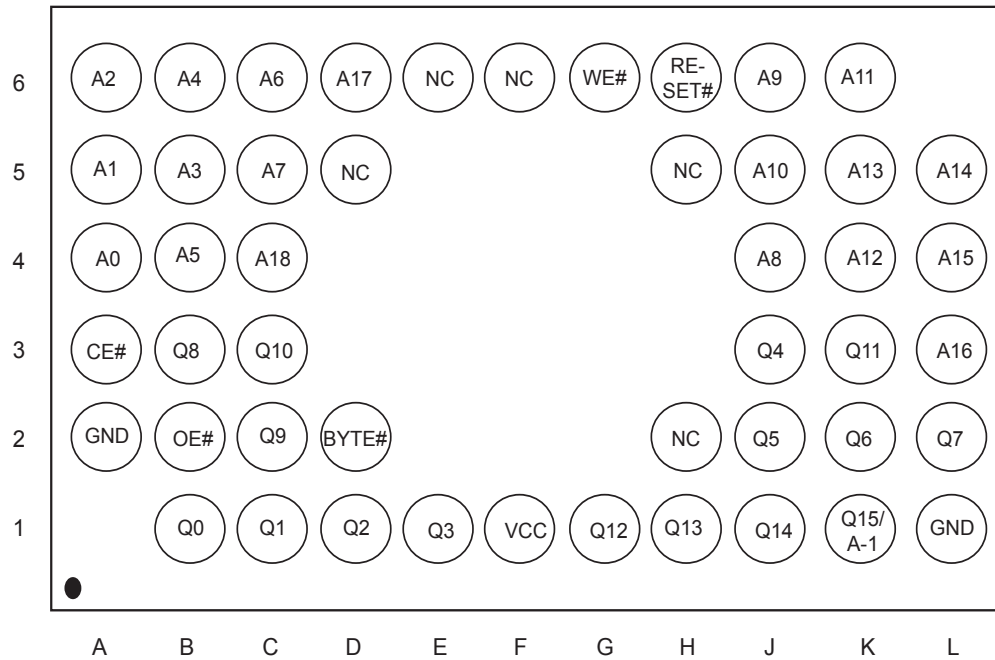
MX29LV800C 48-Ball TFBGA/LFBGA (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



MX29LV800C 48-Ball WFBGA (Balls Facing Down, 4 x 6 x 0.75 mm)

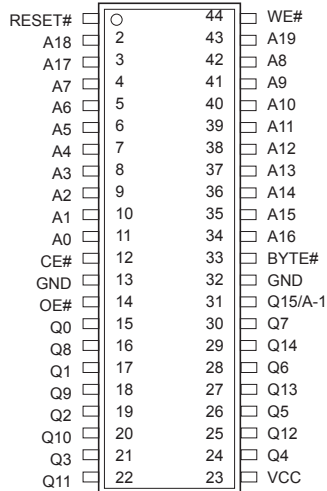


MX29LV800C 48-Ball XFLGA (Balls Facing Down, 4 x 6 x 0.5 mm)



MX29LV160C PIN CONFIGURATIONS

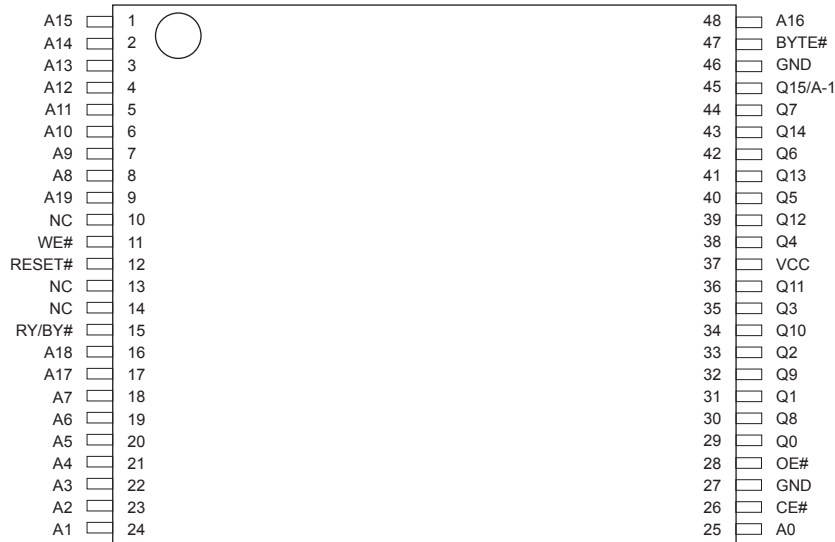
MX29LV160C 44 SOP(500 mil)



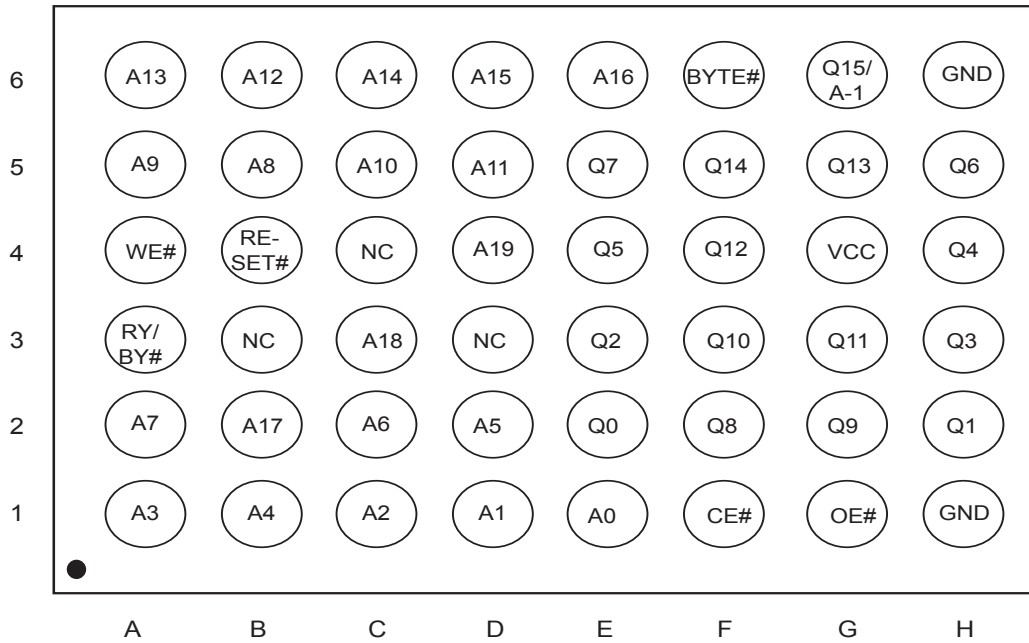
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
CE#	Chip Enable Input
WE#	Write Enable Input
BYTE#	Word/Byte Selection input
RESET#	Hardware Reset Pin/Sector Protect Unlock
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

MX29LV160C 48 TSOP (Standard Type) (12mm x 20mm)



MX29LV160C 48-Ball TFBGA/LFBGA (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



BLOCK DIAGRAM

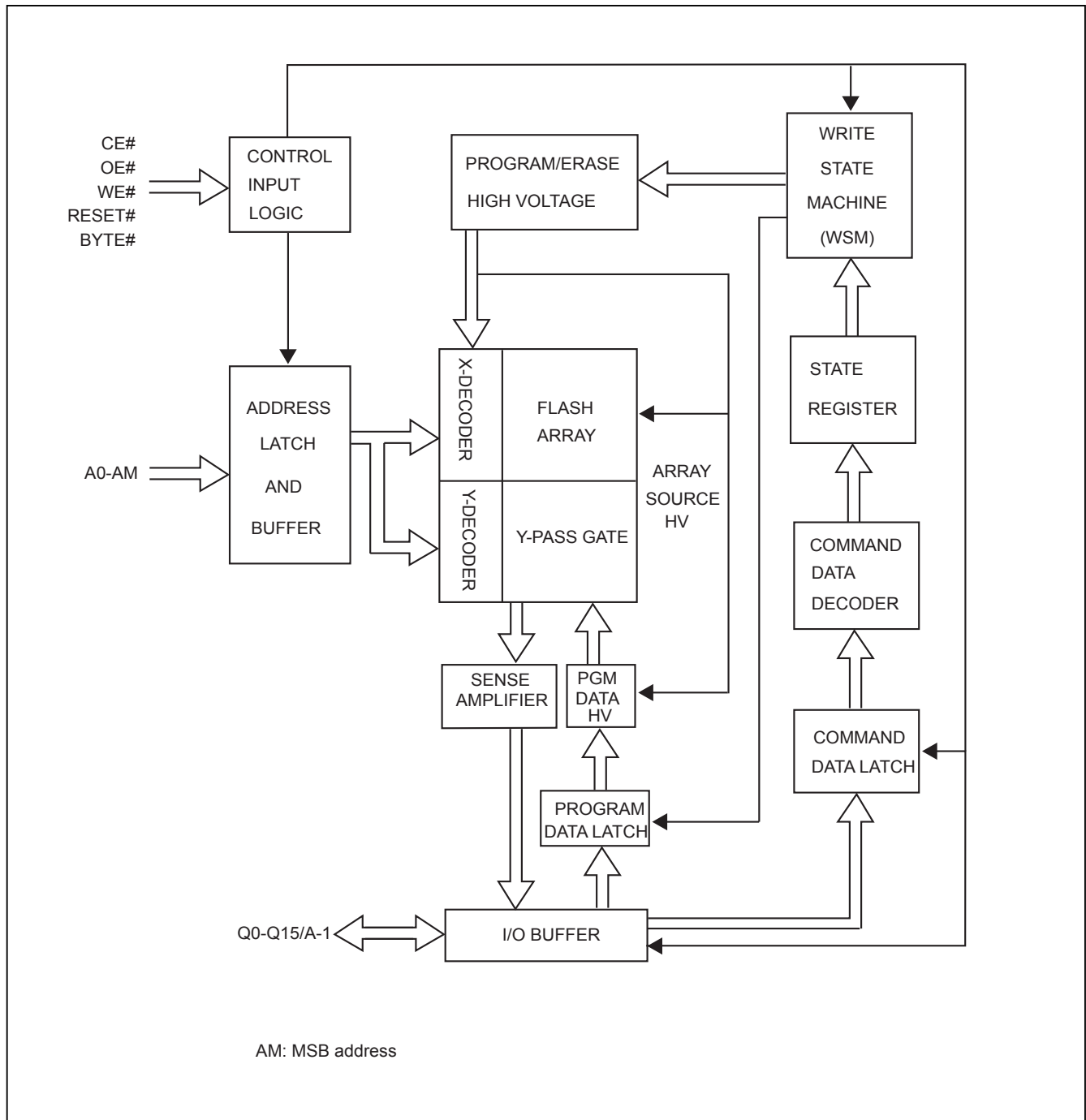


Table 1. BLOCK STRUCTURE

MX29LV400CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address					
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000-0FFFF	00000-07FFF	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000-1FFFF	08000-0FFFF	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000-2FFFF	10000-17FFF	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000-3FFFF	18000-1FFFF	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000-4FFFF	20000-27FFF	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000-5FFFF	28000-2FFFF	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000-6FFFF	30000-37FFF	1	1	0	X	X	X
SA7	32Kbytes	16Kwords	70000-77FFF	38000-3BFFF	1	1	1	0	X	X
SA8	8Kbytes	4Kwords	78000-79FFF	3C000-3CFFF	1	1	1	1	0	0
SA9	8Kbytes	4Kwords	7A000-7BFFF	3D000-3DFFF	1	1	1	1	0	1
SA10	16Kbytes	8Kwords	7C000-7FFFF	3E000-3FFFF	1	1	1	1	1	X

MX29LV400CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address					
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	00000-03FFF	00000-01FFF	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	04000-05FFF	02000-02FFF	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	06000-07FFF	03000-03FFF	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	08000-0FFFF	04000-07FFF	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	10000-1FFFF	08000-0FFFF	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	20000-2FFFF	10000-17FFF	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	30000-3FFFF	18000-1FFFF	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	40000-4FFFF	20000-27FFF	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	50000-5FFFF	28000-2FFFF	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	60000-6FFFF	30000-37FFF	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	70000-7FFFF	38000-3FFFF	1	1	1	X	X	X

MX29LV800CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address						
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000h-0FFFFh	00000h-07FFFh	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
SA15	32Kbytes	16Kwords	F0000h-F7FFFh	78000h-7BFFFh	1	1	1	1	0	X	X
SA16	8Kbytes	4Kwords	F8000h-F9FFFh	7C000h-7CFFFh	1	1	1	1	1	0	0
SA17	8Kbytes	4Kwords	FA000h-FBFFFh	7D000h-7DFFFh	1	1	1	1	1	0	1
SA18	16Kbytes	8Kwords	FC000h-FFFFFh	7E000h-7FFFFh	1	1	1	1	1	1	X

MX29LV800CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address						
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A18	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	00000h-03FFFh	00000h-01FFFh	0	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	04000h-05FFFh	02000h-02FFFh	0	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	06000h-07FFFh	03000h-03FFFh	0	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	08000h-0FFFFh	04000h-07FFFh	0	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
SA11	64Kbytes	32Kwords	80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
SA12	64Kbytes	32Kwords	90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
SA13	64Kbytes	32Kwords	A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
SA14	64Kbytes	32Kwords	B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
SA15	64Kbytes	32Kwords	C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
SA16	64Kbytes	32Kwords	D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
SA17	64Kbytes	32Kwords	E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
SA18	64Kbytes	32Kwords	F0000h-FFFFFh	78000h-7FFFFh	1	1	1	1	X	X	X

MX29LV160CT SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	000000-00FFFF	00000-07FFF	0	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA15	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA16	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA17	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA18	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA19	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA20	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA21	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA22	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA23	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA24	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA25	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA26	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA27	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA28	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA29	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA30	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-F7FFF	1	1	1	1	0	X	X	X
SA31	32Kbytes	16Kwords	1F0000-1F7FFF	F8000-FBFFF	1	1	1	1	1	0	X	X
SA32	8Kbytes	4Kwords	1F8000-1F9FFF	FC000-FCFFF	1	1	1	1	1	1	0	0
SA33	8Kbytes	4Kwords	1FA000-1FBFFF	FD000-FDFFF	1	1	1	1	1	1	0	1
SA34	16Kbytes	8Kwords	1FC000-1FFFFF	FE000-FFFFF	1	1	1	1	1	1	1	X

MX29LV160CB SECTOR ARCHITECTURE

Sector	Sector Size		Address range		Sector Address							
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A19	A18	A17	A16	A15	A14	A13	A12
SA0	16Kbytes	8Kwords	000000-003FFF	00000-01FFF	0	0	0	0	0	0	0	X
SA1	8Kbytes	4Kwords	004000-005FFF	02000-02FFF	0	0	0	0	0	0	1	0
SA2	8Kbytes	4Kwords	006000-007FFF	03000-03FFF	0	0	0	0	0	0	1	1
SA3	32Kbytes	16Kwords	008000-00FFFF	04000-07FFF	0	0	0	0	0	1	X	X
SA4	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	1	X	X	X
SA5	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	1	0	X	X	X
SA6	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	1	1	X	X	X
SA7	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	1	0	0	X	X	X
SA8	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	1	0	1	X	X	X
SA9	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	1	1	0	X	X	X
SA10	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	1	1	1	X	X	X
SA11	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	1	0	0	0	X	X	X
SA12	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	1	0	0	1	X	X	X
SA13	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	1	0	1	0	X	X	X
SA14	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	1	0	1	1	X	X	X
SA15	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	1	1	0	0	X	X	X
SA16	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	1	1	0	1	X	X	X
SA17	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	1	1	1	0	X	X	X
SA18	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	1	1	1	1	X	X	X
SA19	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	1	0	0	0	0	X	X	X
SA20	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	1	0	0	0	1	X	X	X
SA21	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	1	0	0	1	0	X	X	X
SA22	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	1	0	0	1	1	X	X	X
SA23	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	1	0	1	0	0	X	X	X
SA24	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	1	0	1	0	1	X	X	X
SA25	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	1	0	1	1	0	X	X	X
SA26	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFFF	1	0	1	1	1	X	X	X
SA27	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	1	1	0	0	0	X	X	X
SA28	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	1	1	0	0	1	X	X	X
SA29	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	1	1	0	1	0	X	X	X
SA30	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	1	1	0	1	1	X	X	X
SA31	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	1	1	1	0	0	X	X	X
SA32	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	1	1	1	0	1	X	X	X
SA33	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-FFFFF	1	1	1	1	0	X	X	X
SA34	64Kbytes	32Kwords	1F0000-1FFFFF	F8000-FFFFF	1	1	1	1	1	X	X	X

Table 2. BUS OPERATION--1

Mode Select	RE-SET#	CE#	WE#	OE#	Address	Data (I/O) Q7~Q0	Byte#	
							Vil	Vih
							Data (I/O) Q15~Q8	
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ
Standby Mode	Vcc± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ	DOUT
Write	H	L	L	H	AIN	DIN		DIN
Temporary Sector Unprotect	Vhv	X	X	X	AIN	DIN	HighZ	DIN
Sector Protect	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT	X	X
Chip Unprotect	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT	X	X

Note:

1. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
2. In Word Mode (Byte#=Vih), the addresses are AM to A0.
In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15).
3. AM: MSB of address.

BUS OPERATION--2

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q7~Q0	Q15~Q8
	CE#	WE#	OE#										
Sector Lock Status Verification	L	H	L	SA	x	V _{hv}	x	L	x	H	L	01h or 00h (Note1)	x
Read Silicon ID Manufacturer Code	L	H	L	x	x	V _{hv}	x	L	x	L	L	C2H	x
Read Silicon ID MX29LV400CT	L	H	L	x	x	V _{hv}	x	L	x	L	H	B9H	22h(Word) x (Byte)
Read Silicon ID MX29LV400CB	L	H	L	x	x	V _{hv}	x	L	x	L	H	BAH	22h(Word) x (Byte)
Read Silicon ID MX29LV800CT	L	H	L	x	x	V _{hv}	x	L	x	L	H	DAH	22h(Word) x (Byte)
Read Silicon ID MX29LV800CB	L	H	L	x	x	V _{hv}	x	L	x	L	H	5BH	22h(Word) x (Byte)
Read Silicon ID MX29LV160CT	L	H	L	x	x	V _{hv}	x	L	x	L	H	C4H	22h(Word) x (Byte)
Read Silicon ID MX29LV160CB	L	H	L	x	x	V _{hv}	x	L	x	L	H	49H	22h(Word) x (Byte)

Notes:

1. Sector unprotected code:00h. Sector protected code:01h.
2. AM: MSB of address.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of WE#, and all data are latched at the earlier rising edge of WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.
2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

RESET# OPERATION

Driving RESET# pin low for a period more than T_{rp} will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of T_{ready1} for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at $GND \pm 0.3V$, the device consumes standby current (I_{sb}). However, device draws larger current if RESET# pin is held at V_{il} but not within $GND \pm 0.3V$.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on that protected sector. MX29LV400C/MX29LV800C/MX29LV160C T/B provides two methods for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at V_{hv} . Refer to temporary sector unprotect operation for further details.

The first method is by applying V_{hv} on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for the algorithm for this method.

The other method is asserting V_{hv} on A9 and OE# pins, with A6 and CE# at V_{il} . The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV400C/MX29LV800C/MX29LV160C T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors are unprotected when shipped from the factory.

The first method is by applying V_{hv} on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for algorithm of the operation.

The other method is asserting V_{hv} on A9 and OE# pins, with A6 at V_{ih} and CE# at V_{il} (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at V_{hv} to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The device returns to normal operation once V_{hv} is removed from RESET# pin and previously protected sectors are again protected.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR PROTECT STATUS OPERATION

MX29LV400C/MX29LV800C/MX29LV160C T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires Vhv on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to Am pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than 1.4V. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than 1.4V and write cycles are ignored until Vcc is greater than 1.4V. System must provide proper signals on control pins after Vcc is larger than 1.4V to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.



MACRONIX
INTERNATIONAL Co., LTD.

MX29LV400C T/B
MX29LV800C T/B
MX29LV160C T/B

POWER-UP SEQUENCE

Upon power up, MX29LV400C/MX29LV800C/MX29LV160C T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at V_{il} and OE# is held at V_{ih} during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1 μ F capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29LV400C/MX29LV800C/MX29LV160C T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select						Program	
				Manufacturer ID		Device ID		Sector Protect Verify		Word	Byte
				Word	Byte	Word	Byte	Word	Byte		
1st Bus Cycle	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	555	2AA	555	2AA	555	2AA	555
	Data			55	55	55	55	55	55	55	55
3rd Bus Cycle	Addr			555	AAA	555	AAA	555	AAA	555	AAA
	Data			90	90	90	90	90	90	A0	A0
4th Bus Cycle	Addr			X00	X00	X01	X02	(Sector) X02	(Sector) X04	Addr	Addr
	Data			C2	C2	ID	ID	00/01	00/01	Data	Data
5th Bus Cycle	Addr										
	Data										
6th Bus Cycle	Addr										
	Data										

Command		Chip Erase		Sector Erase		CFI Read		Erase Suspend	Erase Resume
		Word	Byte	Word	Byte	Word	Byte	Byte/Word	Byte/Word
1st Bus Cycle	Addr	555	AAA	555	AAA	55	AA	XXX	XXX
	Data	AA	AA	AA	AA	98	98	B0	30
2nd Bus Cycle	Addr	2AA	555	2AA	555				
	Data	55	55	55	55				
3rd Bus Cycle	Addr	555	AAA	555	AAA				
	Data	80	80	80	80				
4th Bus Cycle	Addr	555	AAA	555	AAA				
	Data	AA	AA	AA	AA				
5th Bus Cycle	Addr	2AA	555	2AA	555				
	Data	55	55	55	55				
6th Bus Cycle	Addr	555	AAA	Sector	Sector				
	Data	10	10	30	30				

Notes:

1. Device ID : MX29LV400CT: 22B9; MX29LV400CB: 22BA.
MX29LV800CT: 22DA; MX29LV800CB: 225B.
MX29LV160CT: 22C4; MX29LV160CB: 2249.
2. For sector protect verify result, XX00H/00H means sector is not protected, XX01H/01H means sector has been protected.
3. Sector Protect command is valid during V_{hv} at RESET# pin, V_{ih} at A1 pin and V_{il} at A0, A6 pins. The last Bus cyc is for protect verify.
4. It is not allowed to adopt any other code which is not in the above command definition table.

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

Read Silicon ID	Address		Data (Hex)	Representation
Manufacturer ID	Word	X00	00C2	
	Byte	X00	C2	
Device ID	Word	X01	ID	Top/Bottom Boot Sector
	Byte	X02	ID	Top/Bottom Boot Sector
Sector Protect Verify	Word	(Sector address) X 02	00/01	Unprotected/protected
	Byte	(Sector address) X 04	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires V_hv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29LV400C/MX29LV800C/MX29LV160C T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV400C/MX29LV800C/MX29LV160C T/B is less than 36 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.

*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.

*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programming the data in the protected sector.